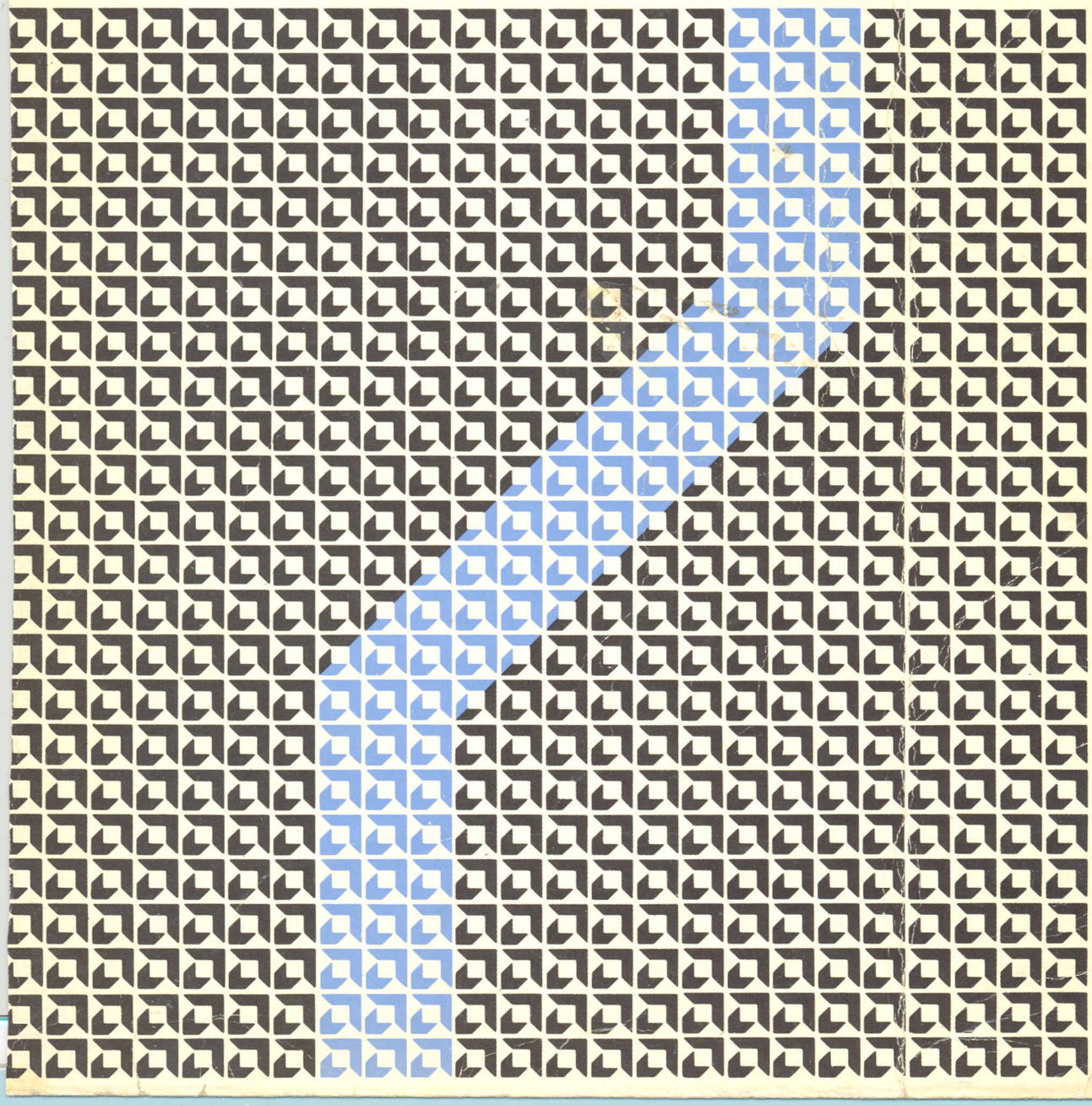
Advanced Micro Devices, Inc.

# MOS/LSI Data Book



# Advanced Micro Devices

## MOS/LSI Data Book

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AM-PUB118

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# TABLE OF CONTENTS


PRODUCT SELECTOR GUIDE ..... 1-1

MOS CROSS REFERENCE GUIDE ..... 1-5

RANDOM ACCESS MEMORIES:

| | | |
|---|---|---|
| Am9016 (Military) | 16384 x 1 Dynamic R/W Random Access Memory | 2-1 |
| Am9016 (Commercial) | 16384 x 1 Dynamic R/W Random Access Memory | 2-11 |
| Am9044/9244 | 4096 x 1 Static R/W Random Access Memory | 2-21 |
| Am9101/91L01/2101 Family | 256 x 4 Static R/W Random Access Memories | 2-25 |
| Am9111/91L11/2111 Family | 256 x 4 Static R/W Random Access Memories | 2-31 |
| Am9112/91L12 Family | 256 x 4 Static R/W Random Access Memories | 2-37 |
| Am9114/9124 | 1024 x 4 Static R/W Random Access Memory | 2-43 |
| Am9130/91L30 | 1024 x 4 Static R/W Random Access Memories | 2-47 |
| Am9131/91L31 | 1024 x 4 Static R/W Random Access Memories | 2-55 |
| Am9140/91L40 | 4096 x 1 Static R/W Random Access Memories | 2-57 |
| Am9141/91L41 | 4096 x 1 Static R/W Random Access Memories | 2-65 |
| Am9147 | 4096 x 1 Static R/W Random Access Memory | 2-67 |

UV ERASABLE-PROGRAMMABLE ROMs

| | | |
|---|---|---|
| Am1702A | 256-Word x 8-Bit Programmable Read-Only Memory | 3-1 |
| Am9708/2708 | 1024 x 8 Erasable Read Only Memory | 3-7 |
| Am2716 | 2048 x 8-Bit UV Erasable PROM | 3-11 |
| Am9732/Am2732 | 4096 x 8-Bit UV Erasable PROM | 3-16 |

READ ONLY MEMORIES

| | | |
|---|---|---|
| Am9208 | 1024 x 8 Read-Only Memory | 4-1 |
| Am9214/3514 | 512 x 8 Read-Only Memory | 4-5 |
| Am9216 | 2048 x 8 Read-Only Memory | 4-11 |
| Am9217/8316A | 2048 x 8 Read-Only Memory | 4-15 |
| Am9218/8316E | 2048 x 8 Read-Only Memory | 4-18 |
| Am9232/9233 | 4096 x 8 Read-Only Memory | 4-21 |

SHIFT REGISTERS:

| | | |
|---|---|---|
| Am14/1506Am14/1507 | Dual 100-Bit Dynamic Shift Registers | 5-1 |
| Am1402A/1403A/1404A/ Am2802/2803/2804 | 1024-Bit Dynamic Shift Registers | 5-7 |
| Am2805/2806/2807/2808 | 512- and 1024-Bit Dynamic Shift Registers | 5-13 |
| Am2809 | Dual 128-Bit Static Shift Register | 5-19 |
| Am2810 | Dual 128-Bit Static Shift Register | 5-23 |
| Am2814/3114 | Dual 128-Bit Static Shift Register | 5-27 |
| Am2825/2826/2827 | 2048-Bit Dynamic Shift Register | 5-31 |
| L4.00 Am2833/2533 | 1024-Bit Static Shift Registers | 5-36 |
| Am2847/2896 | Quad 80-Bit and Quad 96-Bit Static Shift Registers | 5-40 |
| Am2855/2856/2857 | Quad 128-Bit, Dual 256-Bit and Single 512-Bit Static Shift Registers | 5-44 |
| Am4025/5025/4026/5026/ 4027/5027 | 2048-Bit Dynamic Shift Registers | 5-48 |
| Am4055/5055/4056/5056/ 4057/5057 | Quad 128-Bit, Dual 256-Bit and Single 512-Bit Static Shift Registers | 5-53 |
| Am9401/2401 | Dual 1024-Bit Dynamic Shift Register | 5-57 |

FIRST-IN FIRST-OUT MEMORIES:

| | | |
|---|---|---|
| Am2812/2812A/ 17.95 2813/2813A | 32 x 8 and 32 x 9 First-In First-Out Memories | 6-1 |
| Am2841/3341/2841A | 64 x 4 First-In First-Out Memories | 6-7 |

# TABLE OF CONTENTS


PRODUCT SELECTOR GUIDE ..... 1-1

MOS CROSS REFERENCE GUIDE ..... 1-5

RANDOM ACCESS MEMORIES:

Am9016 (Military) 16384 x 1 Dynamic R/W Random Access Memory ..... 2-1

Am9016 (Commercial) 16384 x 1 Dynamic R/W Random Access Memory ..... 2-11

Am9044/9244 4096 x 1 Static R/W Random Access Memory ..... 2-21

Am9101/9L01/2101 Family 256 x 4 Static R/W Random Access Memories ..... 2-25

Am9111/9L11/2111 Family 256 x 4 Static R/W Random Access Memories ..... 2-31

Am9112/9L12 Family 256 x 4 Static R/W Random Access Memories ..... 2-37

Am9114/9124 1024 x 4 Static R/W Random Access Memory ..... 2-43

Am9130/9L30 1024 x 4 Static R/W Random Access Memories ..... 2-47

Am9131/9L31 1024 x 4 Static R/W Random Access Memories ..... 2-55

Am9140/9L40 4096 x 1 Static R/W Random Access Memories ..... 2-57

Am9141/9L41 4096 x 1 Static R/W Random Access Memories ..... 2-65

Am9147 4096 x 1 Static R/W Random Access Memory ..... 2-67

UV ERASABLE-PROGRAMMABLE ROMs

Am1702A 256-Word x 8-Bit Programmable Read-Only Memory ..... 3-1

Am2708/2708 1024 x 8 Erasable Read Only Memory ..... 3-7

Am2716 2048 x 8-Bit UV Erasable PROM ..... 3-11

Am2732/Am2732 4096 x 8-Bit UV Erasable PROM ..... 3-19

READ ONLY MEMORIES

Am9208 1024 x 8 Read-Only Memory ..... 4-1

Am9214/9314 512 x 8 Read-Only Memory ..... 4-5

Am9216 2048 x 8 Read-Only Memory ..... 4-11

Am9217/9316A 2048 x 8 Read-Only Memory ..... 4-15

Am9218/9316E 2048 x 8 Read-Only Memory ..... 4-19

Am9232/9232 4096 x 8 Read-Only Memory ..... 4-21

SHIFT REGISTERS:

Am1507 Dual 100-Bit Dynamic Shift Registers ..... 5-1

Am2804 1024-Bit Dynamic Shift Registers ..... 5-7

Am2806/2807/2808 512- and 1024-Bit Dynamic Shift Registers ..... 5-13

Am2809 Dual 128-Bit Static Shift Register ..... 5-19

Am2810 Dual 128-Bit Static Shift Register ..... 5-23

Am2814/3114 Dual 128-Bit Static Shift Register ..... 5-27

Am2825/2826/2827 2048-Bit Dynamic Shift Register ..... 5-31

Am2833/2834 1024-Bit Static Shift Registers ..... 5-36

Am2847/2886 Quad 80-Bit and Quad 96-Bit Static Shift Registers ..... 5-40

Am2857/2886/2857 Quad 128-Bit, Dual 256-Bit and Single 512-Bit Static Shift Registers ..... 5-44

Am4025/8026/4026/8026 402[illegible] 2048-Bit Dynamic Shift Registers ..... 5-48

Am4085/8085/4085/8085 405[illegible] Quad 128-Bit, Dual 256-Bit and Single 512-Bit Static Shift Registers ..... 5-53

Am9401/2401 Dual 1024-Bit Dynamic Shift Register ..... 5-57

FIRST-IN FIRST-OUT MEMORIES:

Am2812/2812A 32 x 8 and 32 x 9 First-In First-Out Memories ..... 6-1

Am2841/2841A 64 x 4 First-In First-Out Memories ..... 6-7

# TABLE OF CONTENTS (Cont.)


MICROPROCESSORS AND PERIPHERAL CIRCUITS:

| | | |
|---|---|---|
| Am8048/8035 | Single-Chip 8-Bit Microcomputers | 7-1 |
| Am8080A/9080A | 8-Bit Microprocessor | 7-5 |
| Am8085A/Am8085A-2/ 9085ADM | Single-Chip 8-Bit N-Channel Microprocessor | 7-13 |
| Am8155/8156 | 2048-Bit Static MOS RAM with I/O Ports and Timer | 7-26 |
| Am8251/9551 | Programmable Communications Interface | 7-36 |
| Am8253/8253-5 | Programmable Interval Timer | 7-43 |
| Am8255A/8255A-5 | Programmable Peripheral Interface | 7-49 |
| Am8257/9557 | Programmable DMA Controller | 7-54 |
| Am8279/8279-5 | Programmable Keyboard/Display Interface | 7-62 |
| Am9511A | Arithmetic Processor | 7-66 |
| Am9512 | Floating Point Processor | 7-91 |
| Am9513 | System Timing Controller | 7-110 |
| Am9517A | Multimode DMA Controller | 7-135 |
| Am9519A | Universal Interrupt Controller | 7-149 |

BIPOLAR SUPPORT PRODUCTS FOR MOS MICROPROCESSOR AND MEMORY SYSTEMS:

| | | |
|---|---|---|
| Am3212 | 8-Bit Input/Output Port | 8-58 |
| Am3216 | 4-Bit Bidirectional Bus Driver | 8-65 |
| Am3226 | 4-Bit Bidirectional Bus Driver | 8-65 |
| Am3448A | IEEE-488 Quad Bidirectional Bus Transceiver | 8-1 |
| AmZ8103 | Octal Bus Transceiver (Inverting) | 8-6 |
| AmZ8104 | Octal Bus Transceiver (Non-Inverting) | 8-6 |
| AmZ8107 | Octal Bus Transceiver (Inverting) | 8-12 |
| AmZ8108 | Octal Bus Transceiver (Non-Inverting) | 8-12 |
| AmZ8120 | Octal Register | 8-14 |
| AmZ8121 | 8-Bit Comparator | 8-18 |
| AmZ8127 | Clock Generator | 8-22 |
| AmZ8133 | Octal Latch (Inverting) | 8-23 |
| AmZ8136 | 8-Bit Decoder w/Storage | 8-28 |
| AmZ8140 | Octal 3-State Buffer (Inverting) | 8-32 |
| AmZ8144 | Octal 3-State Buffer (Non-Inverting) | 8-32 |
| AmZ8148 | Address Decoder w/Acknowledge | 8-36 |
| AmZ8160 | Error Detection and Correction Unit | 8-41 |
| AmZ8161 | EDC Bus Buffer (Inverting to Bus) | 8-49 |
| AmZ8162 | EDC Bus Buffer (Non-Inverting to Bus) | 8-49 |
| AmZ8163 | Refresh and EDC Controller | 8-50 |
| AmZ8164 | Dynamic Memory Controller | 8-51 |
| AmZ8165 | Dynamic RAM Driver (Inverting) | 8-52 |
| AmZ8166 | Dynamic RAM Driver (Non-Inverting) | 8-52 |
| AmZ8173 | Octal Latch (Non-Inverting) | 8-23 |
| Am8212 | 8-Bit Input/Output Port | 8-58 |
| Am8216 | 4-Bit Bidirectional Bus Driver (Non-Inverting) | 8-65 |
| Am8224 | Clock Generator | 8-70 |
| Am8226 | 4-Bit Bidirectional Bus Driver (Inverting) | 8-65 |
| Am8228 | System Controller/Bus Driver for Am9080A | 8-77 |
| Am8238 | System Controller/Bus Driver for Am9080A | 8-77 |

APPLICATION NOTES:

| | |
|---|---|
| Improved Performance with the Am9124 | 2-72 |
| Am9130/9140 | 9-1 |
| Application of First-In First-Out Memories | 9-17 |
| Algorithm Details for the Am9511 | 9-26 |
| Designing Interrupt Systems with the Am9519 | 9-49 |

APPENDICES

| | |
|---|---|
| Commitment to Excellence | A-1 |
| Product Assurance | B-1 |
| Packages | C-1 |

MICROPROCESSORS AND PERIPHERAL CIRCUITS

Am9080A/8080A Single-Chip 8-Bit Microcomputers ..... 7-1
Am8080A/8080A 8-Bit Microprocessor ..... 7-5
Am8085A/Am8085A-2 ..... 7-13
8085A/ADM Single-Chip 8-Bit N-Channel Microprocessor ..... 7-13
Am9516/8156 2048-Bit Static MOS RAM with I/O Ports and Timer ..... 7-26
Am8251/8551 Programmable Communications Interface ..... 7-38
Am8253/8253-5 Programmable Interval Timer ..... 7-43
Am8255A/8255A-5 Programmable Peripheral Interface ..... 7-49
Am9257/8567 Programmable DMA Controller ..... 7-54
Am8279/8279-5 Programmable Keyboard/Display Interface ..... 7-62
Am8841A Arithmetic Processor ..... 7-66
Am8512 Floating Point Processor ..... 7-91
Am9513 System Timing Controller ..... 7-110
Am8517A Multimode DMA Controller ..... 7-135
Am9519A Universal Interrupt Controller ..... 7-149

BIPOLAR SUPPORT PRODUCTS FOR MOS MICROPROCESSOR AND MEMORY SYSTEMS

Am3212 8-Bit Input/Output Port ..... 8-58
Am3216 4-Bit Bidirectional Bus Driver ..... 8-65
Am3226 4-Bit Bidirectional Bus Driver ..... 8-65
Am3486A IEEE-488 Quad Bidirectional Bus Transceiver ..... 9-1
Am8T03 Octal Bus Transceiver (Inverting) ..... 8-6
Am8T04 Octal Bus Transceiver (Non-Inverting) ..... 8-6
Am8T07 Octal Bus Transceiver (Inverting) ..... 8-12
Am8T08 Octal Bus Transceiver (Non-Inverting) ..... 8-12
Am8T20 Octal Register ..... 8-14
Am8T21 8-Bit Comparator ..... 8-18
Am8T27 Clock Generator ..... 8-22
Am8T33 Octal Latch (Inverting) ..... 8-23
Am8T38 8-Bit Decoder w/Storage ..... 8-28
Am8T40 Octal 3-State Buffer (Inverting) ..... 8-32
Am8T44 Octal 3-State Buffer (Non-Inverting) ..... 8-32
Am8T48 Address Decoder w/Acknowledge ..... 8-36
Am8T60 Error Detection and Correction Unit ..... 8-41
Am8T61 EDC Bus Buffer (Inverting to Bus) ..... 8-45
Am8T62 EDC Bus Buffer (Non-Inverting to Bus) ..... 8-49
Am8T63 Refresh and EDC Controller ..... 8-50
Am8T64 Dynamic Memory Controller ..... 8-51
Am8T65 Dynamic RAM Driver (Inverting) ..... 8-52
Am8T66 Dynamic RAM Driver (Non-Inverting) ..... 8-52
Am8T73 Octal Latch (Non-Inverting) ..... 8-23
Am8212 8-Bit Input/Output Port ..... 8-58
Am8216 4-Bit Bidirectional Bus Driver (Non-Inverting) ..... 8-65
Am8224 Clock Generator ..... 8-70
Am8226 4-Bit Bidirectional Bus Driver (Inverting) ..... 8-65
Am8228 System Controller/Bus Driver for Am9080A ..... 8-77
Am8238 System Controller/Bus Driver for Am9080A ..... 8-77

APPLICATION NOTES:

Improved Performance with the Am9124 ..... 2-72
Am9130/9140 ..... 9-1
Application of First-In First-Out Memories ..... 8-17
Algorithm Details for the Am9511 ..... 8-25
Designing Interrupt Systems with the Am9519 ..... 8-49

APPENDICES

Commitment to Excellence ..... A-1
Product Assurance ..... B-1
Packages ..... C-1

# PRODUCT SELECTOR GUIDE



## 1K STATIC RAMs

| Part Number | Organization | Access Time (ns) | Power Dissipation (mW) Standby | Active | Pins | Supply Voltage (V) | Temp. Range | Package |
|---|---|---|---|---|---|---|---|---|
| Am9101A | 256 x 4 | 500 | 47 | 290 | 22 | 5 | C, M | D, P |
| Am91L01A | 256 x 4 | 500 | 38 | 173 | 22 | 5 | C, M | D, P |
| Am9101B | 256 x 4 | 400 | 47 | 290 | 22 | 5 | C, M | D, P |
| Am91L01B | 256 x 4 | 400 | 38 | 173 | 22 | 5 | C, M | D, P |
| Am9101C | 256 x 4 | 300 | 47 | 315 | 22 | 5 | C, M | D, P |
| Am91L01C | 256 x 4 | 300 | 38 | 189 | 22 | 5 | C, M | D, P |
| Am9101D | 256 x 4 | 250 | 47 | 315 | 22 | 5 | C, M | D, P |
| Am9111A | 256 x 4 | 500 | 47 | 290 | 18 | 5 | C, M | D, P |
| Am91L11A | 256 x 4 | 500 | 38 | 173 | 18 | 5 | C, M | D, P |
| Am9111B | 256 x 4 | 400 | 47 | 290 | 18 | 5 | C, M | D, P |
| Am91L11B | 256 x 4 | 400 | 38 | 173 | 18 | 5 | C, M | D, P |
| Am9111C | 256 x 4 | 300 | 47 | 315 | 18 | 5 | C, M | D, P |
| Am91L11C | 256 x 4 | 300 | 38 | 189 | 18 | 5 | C, M | D, P |
| Am9111D | 256 x 4 | 250 | 47 | 315 | 18 | 5 | C | D, P |
| Am9112A | 256 x 4 | 500 | 47 | 290 | 16 | 5 | C, M | D, P |
| Am91L12A | 256 x 4 | 500 | 38 | 173 | 16 | 5 | C, M | D, P |
| Am9112B | 256 x 4 | 400 | 47 | 290 | 16 | 5 | C, M | D, P |
| Am91L12B | 256 x 4 | 400 | 38 | 173 | 16 | 5 | C, M | D, P |
| Am9112C | 256 x 4 | 300 | 47 | 315 | 16 | 5 | C, M | D, P |
| Am91L12C | 256 x 4 | 300 | 38 | 189 | 16 | 5 | C, M | D, P |
| Am9112D | 256 x 4 | 250 | 47 | 315 | 16 | 5 | C | D, P |

## 4K STATIC RAMs

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Am9044B | 4096 x 1 | 450 | | 350 | 18 | 5 | C, M | D, P |
| Am90L44B | 4096 x 1 | 450 | | 250 | 18 | 5 | C, M | D, P |
| Am9044C | 4096 x 1 | 300 | | 350 | 18 | 5 | C, M | D, P |
| Am90L44C | 4096 x 1 | 300 | | 250 | 18 | 5 | C, M | D, P |
| Am9044E | 4096 x 1 | 200 | | 350 | 18 | 5 | C | D, P |
| Am9244B | 4096 x 1 | 450 | 150 | 350 | 18 | 5 | C, M | D, P |
| Am92L44B | 4096 x 1 | 450 | 100 | 250 | 18 | 5 | C, M | D, P |
| Am9244C | 4096 x 1 | 300 | 150 | 350 | 18 | 5 | C, M | D, P |
| Am92L44C | 4096 x 1 | 300 | 100 | 250 | 18 | 5 | C, M | D, P |
| Am9244E | 4096 x 1 | 200 | 150 | 350 | 18 | 5 | C | D, P |
| Am9114B | 1024 x 4 | 450 | | 350 | 18 | 5 | C, M | D, P, F |
| Am91L14B | 1024 x 4 | 450 | | 250 | 18 | 5 | C, M | D, P, F |
| Am9114C | 1024 x 4 | 300 | | 350 | 18 | 5 | C, M | D, P, F |
| Am91L14C | 1024 x 4 | 300 | | 250 | 18 | 5 | C, M | D, P, F |
| Am9114E | 1024 x 4 | 200 | | 350 | 18 | 5 | C | D, P |
| Am9124B | 1024 x 4 | 450 | 150 | 350 | 18 | 5 | C, M | D, P, F |
| Am91L24B | 1024 x 4 | 450 | 100 | 250 | 18 | 5 | C, M | D, P, F |
| Am9124C | 1024 x 4 | 300 | 150 | 350 | 18 | 5 | C, M | D, P, F |
| Am91L24C | 1024 x 4 | 300 | 100 | 250 | 18 | 5 | C, M | D, P, F |
| Am9124E | 1024 x 4 | 200 | 150 | 350 | 18 | 5 | C | D, P |
| Am9130A | 1024 x 4 | 500 | 84 | 578 | 22 | 5 | C, M | D, P, F |
| Am91L30A | 1024 x 4 | 500 | 72 | 367 | 22 | 5 | C, M | D, P, F |
| Am9130B | 1024 x 4 | 400 | 84 | 578 | 22 | 5 | C, M | D, P, F |
| Am91L30B | 1024 x 4 | 400 | 72 | 367 | 22 | 5 | C, M | D, P, F |
| Am9130C | 1024 x 4 | 300 | 84 | 578 | 22 | 5 | C, M | D, P, F |
| Am91L30C | 1024 x 4 | 300 | 72 | 367 | 22 | 5 | C, M | D, P, F |
| Am9130D | 1024 x 4 | 250 | 84 | 578 | 22 | 5 | C, M | D, P, F |
| Am91L30D | 1024 x 4 | 250 | 78 | 367 | 22 | 5 | C | D, P |
| Am9130E | 1024 x 4 | 200 | 84 | 578 | 22 | 5 | C | D, P |
| Am9131A | 1024 x 4 | 500 | 84 | 578 | 22 | 5 | C, M | D, P, F |
| Am91L31A | 1024 x 4 | 500 | 72 | 367 | 22 | 5 | C, M | D, P, F |
| Am9131B | 1024 x 4 | 400 | 84 | 578 | 22 | 5 | C, M | D, P, F |
| Am91L31B | 1024 x 4 | 400 | 72 | 367 | 22 | 5 | C, M | D, P, F |
| Am9131C | 1024 x 4 | 300 | 84 | 578 | 22 | 5 | C, M | D, P, F |
| Am91L31C | 1024 x 4 | 300 | 72 | 367 | 22 | 5 | C, M | D, P, F |
| Am9131D | 1024 x 4 | 250 | 84 | 578 | 22 | 5 | C | D, P |
| Am91L31D | 1024 x 4 | 250 | 72 | 367 | 22 | 5 | C | D, P |
| Am9131E | 1024 x 4 | 200 | 84 | 578 | 22 | 5 | C | D, P |

# PRODUCT SELECTOR GUIDE (Cont.)

## 4K STATIC RAMs (Cont.)

| Part Number | Organization | Access Time (ns) | Power Dissipation (mW) Standby | Active | Pins | Supply Voltage (V) | Temp. Range | Package |
|---|---|---|---|---|---|---|---|---|
| Am9140A | 4096 x 1 | 500 | 84 | 578 | 22 | 5 | C, M | D, P, F |
| Am91L40A | 4096 x 1 | 500 | 72 | 367 | 22 | 5 | C, M | D, P, F |
| Am9140B | 4096 x 1 | 400 | 84 | 578 | 22 | 5 | C, M | D, P, F |
| Am91L40B | 4096 x 1 | 400 | 72 | 367 | 22 | 5 | C, M | D, P, F |
| Am9140C | 4096 x 1 | 300 | 84 | 578 | 22 | 5 | C, M | D, P, F |
| Am91L40C | 4096 x 1 | 300 | 72 | 367 | 22 | 5 | C, M | D, P, F |
| Am9140D | 4096 x 1 | 250 | 84 | 578 | 22 | 5 | C | D, P |
| Am91L40D | 4096 x 1 | 250 | 72 | 367 | 22 | 5 | C | D, P |
| Am91L40E | 4096 x 1 | 200 | 84 | 578 | 22 | 5 | C | D, P |
| Am9141A | 4096 x 1 | 500 | 84 | 367 | 22 | 5 | C, M | D, P, F |
| Am91L41A | 4096 x 1 | 500 | 72 | 578 | 22 | 5 | C, M | D, P, F |
| Am9141B | 4096 x 1 | 400 | 84 | 367 | 22 | 5 | C, M | D, P, F |
| Am91L41B | 4096 x 1 | 400 | 72 | 578 | 22 | 5 | C, M | D, P, F |
| Am9141C | 4096 x 1 | 300 | 84 | 367 | 22 | 5 | C, M | D, P, F |
| Am91L41C | 4096 x 1 | 300 | 72 | 578 | 22 | 5 | C, M | D, P, F |
| Am9141D | 4096 x 1 | 250 | 84 | 367 | 22 | 5 | C | D, P |
| Am91L41D | 4096 x 1 | 250 | 72 | 578 | 22 | 5 | C | D, P |
| Am9141E | 4096 x 1 | 200 | 84 | 367 | 22 | 5 | C | D, P |
| Am9147-70 | 4096 x 1 | 70 | 100 | 800 | 18 | 5 | C | D, P |
| Am9147-55 | 4096 x 1 | 55 | 150 | 900 | 18 | 5 | C | D, P |

## DYNAMIC RAMs

| Part Number | Organization | Access Time (ns) | Power Dissipation (mW) Standby | Active | Pins | Supply Voltage (V) | Temp. Range | Package |
|---|---|---|---|---|---|---|---|---|
| Am9016C | 16384 x 1 | 300 | 8 | 175 | 16 | +12 ±5 | C, L | P, D, F |
| Am9016D | 16384 x 1 | 250 | 8 | 175 | 16 | +12 ±5 | C, L | P, D, F |
| Am9016E | 16384 x 1 | 200 | 8 | 175 | 16 | +12 ±5 | C, L | P, D |
| Am9016F | 16384 x 1 | 150 | 8 | 175 | 16 | +12 ±5 | C | P, D |

## ROMs

| Part Number | Organization | Access Time (nsec) | Temp. Range | Supply Voltages | Operating Power Max (mW) | Outputs |
|---|---|---|---|---|---|---|
| Am9214 | 512 x 8 | 500 | C, M | +5 | 263 | 3-State |
| Am9208B | 1024 x 8 | 400 | C, M | +5, +12 | 620 | 3-State |
| Am9208C | 1024 x 8 | 300 | C, M | +5, +12 | 620 | 3-State |
| Am9216B | 2048 x 8 | 400 | C, M | +5, +12 | 660 | 3-State |
| Am9216C | 2048 x 8 | 300 | C | +5, +12 | 700 | 3-State |
| 8316A | 2048 x 8 | 550 | C, M | +5 | 515 | 3-State |
| Am9217A | 2048 x 8 | 550 | C, M | +5 | 368 | 3-State |
| Am9217B | 2048 x 8 | 450 | C, M | +5 | 368 | 3-State |
| 8316E | 2048 x 8 | 450 | C, M | +5 | 499 | 3-State |
| Am9218B | 2048 x 8 | 450 | C, M | +5 | 368 | 3-State |
| Am9218C | 2048 x 8 | 350 | C | +5 | 368 | 3-State |
| Am9232B | 4096 x 8 | 450 | C, M | +5 | 420 | 3-State |
| Am9232C | 4096 x 8 | 300 | C | +5 | 420 | 3-State |
| Am9233B | 4096 x 8 | 450 | C, M | +5 | 420 | 3-State |
| Am9233C | 4096 x 8 | 300 | C | +5 | 420 | 3-State |

# PRODUCT SELECTOR GUIDE (Cont.)

## U.V. ERASABLE PROMs

| Part Number | Organization | Access Time (ns) | Temp. Range | Operating Power – Act/Stby Max (mW) | Supply Voltages | Outputs | Number of Pins |
|---|---|---|---|---|---|---|---|
| Am1702A | 256 x 8 | 1000 | C, E | 676 | −9, +5 | 3-State | 24 |
| Am1702AL | 256 x 8 | 1000 | C, E | – | −9, +5 | 3-State | 24 |
| Am1702A-1 | 256 x 8 | 550 | C, E | 676 | −9, +5 | 3-State | 24 |
| Am1702AL-1 | 256 x 8 | 550 | C, E | – | −9, +5 | 3-State | 24 |
| Am1702A-2 | 256 x 8 | 650 | C, E | 676 | −9, +5 | 3-State | 24 |
| Am1702AL-2 | 256 x 8 | 650 | C, E | – | −9, +5 | 3-State | 24 |
| Am9708/2708 | 1024 x 8 | 450 | C, M | 800 | +5, +12, −5 | 3-State | 24 |
| Am2708-1 | 1024 x 8 | 350 | C | 800 | +5, +12, −5 | 3-State | 24 |
| Am2716 | 2048 x 8 | 450 | C | 525/132 | +5 | 3-State | 24 |
| Am2716-1 | 2048 x 8 | 350 | C | 525/132 | +5 | 3-State | 24 |
| Am2716-2 | 2048 x 8 | 390 | C | 525/132 | +5 | 3-State | 24 |
| Am2732 | 4096 x 8 | 450 | C | 787/157 | +5 | 3-State | 24 |

## FIRST-IN FIRST-OUT MEMORIES

| Part Number | Organization | Serial I/O | Fullness Flag | Output Enable | Package Pins | Data Rate MHz | Temp. Range |
|---|---|---|---|---|---|---|---|
| Am2812 | 32 x 8 | Yes | Yes | Yes | 28 | 0.5 | C, E* |
| Am2812A | 32 x 8 | Yes | Yes | Yes | 28 | 1.0 | C, E |
| Am2813 | 32 x 9 | No | Yes | Yes | 28 | 0.5 | C, E |
| Am2813A | 32 x 9 | No | Yes | Yes | 28 | 1.0 | C, E |
| Am2841 | 64 x 4 | No | No | No | 16 | 1.0 | C, E |
| Am2841A | 64 x 4 | No | No | No | 16 | 1.2 | C |

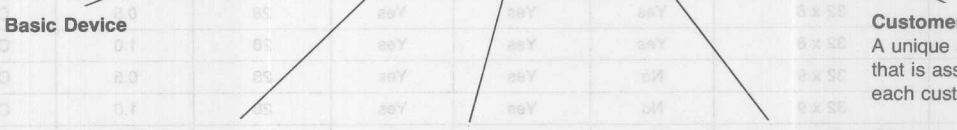
## SHIFT REGISTERS

| Part Number | Capacity/ Organization | Mode | Speed (MHz) | Supply Voltages | Clock Phases | TTL Clocks | Recirc Logic | Pins | Output |
|---|---|---|---|---|---|---|---|---|---|
| Am1507 | Dual 100 | Dynamic | 2 | +5, −5 | Two | No | No | 8 | Single-ended |
| Am2802 | Quad 256 | Dynamic | 10 | +5, −5 | Two | No | No | 16 | Single-ended |
| Am2803 | Dual 512 | Dynamic | 10 | +5, −5 | Two | No | No | 8 | Single-ended |
| Am2804 | Single 1024 | Dynamic | 10 | +5, −5 | Two | No | No | 8 | Single-ended |
| Am2805/Am2807 | Single 512 | Dynamic | 4 | +5, −5 | Two | No | Yes | 10/8 | Single-ended |
| Am2808 | Single 1024 | Dynamic | 4 | +5, −5 | Two | No | Yes | 8 | Single-ended |
| Am2827 | Single 2048 | Dynamic | 6 | +5, −10.5 | Two | No | Yes | 8 | Push-pull |
| Am9401/Am2401 | Dual 1024 | Dynamic | 2 | +5 | One | Yes | Yes | 16 | Single-ended |
| Am2809 | Dual 128 | Static | 2.5 | +5, −12 | One | Yes | Yes | 8 | Push-pull |
| Am2814 | Dual 128 | Static | 2.5 | +5, −12 | One | Yes | Yes | 16 | Push-pull |
| Am2833 | Single 1024 | Static | 2 | +5, −12 | One | Yes | Yes | 8 | Push-pull |
| Am2847 | Quad 80 | Static | 3 | +5, −12 | One | Yes | Yes | 16 | Push-pull |
| Am2855 | Quad 128 | Static | 2.5 | +5, −12 | One | Yes | Yes | 16 | Push-pull |
| Am2856 | Dual 256 | Static | 2.5 | +5, −12 | One | Yes | Yes | 10 | Push-pull |
| Am2857 | Single 512 | Static | 2.5 | +5, −12 | One | Yes | Yes | 8 | Push-pull |

*E is extended temperature range, −55°C to 85°C.

**Example:**

AM 9218 B PC 31500



**Basic Device**

**Customer Identifier**
A unique 5 digit code that is assigned to each customer pattern.

**Speed**
A = 500 or 550nsec
B = 400 or 450nsec
C = 300 or 350nsec
D = 250nsec

**Package Type**
P = Plastic
D = Side-Brazed
C = Cerdip

**Operating Temperature Range**
C = 0°C ≤ $T_A$ ≤ 70°C
I = −25°C ≤ $T_A$ ≤ +85°C
L = Special
M = −55°C ≤ $T_A$ ≤ +125°C

# MOS MEMORY CROSS REFERENCE

| AMI | AMD |
|---|---|
| S3514 | Am9214 |
| S4216B | Am9218 |
| S4264 | Am9264 |
| S6831A | Am9217 |
| S6831B | Am9218 |
| S68332 | Am9232 |
| S8865 | Am9208 |

| EA | AMD |
|---|---|
| EA-2308A | Am9208 |
| EA-2316A/8316A | Am9217 |
| EA-2316E/8316E | Am9218 |
| EA-4700 | Am9208 |
| EA-8332 | Am9232 |

| FAIRCHILD | AMD |
|---|---|
| F16K | Am9016 |
| F2114 | Am9114 |
| F2114L | Am9114 |
| F2533 | Am2833 |
| F2708 | Am2708 |
| F3341 | Am2841 |
| F3341A | Am2841A |
| F3347 | Am2847 |
| F3357-2 | Am2847 |
| F3508 | Am9208 |
| F3514 | Am9214 |
| F3515 | Am9214 |
| F3516E | Am9216 |

| G.I. | AMD |
|---|---|
| RO3-8316 | Am9217 |
| RO3-9322 | Am9232 |

| INTEL | AMD |
|---|---|
| 1402A | Am2802 |
| 1403A | Am2803 |
| 1404A | Am2804 |
| 1405A | Am2805 |
| 1406 | Am1406 |
| 1407 | Am1407 |
| 1506 | Am1506 |
| 1507 | Am1507 |
| 1702 | Am9708 |
| 1702A | Am1702A |
| 1702AL | Am1702AL |
| 2101A/8101A | Am9101 |
| 2111A/8111A | Am9111 |
| 2112A | Am9112 |
| 2114 | Am9114 |
| 2114L | Am9114 |
| 2117 | Am9016 |
| 2147 | Am9147 |
| 2148 | Am9148 |
| 2308/8308 | Am9208 |
| 2316A/8316A | Am9217 |
| 2316E/8316E | Am9218 |
| 2332 | Am9233 |
| 2364 | Am9265 |
| 2401 | Am2401 |
| 2405 | Am2405 |
| 2708 | Am2708 |

| MOSTEK | AMD |
|---|---|
| MK1002P | Am2810 |
| MK1007 | Am2847 |
| MK2147 | Am9147 |
| MK2600 | Am9214 |
| MK30000 | Am9208 |
| MK31000 | Am9217 |
| MK32000 | Am9232 |
| MK34000 | Am9218 |
| MK36000 | Am9264 |
| MK37000 | Am9265 |
| MK3702 | Am1702A |
| MK3708 | Am2708 |
| MK4116 | Am9016 |

| MOTOROLA | AMD |
|---|---|
| MCM2114 | Am9114 |
| MCM2147 | Am9147 |
| MCM4116 | Am9016 |
| MCM68308 | Am9208 |
| MCM68332 | Am9232 |
| MCM8316A | Am9217 |
| MCM8316E | Am9218 |

| NATIONAL | AMD |
|---|---|
| MM101A | Am1101A |
| MM1402A | Am2802 |
| MM1403A | Am2803 |
| MM1404A | Am2804 |
| MM1702A | Am1702A |
| MM2101A | Am9101 |
| MM2111A | Am9111 |
| MM2112A | Am9112 |
| MM2114 | Am9114 |
| MM2114L | Am9114 |
| MM2316A | Am9217 |
| MM2708 | Am2708 |
| MM4006 | Am1406 |
| MM4007 | Am1407 |
| MM4025 | Am2825 |
| MM4026 | Am2826 |
| MM4027 | Am2827 |
| MM4055 | Am2855 |
| MM4056 | Am2856 |
| MM4057 | Am2857 |
| MM5025 | Am2855 |
| MM5026 | Am2826 |
| MM5027 | Am2827 |
| MM5055 | Am2855 |
| MM5057 | Am2857 |
| MM5058 | Am2833 |
| MM5202AQ | Am1702A |
| MM52116 | Am9218 |
| MM52132 | Am9232 |
| MM5214 | Am9214 |
| MM52164 | Am9264 |
| MM5235 | Am9265 |
| MM5257 | Am9044 |
| MM5258 | Am9218 |
| MM5290 | Am9016 |

| NEC | AMD |
|---|---|
| μPD2308 | Am9208 |
| μPD2316A | Am9217 |
| μPD2316E | Am9218 |
| μPD2332 | Am9232 |

| SIGNETICS | AMD |
|---|---|
| 1702A | Am1702A |
| 2101 | Am9101 |
| 2111 | Am9111 |
| 2112 | Am9112 |
| 2501 | Am1101 |
| 2502 | Am2802 |
| 2503 | Am2803 |
| 2504 | Am2804 |
| 2505 | Am2805 |
| 2506 | Am1406/1506 |
| 2507 | Am1407/1507 |
| 2512 | Am2806 |
| 2521 | Am2809 |
| 2524 | Am2807 |
| 2525 | Am2808 |
| 2532 | Am2847 |
| 2533 | Am2833 |
| 2607 | Am9208 |
| 2616 | Am9218 |
| 2617 | Am9216 |
| 2632 | Am9232 |
| 2664 | Am9264 |

| SYNERTEK | AMD |
|---|---|
| SY1402 | Am2802 |
| SY1403 | Am2803 |
| SY1404 | Am2804 |
| SY2316A | Am9217 |
| SY2316E | Am9218 |
| SY2332 | Am9232 |
| SY2333 | Am9233 |
| SY2364 | Am9264 |
| SY2405 | Am2405 |
| SY2802 | Am2802 |
| SY2803 | Am2803 |
| SY2804 | Am2804 |
| SY2825 | Am2825 |
| SY2826 | Am2826 |
| SY2827 | Am2827 |
| SY2833 | Am2833 |
| SY3514 | Am9214 |
| SY3515 | Am9214 |

| T.I. | AMD |
|---|---|
| TMS2708 | Am2708 |
| TMS3114 | Am2814 |
| TMS3120 | Am2847 |
| TMS3128 | Am2809 |
| TMS3133 | Am2833 |
| TMS3406 | Am1406 |
| TMS3407 | Am1407 |
| TMS2412 | Am2802 |
| TMS3413 | Am2803 |
| TMS3414 | Am2804 |
| TMS40L44 | Am90L44 |
| TMS4044 | Am9044 |
| TMS40L45 | Am91L14 |
| TMS4045 | Am9114 |
| TMS4116 | Am9016 |
| TMS4244 | Am9244 |
| TMS4245 | Am9124 |
| TMS4700 | Am9208 |
| TMS4732 | Am9232 |
| SBP8316M | Am9218 |

# MOS MEMORY CROSS REFERENCE

| INTEL | AMD |
|---|---|
| 1402A | Am2302 |
| 1403A | Am2303 |
| 1404A | Am2704 |
| 1405A | Am2305 |
| 1408 | Am1406 |
| 1407 | Am1407 |
| 1602 | Am1302 |
| 1507 | Am1307 |
| 1702 | Am9708 |
| 1702A | Am1702A |
| 1702AL | Am1702AL |
| 2101A/P2101A | Am9101 |
| 2111A/P2111A | Am9111 |
| 2112A | Am9112 |
| 2114 | Am9114 |
| 2114L | Am9114 |
| 2127 | Am9216 |
| 2147 | Am9147 |
| 2148 | Am9148 |
| 2308/8308 | Am9308 |
| 2316A/2316A | Am9217 |
| 2316E/2316E | Am9218 |
| 2332 | Am9233 |
| 2364 | Am9265 |
| 2401 | Am2401 |
| 2405 | Am2405 |
| 2708 | Am2708 |

| EA | AMD |
|---|---|
| EA-2308A | Am9208 |
| EA-2316A/2316A | Am9217 |
| EA-2316E/2316E | Am9218 |
| EA-4700 | Am9708 |
| EA-6332 | Am9232 |

| FAIRCHILD | AMD |
|---|---|
| F16K | Am9016 |
| F2114 | Am9114 |
| F2114L | Am9114 |
| F2115 | Am2323 |
| F2708 | Am2708 |
| F3341 | Am2341 |
| F3341A | Am2341A |
| F3517 | Am3517 |
| F3517-2 | Am2347 |
| F3608 | Am9208 |
| F3614 | Am9214 |
| F3615 | Am9214 |
| F3615E | Am2216 |

| G.I. | AMD |
|---|---|
| RO3-8516 | Am9127 |
| RO3-8522 | Am9232 |

| MOSTEK | AMD |
|---|---|
| MK1002P | Am2810 |
| MK1007 | Am2847 |
| MK2147 | Am9147 |
| MK2560 | Am2514 |
| MK3000 | Am9208 |
| MK3100 | Am9217 |
| MK3200 | Am2232 |
| MK4060 | Am2218 |
| MK4096 | Am9284 |
| MK4200 | Am2283 |
| MK4702 | Am1702A |
| MK4708 | Am2708 |
| MK4116 | Am9016 |

| MOTOROLA | AMD |
|---|---|
| MCM2114 | Am9114 |
| MCM2147 | Am9147 |
| MCM4116 | Am9016 |
| MCM83308 | Am9208 |
| MCM83232 | Am9232 |
| MCM83164 | Am9217 |
| MCM8316E | Am9218 |

| NATIONAL | AMD |
|---|---|
| MM1013 | Am1813 |
| MM1402A | Am2802 |
| MM1403A | Am2803 |
| MM1404A | Am2804 |
| MM1702A | Am1702A |
| MM2101A | Am9101 |
| MM2111A | Am9111 |
| MM2112A | Am9112 |
| MM2114 | Am9114 |
| MM2114L | Am9114 |
| MM2316A | Am9217 |
| MM2708 | Am2708 |
| MM4006 | Am1406 |
| MM4007 | Am1407 |
| MM4028 | Am2828 |
| MM4029 | Am2829 |
| MM4027 | Am2827 |
| MM4055 | Am2865 |
| MM4056 | Am2866 |
| MM4057 | Am2867 |
| MM5025 | Am2825 |
| MM5026 | Am2826 |
| MM5027 | Am2827 |
| MM5058 | Am2858 |
| MM5059 | Am2859 |
| MM52/2AO | Am1702A |
| MM5214 | Am9218 |
| MM5218 | Am9232 |
| MM5234 | Am9234 |
| MM5256 | Am9284 |
| MM5257 | Am9044 |
| MM5258 | Am9218 |
| MM5280 | Am9016 |

| NEC | AMD |
|---|---|
| μPD2308 | Am9208 |
| μPD2316A | Am9217 |
| μPD2316E | Am9218 |
| μPD2332 | Am9232 |

| SIGNETICS | AMD |
|---|---|
| 1702A | Am1702A |
| 2101 | Am9101 |
| 2111 | Am9111 |
| 2112 | Am9112 |
| 2301 | Am1101 |
| 2302 | Am2802 |
| 2503 | Am2803 |
| 2504 | Am2804 |
| 2505 | Am2805 |
| 2506 | Am1406/1506 |
| 2507 | Am1427/1507 |
| 2512 | Am2809 |
| 2521 | Am2809 |
| 2524 | Am2807 |
| 2532 | Am2804 |
| 2533 | Am2847 |
| 2538 | Am2832 |
| 2607 | Am9208 |
| 2616 | Am9218 |
| 2617 | Am9216 |
| 2532 | Am9232 |
| 2564 | Am9264 |

| SYNERTEK | AMD |
|---|---|
| SY1402 | Am2802 |
| SY1403 | Am2803 |
| SY1404 | Am2804 |
| SY2316A | Am9217 |
| SY2316E | Am9218 |
| SY2332 | Am9232 |
| SY2333 | Am9233 |
| SY2364 | Am9264 |
| SY2405 | Am2405 |
| SY2802 | Am2802 |
| SY2803 | Am2803 |
| SY2804 | Am2804 |
| SY2805 | Am2805 |
| SY2826 | Am2826 |
| SY2827 | Am2827 |
| SY2833 | Am2833 |
| SY3514 | Am2814 |
| SY3515 | Am9216 |

| TI | AMD |
|---|---|
| TMS2708 | Am2708 |
| TMS3114 | Am2814 |
| TMS3120 | Am2847 |
| TMS3128 | Am2809 |
| TMS3134 | Am2833 |
| TMS3408 | Am1408 |
| TMS3407 | Am1407 |
| TMS3412 | Am2802 |
| TMS3413 | Am2803 |
| TMS3414 | Am2804 |
| TMS4044 | Am9044 |
| TMS4060 | Am9016 |
| TMS4116 | Am9016 |
| TMS4244 | Am9244 |
| TMS4316 | Am9016 |
| TMS4720 | Am9208 |
| TMS4732 | Am9232 |
| SBP9318M | Am9218 |

# Random Access Memories

2

## NUMERICAL INDEX


| | | Page |
|---|---|---|
| Am2101 | 256 x 4 Static | 2-25 |
| Am2111 | 256 x 4 Static | 2-31 |
| Am9016 | 16384 x 1 Dynamic (Military Version) | 2-1 |
| Am9016 | 16384 x 1 Dynamic (Commercial Version) | 2-11 |
| Am9044 | 4096 x 1 Static | 2-21 |
| Am9101 | 256 x 4 Static | 2-25 |
| Am91L01 | 256 x 4 Static | 2-25 |
| Am9111 | 256 x 4 Static | 2-31 |
| Am91L11 | 256 x 4 Static | 2-31 |
| Am9112 | 256 x 4 Static | 2-37 |
| Am91L12 | 256 x 4 Static | 2-37 |
| Am9114 | 1024 x 4 Static | 2-43 |
| Am9124 | 1024 x 4 Static | 2-43 |
| Am9130 | 1024 x 4 Static | 2-47 |
| Am91L30 | 1024 x 4 Static | 2-47 |
| Am9131 | 1024 x 4 Static | 2-55 |
| Am91L31 | 1024 x 4 Static | 2-55 |
| Am9140 | 4096 x 1 Static | 2-57 |
| Am91L40 | 4096 x 1 Static | 2-57 |
| Am9141 | 4096 x 1 Static | 2-65 |
| Am91L41 | 4096 x 1 Static | 2-65 |
| Am9147 | 4096 x 1 Static | 2-67 |
| Am9244 | 4096 x 1 Static | 2-21 |

**Application Note**

Improved Performance with the Am9124 ..... 2-72

2

# NUMERICAL INDEX


| | | Page |
|---|---|---|
| Am2101 | 256 x 4 Static | 2-25 |
| Am2111 | 256 x 4 Static | 2-31 |
| Am9016 | 16384 x 1 Dynamic (Military Version) | 2-1 |
| Am9016 | 16384 x 1 Dynamic (Commercial Version) | 2-11 |
| Am9044 | 4096 x 1 Static | 2-21 |
| Am9101 | 256 x 4 Static | 2-25 |
| Am91L01 | 256 x 4 Static | 2-29 |
| Am9111 | 256 x 4 Static | 2-31 |
| Am91L11 | 256 x 4 Static | 2-31 |
| Am9112 | 256 x 4 Static | 2-37 |
| Am91L12 | 256 x 4 Static | 2-37 |
| Am9114 | 1024 x 4 Static | 2-43 |
| Am9124 | 1024 x 4 Static | 2-43 |
| Am9130 | 1024 x 4 Static | 2-47 |
| Am91L30 | 1024 x 4 Static | 2-47 |
| Am9131 | 1024 x 4 Static | 2-55 |
| Am91L31 | 1024 x 4 Static | 2-55 |
| Am9140 | 4096 x 1 Static | 2-57 |
| Am91L40 | 4096 x 1 Static | 2-57 |
| Am9141 | 4096 x 1 Static | 2-65 |
| Am91L41 | 4096 x 1 Static | 2-65 |
| Am9147 | 4096 x 1 Static | 2-67 |
| Am9244 | 4096 x 1 Static | 2-71 |


Application Note


Improved Performance with the Am9124 ..... 2-72

# Am9016

## Extended Operating Temperature Range
## 16,384 x 1 Dynamic R/W Random Access Memory

2

### DISTINCTIVE CHARACTERISTICS

- High density 16K x 1 organization
- Replacement for MK4116 (P)-83/84
- Low maximum power dissipation – 462mW active, 20mW standby
- High speed operation – 200ns access, 375ns cycle
- ±10% tolerance on standard +12, +5, −5 voltages
- TTL compatible interface signals
- Three-state output
- RAS only, RMW and Page mode clocking options
- 128 cycle refreshing
- Unlatched data output
- Standard 16-pin, .3 inch wide dual-in-line package
- Double poly N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing
- Extended ambient operating temperature (−55 to +85°C)

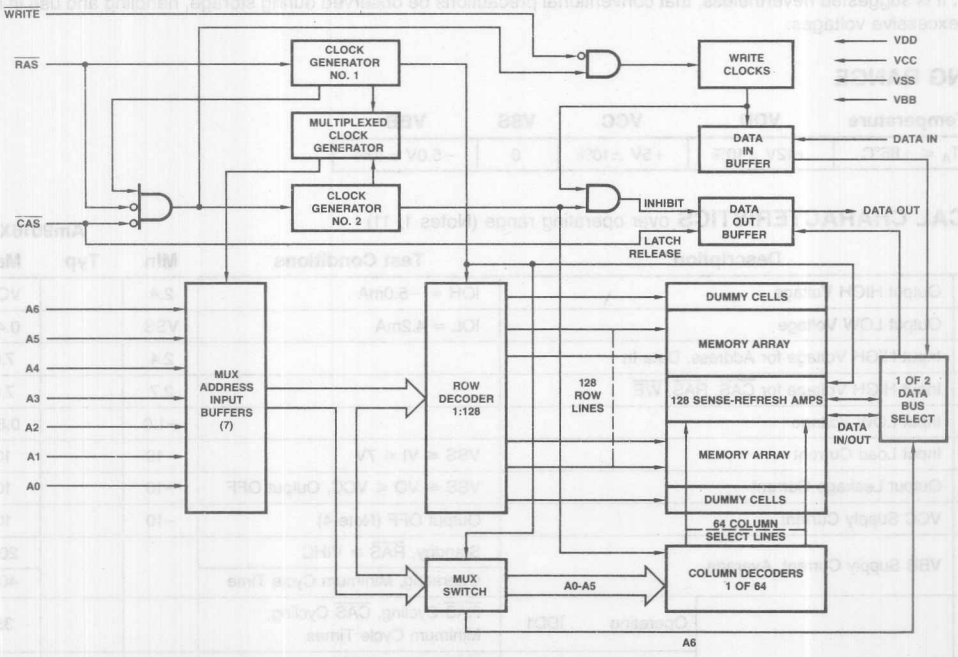
### GENERAL DESCRIPTION

The Am9016 is a high-speed, 16K-bit, dynamic, read/write random access memory. It is organized as 16,384 words by 1 bit per word and is packaged in a standard 16-pin DIP or 18-pin leadless chip carrier. The basic memory element is a single transistor cell that stores charge on a small capacitor. This mechanism requires periodic refreshing of the memory cells to maintain stored information.

All input signals, including the two clocks, are TTL compatible. The Row Address Strobe ($\overline{RAS}$) loads the row address and the Column Address Strobe ($\overline{CAS}$) loads the column address. The row and column address signals share seven input lines. Active cycles are initiated when $\overline{RAS}$ goes low, and standby mode is entered when $\overline{RAS}$ goes high. In addition to normal read and write cycles, other types of operations are available to improve versatility, performance and power dissipation.

The 3-state output buffer turns on when the column access time has elapsed and turns off after $\overline{CAS}$ goes high. Input and output data are the same polarity.

### BLOCK DIAGRAM



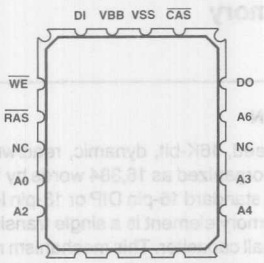

MOS-190

### ORDERING INFORMATION

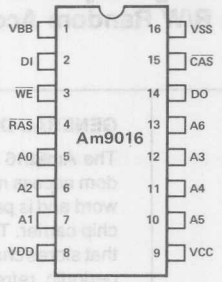
| Ambient Temperature | Package Type | Access Time | | |
|---|---|---|---|---|
| | | 300ns | 250ns | 200ns |
| −55°C ≤ $T_A$ ≤ +85°C | Hermetic DIP | AM9016CDL | AM9016DDL | AM9016EDL |
| | Chip Carrier | AM9016CZL | AM9016DZL | AM9016EZL |

## CONNECTION DIAGRAMS

**Leadless Chip Carrier**




**DIP**




Top Views

| | |
|---|---|
| A0 – A6 | ADDRESS INPUTS |
| CAS | COLUMN ADDRESS STROBE |
| DI | DATA IN |
| DO | DATA OUT |
| RAS | ROW ADDRESS STROBE |
| VDD | POWER (+12V) |
| VCC | POWER (+5V) |
| VSS | GROUND |
| VBB | POWER (–5V) |
| WE | WRITE ENABLE |

MOS-191

## MAXIMUM RATINGS above which useful life may be impaired

| | |
|---|---|
| Storage Temperature | –65 to +150°C |
| Ambient Temperature Under Bias | –55 to +85°C |
| Voltage on Any Pin Relative to VBB | –0.5 to +20V |
| VDD and VCC Supply Voltages with Respect to VSS | –1.0 to +15.0V |
| VBB – VSS (VDD – VSS > 0V) | 0V |
| Power Dissipation | 1.0W |
| Short Circuit Output Current | 50mA |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGE

| Ambient Temperature | VDD | VCC | VSS | VBB |
|---|---|---|---|---|
| $-55°C \leq T_A \leq +85°C$ | +12V ±10% | +5V ±10% | 0 | –5.0V ±10% |

## ELECTRICAL CHARACTERISTICS over operating range (Notes 1, 11)

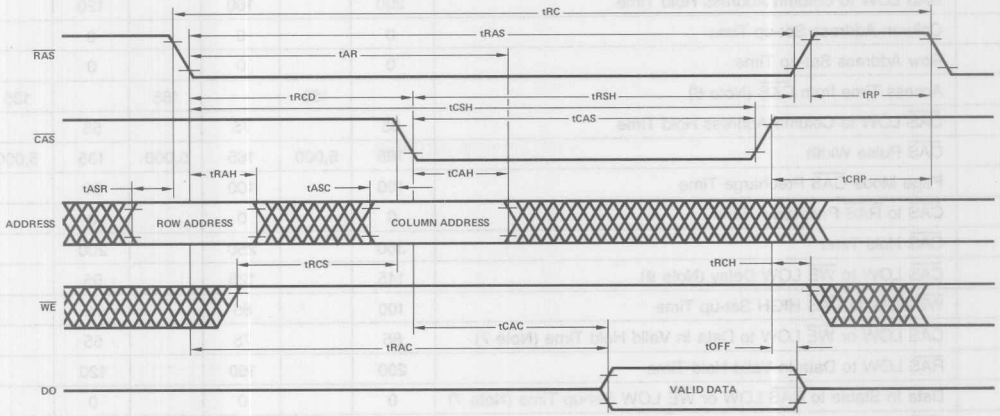
| Parameters | Description | | Test Conditions | Am9016X Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| VOH | Output HIGH Voltage | | IOH = –5.0mA | 2.4 | | VCC | Volts |
| VOL | Output LOW Voltage | | IOL = 4.2mA | VSS | | 0.40 | Volts |
| VIH | Input HIGH Voltage for Address, Data In | | | 2.4 | | 7.0 | Volts |
| VIHC | Input HIGH Voltage for CAS, RAS, WE | | | 2.7 | | 7.0 | Volts |
| VIL | Input LOW Voltage | | | –1.0 | | 0.80 | Volts |
| IIX | Input Load Current | | VSS ≤ VI ≤ 7V | –10 | | 10 | µA |
| IOZ | Output Leakage Current | | VSS ≤ VO ≤ VCC, Output OFF | –10 | | 10 | µA |
| ICC | VCC Supply Current | | Output OFF (Note 4) | –10 | | 10 | µA |
| IBB | VBB Supply Current, Average | | Standby, RAS ≥ VIHC | | | 200 | µA |
| | | | Operating, Minimum Cycle Time | | | 400 | |
| IDD | VDD Supply Current, Average | Operating IDD1 | RAS Cycling, CAS Cycling, Minimum Cycle Times | | | 35 | mA |
| | | Page Mode IDD4 | RAS ≤ VIL, CAS Cycling, Minimum Cycle Times | | | 27 | |
| | | RAS – Only Refresh IDD3 | RAS Cycling, CAS ≥ VIHC, Minimum Cycle Times | | | 27 | |
| | | Standby IDD2 | RAS ≥ VIHC | | | 2.25 | |
| CI | Input Capacitance | RAS, CAS, WE | Inputs at 0V, f = 1MHz, Nominal Supply Voltages | | | 10.0 | pF |
| | | Address, Data In | | | | 5.0 | |
| CO | Output Capacitance | | Output OFF | | | 7.0 | |

## SWITCHING CHARACTERISTICS over operating range (Notes 2, 3, 5, 10)

| Parameters | Description | Am9016C Min | Am9016C Max | Am9016D Min | Am9016D Max | Am9016E Min | Am9016E Max | Units |
|---|---|---|---|---|---|---|---|---|
| tAR | $\overline{RAS}$ LOW to Column Address Hold Time | 200 | | 160 | | 120 | | ns |
| tASC | Column Address Set-up Time | 0 | | 0 | | 0 | | ns |
| tASR | Row Address Set-up Time | 0 | | 0 | | 0 | | ns |
| tCAC | Access Time from $\overline{CAS}$ (Note 6) | | 185 | | 165 | | 135 | ns |
| tCAH | $\overline{CAS}$ LOW to Column Address Hold Time | 85 | | 75 | | 55 | | ns |
| tCAS | $\overline{CAS}$ Pulse Width | 185 | 5,000 | 165 | 5,000 | 135 | 5,000 | ns |
| tCP | Page Mode $\overline{CAS}$ Precharge Time | 100 | | 100 | | 80 | | ns |
| tCRP | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | 0 | | 0 | | 0 | | ns |
| tCSH | $\overline{CAS}$ Hold Time | 300 | | 250 | | 200 | | ns |
| tCWD | $\overline{CAS}$ LOW to $\overline{WE}$ LOW Delay (Note 9) | 145 | | 125 | | 95 | | ns |
| tCWL | $\overline{WE}$ LOW to $\overline{CAS}$ HIGH Set-up Time | 100 | | 85 | | 70 | | ns |
| tDH | $\overline{CAS}$ LOW or $\overline{WE}$ LOW to Data In Valid Hold Time (Note 7) | 85 | | 75 | | 55 | | ns |
| tDHR | $\overline{RAS}$ LOW to Data In Valid Hold Time | 200 | | 160 | | 120 | | ns |
| tDS | Data In Stable to $\overline{CAS}$ LOW or $\overline{WE}$ LOW Set-up Time (Note 7) | 0 | | 0 | | 0 | | ns |
| tOFF | $\overline{CAS}$ HIGH to Output OFF Delay | 0 | 60 | 0 | 60 | 0 | 50 | ns |
| tPC | Page Mode Cycle Time | 295 | | 275 | | 225 | | ns |
| tRAC | Access Time from $\overline{RAS}$ (Note 6) | | 300 | | 250 | | 200 | ns |
| tRAH | $\overline{RAS}$ LOW to Row Address Hold Time | 45 | | 35 | | 25 | | ns |
| tRAS | $\overline{RAS}$ Pulse Width | 300 | 5,000 | 250 | 5,000 | 200 | 5,000 | ns |
| tRC | Random Read or Write Cycle Time | 460 | | 410 | | 375 | | ns |
| tRCD | $\overline{RAS}$ LOW to $\overline{CAS}$ LOW Delay (Note 6) | 35 | 115 | 35 | 85 | 25 | 65 | ns |
| tRCH | Read Hold Time | 0 | | 0 | | 0 | | ns |
| tRCS | Read Set-up Time | 0 | | 0 | | 0 | | ns |
| tREF | Refresh Interval | | 2 | | 2 | | 2 | ms |
| tRMW | Read Modify Write Cycle Time | 600 | | 500 | | 405 | | ns |
| tRP | $\overline{RAS}$ Precharge Time | 150 | | 150 | | 120 | | ns |
| tRSH | $\overline{CAS}$ LOW to $\overline{RAS}$ HIGH Delay | 185 | | 165 | | 135 | | ns |
| tRWC | Read/Write Cycle Time | 525 | | 425 | | 375 | | ns |
| tRWD | $\overline{RAS}$ LOW to $\overline{WE}$ LOW Delay (Note 9) | 260 | | 210 | | 160 | | ns |
| tRWL | $\overline{WE}$ LOW to $\overline{RAS}$ HIGH Set-up Time | 100 | | 85 | | 70 | | ns |
| tT | Transition Time | 3 | 50 | 3 | 50 | 3 | 50 | ns |
| tWCH | Write Hold Time | 85 | | 75 | | 55 | | ns |
| tWCR | $\overline{RAS}$ LOW to Write Hold Time | 200 | | 160 | | 120 | | ns |
| tWCS | $\overline{WE}$ LOW to $\overline{CAS}$ LOW Set-up Time (Note 9) | 0 | | 0 | | 0 | | ns |
| tWP | Write Pulse Width | 85 | | 75 | | 55 | | ns |

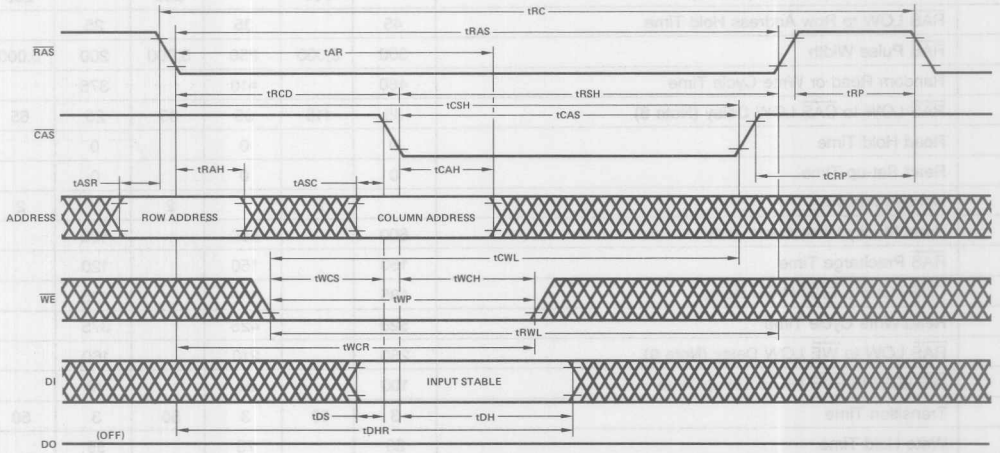
**NOTES**

1. Typical values are for $T_A$ = 25°C, nominal supply voltages and nominal processing parameters.
2. Signal transition times are assumed to be 5ns. Transition times are measured between specified high and low logic levels.
3. Timing reference levels for both input and output signals are the specified worst-case logic levels.
4. VCC is used in the output buffer only. ICC will therefore depend only on leakage current and output loading. When the output is ON and at a logic high level, VCC is connected to the Data Out pin through an equivalent resistance of approximately 135Ω. In standby mode VCC may be reduced to zero without affecting stored data or refresh operations.
5. Output loading is two standard TTL loads plus 100pF capacitance.
6. Both $\overline{RAS}$ and $\overline{CAS}$ must be low to read data. Access timing will depend on the relative positions of their falliing edges. When tRCD is less than the maximum value shown, access time depends on $\overline{RAS}$ and tRAC governs. When tRCD is more than the maximum value shown access time depends on $\overline{CAS}$ and tCAC governs. The maximum value listed for tRCD is shown for reference purposes only and does not restrict operation of the part.
7. Timing reference points for data input set-up and hold times will depend on what type of write cycle is being performed and will be the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
8. At least eight initialization cycles that exercise $\overline{RAS}$ should be performed after power-up and before valid operations are begun.
9. The tWCS, tRWD and tCWD parameters are shown for reference purposes only and do not restrict the operating flexibility of the part. When the falling edge of $\overline{WE}$ follows the falling edge of $\overline{CAS}$ by at most tWCS, the data output buffer will remain off for the whole cycle and an "early write" cycle is defined. When the falling edge of $\overline{WE}$ follows the falling edges of $\overline{RAS}$ and $\overline{CAS}$ by at least tRWD and tCWD respectively, the Data Out from the addressed cell will be valid at the access time and a "read/write" cycle is defined. The falling edge of $\overline{WE}$ may also occur at intermediate positions, but the condition and validity of the Data Out signal will not be known.
10. Switching characteristics are listed in alphabetical order.
11. All voltages referenced to VSS.



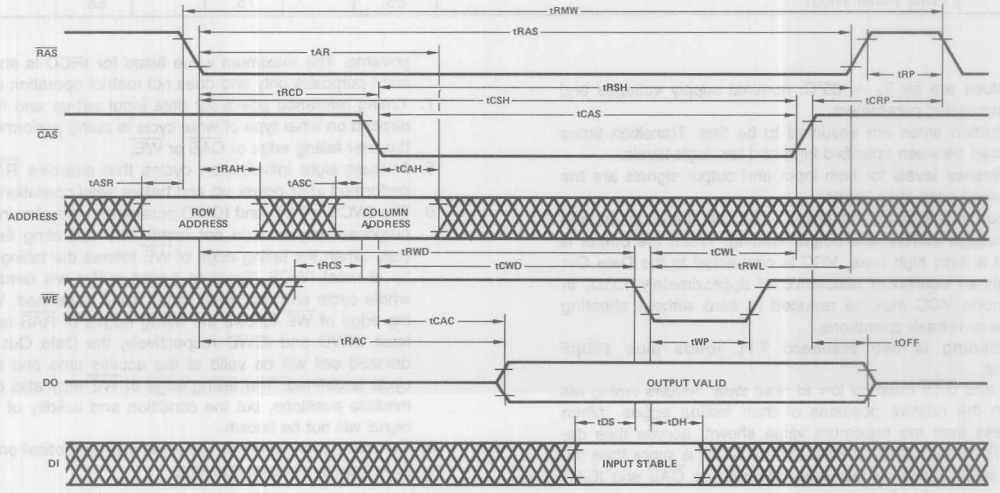

MOS-192

## WRITE CYCLE (EARLY WRITE)




MOS-193

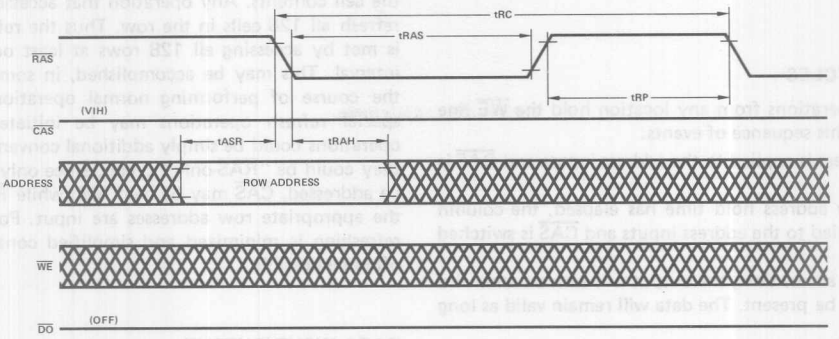
## READ-WRITE/READ-MODIFY-WRITE CYCLE




MOS-194

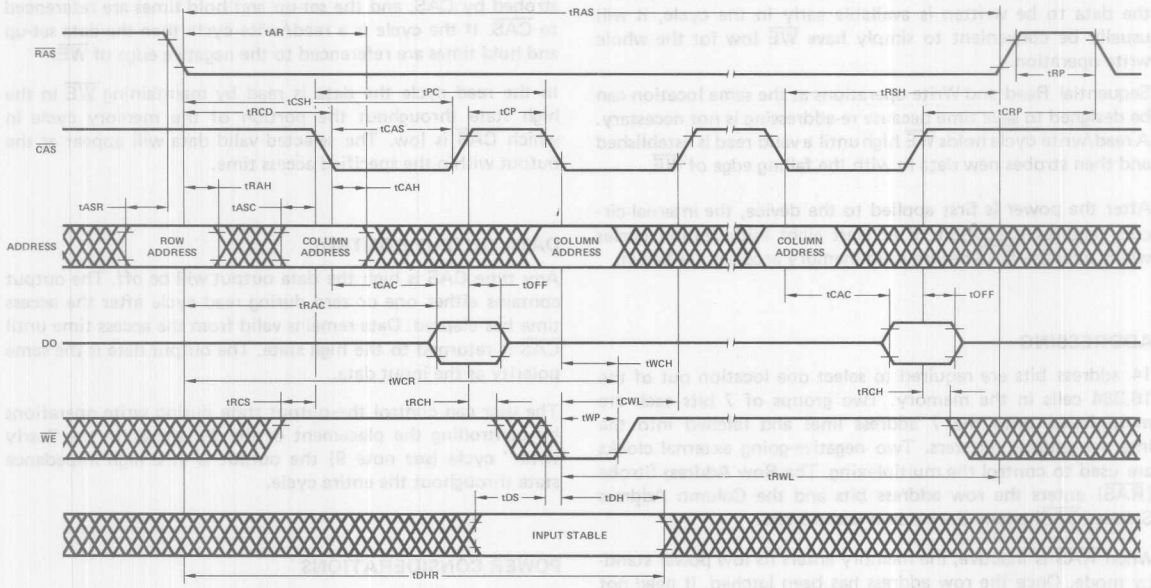
## SWITCHING WAVEFORMS (Cont.)

### $\overline{RAS}$ ONLY REFRESH CYCLE




MOS-195

### PAGE MODE CYCLE




MOS-196

## APPLICATION INFORMATION

The Am9016 electrical connections are such that if power is applied with the device installed upside down it will be permanently damaged. Precautions should be taken to avoid this mishap.

### OPERATING CYCLES

Random read operations from any location hold the $\overline{WE}$ line high and follow this sequence of events:

1) The row address is applied to the address inputs and $\overline{RAS}$ is switched low.
2) After the row address hold time has elapsed, the column address is applied to the address inputs and $\overline{CAS}$ is switched low.
3) Following the access time, the output will turn on and valid read data will be present. The data will remain valid as long as $\overline{CAS}$ is low.
4) $\overline{CAS}$ and $\overline{RAS}$ are then switched high to end the operation. A new cycle cannot begin until the precharge period has elapsed.

Random write operations follow the same sequence of events, except that the $\overline{WE}$ line is low for some portion of the cycle. If the data to be written is available early in the cycle, it will usually be convenient to simply have $\overline{WE}$ low for the whole write operation.

Sequential Read and Write operations at the same location can be designed to save time because re-addressing is not necessary. A read/write cycle holds $\overline{WE}$ high until a valid read is established and then strobes new data in with the falling edge of $\overline{WE}$.

After the power is first applied to the device, the internal circuit requires execution of at least eight initialization cycles which exercise $\overline{RAS}$ before valid memory accesses are begun.

### ADDRESSING

14 address bits are required to select one location out of the 16,384 cells in the memory. Two groups of 7 bits each are multiplexed onto the 7 address lines and latched into the internal address registers. Two negative-going external clocks are used to control the multiplexing. The Row Address Strobe ($\overline{RAS}$) enters the row address bits and the Column Address Strobe ($\overline{CAS}$) enters the column address bits.

When $\overline{RAS}$ is inactive, the memory enters its low power standby mode. Once the row address has been latched, it need not be changed for successive operations within the same row, allowing high-speed page-mode operations.

Page-mode operations first establish the row address and then maintain $\overline{RAS}$ low while $\overline{CAS}$ is repetitively cycled and designated operations are performed. Any column address within the selected row may be accessed in any sequence. The maximum time that $\overline{RAS}$ can remain low is the factor limiting the number of page-mode operations that can be performed.

Multiplexed addressing does not introduce extra delays in the access path. By inserting the row address first and the column address second, the memory takes advantage of the fact that the delay path through the memory is shorter for column addresses. The column address does not propagate through the cell matrix as the row address does and it can therefore arrive somewhat later than the row address without impacting the access time.

### REFRESH

The Am9016 is a dynamic memory and each cell must be refreshed at least once every refresh interval in order to maintain the cell contents. Any operation that accesses a row serves to refresh all 128 cells in the row. Thus the refresh requirement is met by accessing all 128 rows at least once every refresh interval. This may be accomplished, in some applications, in the course of performing normal operations. Alternatively, special refresh operations may be initiated. These special operations could be simply additional conventional accesses or they could be "$\overline{RAS}$-only" cycles. Since only the rows need to be addressed, $\overline{CAS}$ may be held high while $\overline{RAS}$ is cycled and the appropriate row addresses are input. Power required for refreshing is minimized and simplified control circuitry will often be possible.

### DATA INPUT/OUTPUT

Data is written into a selected cell by the combination of $\overline{WE}$ and $\overline{CAS}$ while $\overline{RAS}$ is low. The later negative transition of $\overline{WE}$ or $\overline{CAS}$ strobes the data into the internal register. In a write cycle, if the $\overline{WE}$ input is brought low prior to $\overline{CAS}$, the data is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the cycle is a read/write cycle then the data set-up and hold times are referenced to the negative edge of $\overline{WE}$.

In the read cycle the data is read by maintaining $\overline{WE}$ in the high state throughout the portion of the memory cycle in which $\overline{CAS}$ is low. The selected valid data will appear at the output within the specified access time.

### DATA OUTPUT CONTROL

Any time $\overline{CAS}$ is high the data output will be off. The output contains either one or zero during read cycle after the access time has elapsed. Data remains valid from the access time until $\overline{CAS}$ is returned to the high state. The output data is the same polarity as the input data.

The user can control the output state during write operations by controlling the placement of the $\overline{WE}$ signal. In the "early write" cycle (see note 9) the output is at a high impedance state throughout the entire cycle.

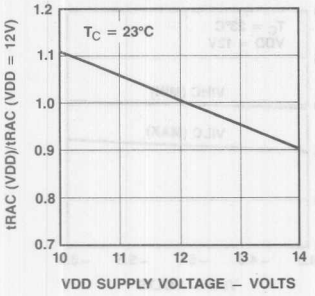
### POWER CONSIDERATIONS

$\overline{RAS}$ and/or $\overline{CAS}$ can be decoded and used as a chip select signal for the Am9016 but overall system power is minimized if $\overline{RAS}$ is used for this purpose. The devices which do not receive $\overline{RAS}$ will be in low power standby mode regardless of the state of $\overline{CAS}$.

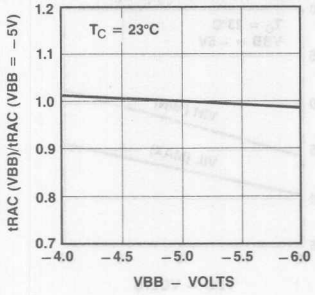
At all times the Absolute Maximum Rating Conditions must be observed. During power supply sequencing VBB should never be more positive than VSS when power is applied to VDD.

## TYPICAL CHARACTERISTICS

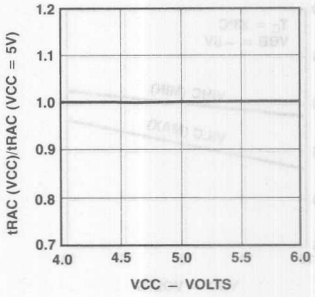
### Typical Access Time (Normalized) tRAC Versus VDD



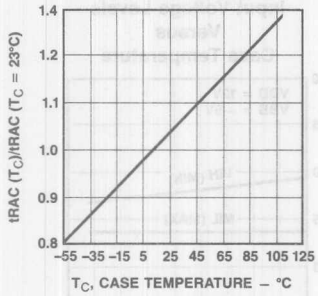

### Typical Access Time (Normalized) tRAC Versus VBB



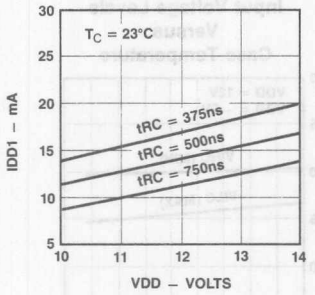

### Typical Access Time (Normalized) tRAC Versus VCC



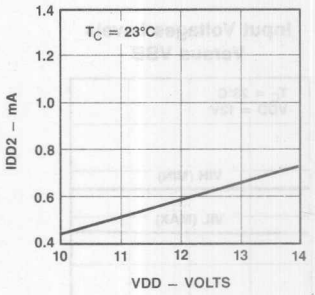

### Typical Access Time (Normalized) tRAC Versus Case Temperature



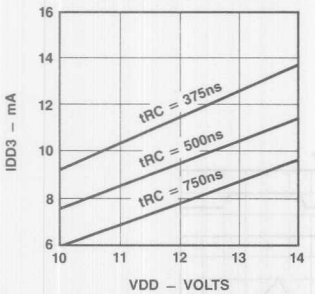

### Typical Operating Current IDD1 Versus VDD



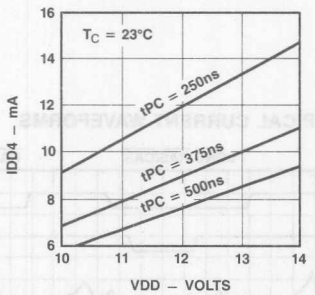

### Typical Standby Current IDD2 Versus VDD



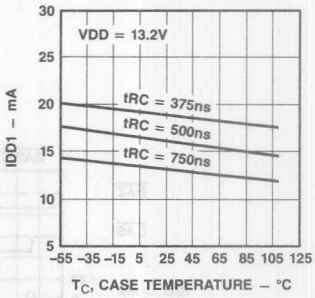

### Typical Refresh Current IDD3 Versus VDD



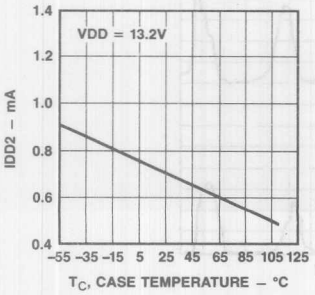

### Typical Page Mode Current IDD4 Versus VDD



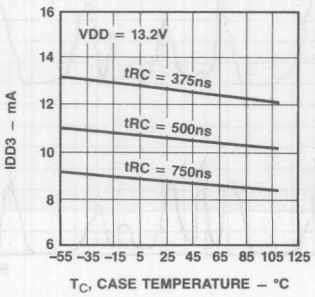

### Typical Operating Current IDD1 Versus Case Temperature



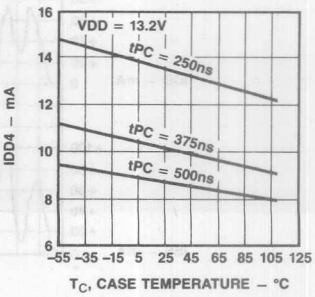

### Typical Standby Current IDD2 Versus Case Temperature




### Typical Refresh Current IDD3 Versus Case Temperature



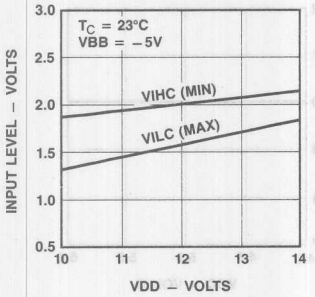

### Typical Page Mode Current IDD4 Versus Case Temperature



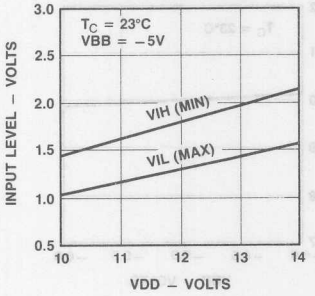

MOS-197

## TYPICAL CHARACTERISTICS (Cont.)

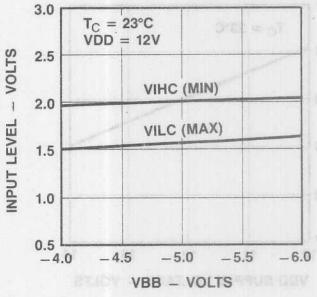
### Input Voltage Levels Versus VDD



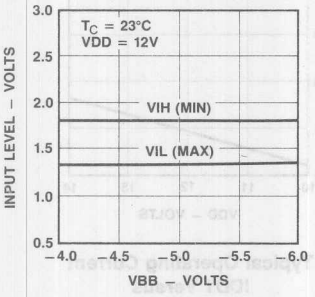

### Input Voltage Levels Versus VDD



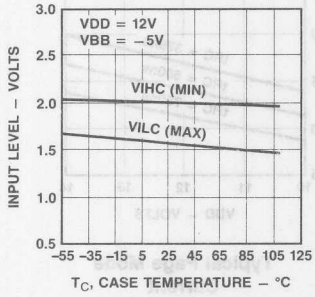

### Input Voltage Levels Versus VBB



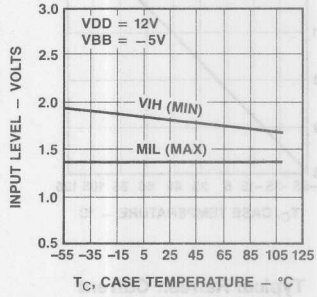

### Input Voltages Levels Versus VBB



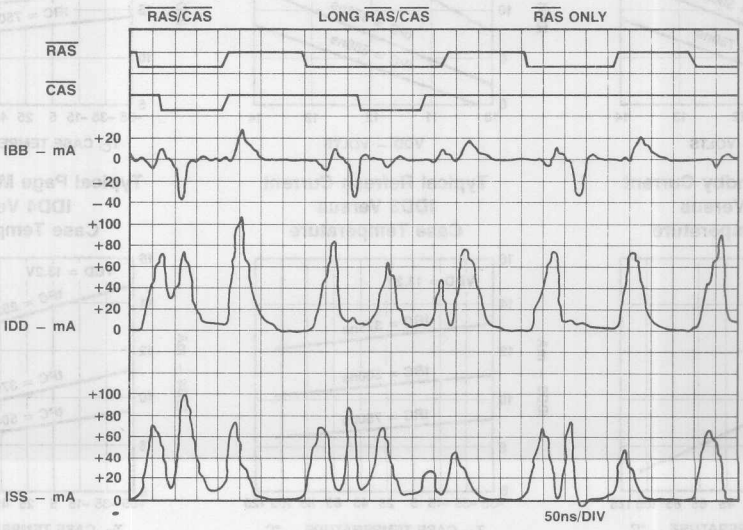

### Input Voltage Levels Versus Case Temperature



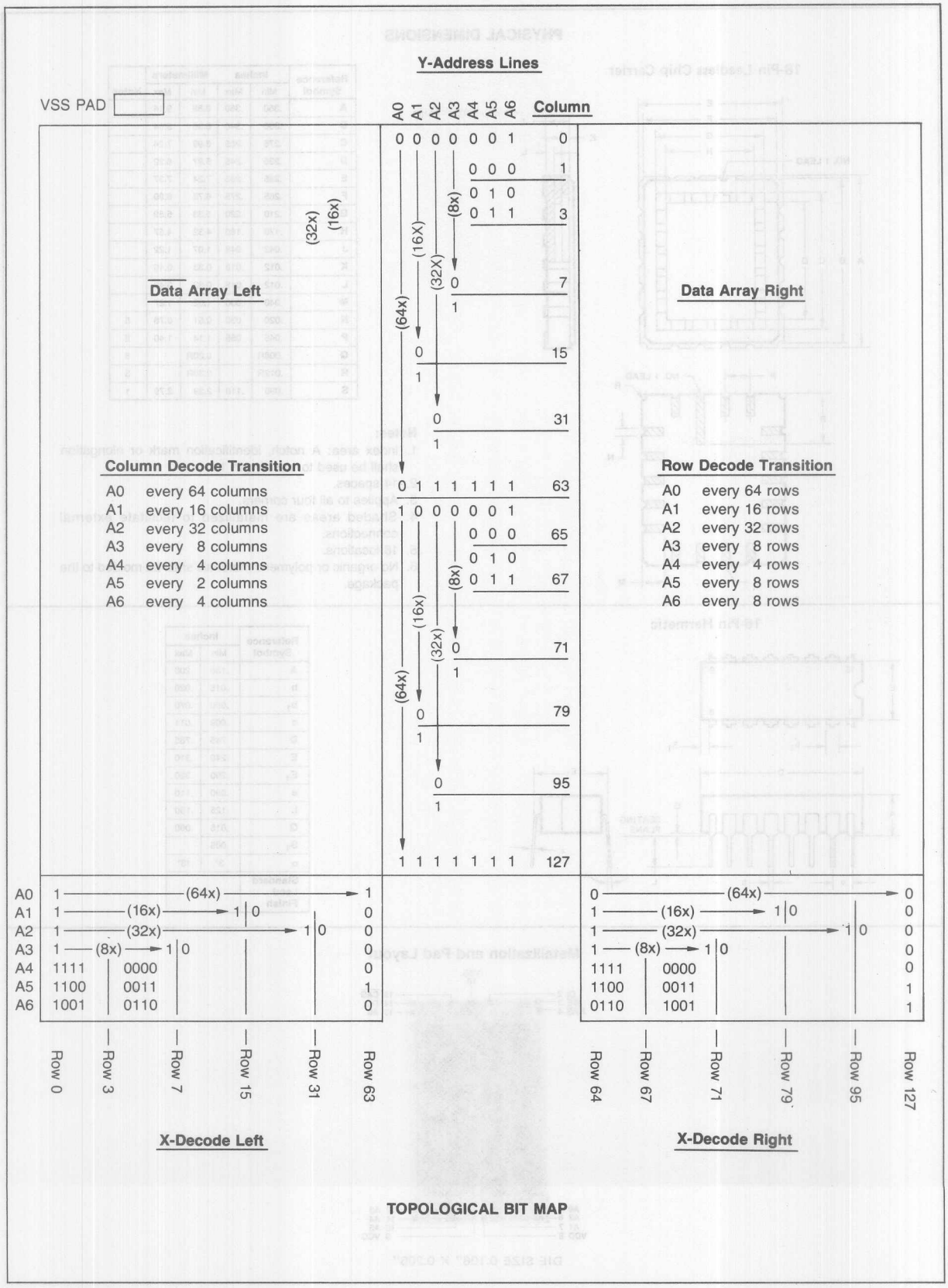

### Input Voltage Levels Versus Case Temperature




## TYPICAL CURRENT WAVEFORMS



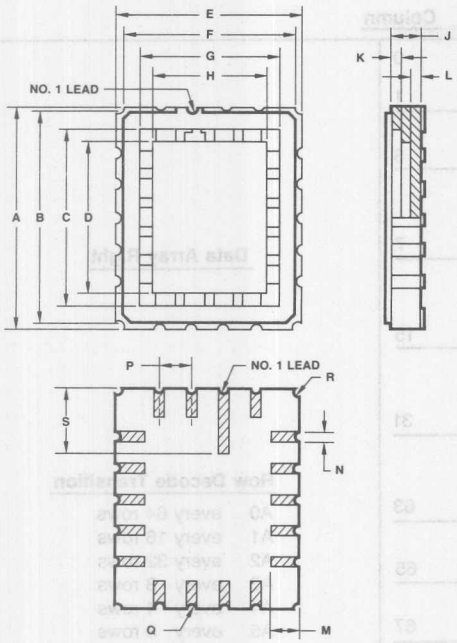

MOS-198




TOPOLOGICAL BIT MAP

## PHYSICAL DIMENSIONS

### 18-Pin Leadless Chip Carrier

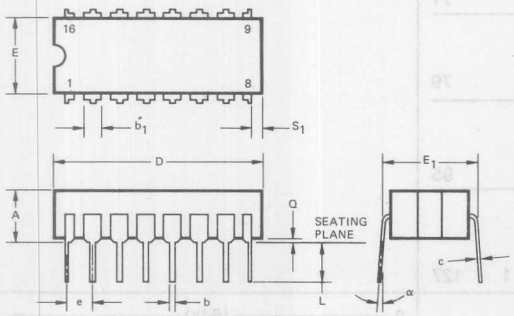



| Reference Symbol | Inches | | Millimeters | | Notes |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| A | .350 | .360 | 8.89 | 9.14 | |
| B | .330 | .340 | 8.38 | 8.64 | |
| C | .275 | .285 | 6.99 | 7.24 | |
| D | .235 | .245 | 5.97 | 6.22 | |
| E | .285 | .295 | 7.24 | 7.37 | |
| F | .265 | .275 | 6.73 | 6.99 | |
| G | .210 | .220 | 5.33 | 5.59 | |
| H | .170 | .180 | 4.32 | 4.57 | |
| J | .042 | .048 | 1.07 | 1.22 | |
| K | .012 | .018 | 0.33 | 0.46 | |
| L | .012 | .018 | 0.33 | 0.46 | |
| M | .040 | .050 | 1.02 | 1.27 | |
| N | .020 | .030 | 0.51 | 0.76 | 5 |
| P | .045 | .055 | 1.14 | 1.40 | 2 |
| Q | .008R | | 0.20R | | 5 |
| R | .012R | | 0.30R | | 3 |
| S | .090 | .110 | 2.29 | 2.79 | 1 |

**Notes:**

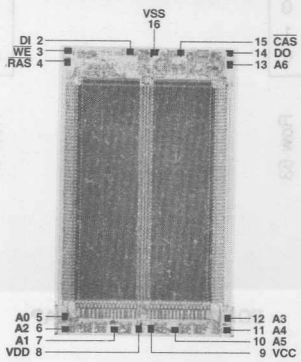
1. Index area: A notch, identification mark or elongation shall be used to identify pin 1.
2. 14 spaces.
3. Applies to all four corners.
4. Shaded areas are metallized to facilitate external connections.
5. 18 locations.
6. No organic or polymeric materials shall be molded to the package.

### 16-Pin Hermetic




| Reference Symbol | Inches | |
|---|---|---|
| | Min | Max |
| A | .130 | .200 |
| b | .016 | .020 |
| $b_1$ | .050 | .070 |
| c | .009 | .011 |
| D | .745 | .785 |
| E | .240 | .310 |
| $E_1$ | .290 | .320 |
| e | .090 | .110 |
| L | .125 | .150 |
| Q | .015 | .060 |
| $S_1$ | .005 | |
| α | 3° | 13° |
| Standard Lead Finish | b | |

### Metallization and Pad Layout




DIE SIZE 0.106" X 0.205"

# Am9016

## 16,384 x 1 Dynamic R/W Random Access Memory

2

### DISTINCTIVE CHARACTERISTICS

- High density 16k x 1 organization
- Direct replacement for MK4116
- Low maximum power dissipation — 462mW active, 20mW standby
- High speed operation — 150ns access, 320ns cycle
- ±10% tolerance on standard +12, +5, −5 voltages
- TTL compatible interface signals
- Three-state output
- RAS only, RMW and Page mode clocking options
- 128 cycle refreshing
- Unlatched data output
- Standard 16-pin, .3 inch wide dual in-line package
- Double poly N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

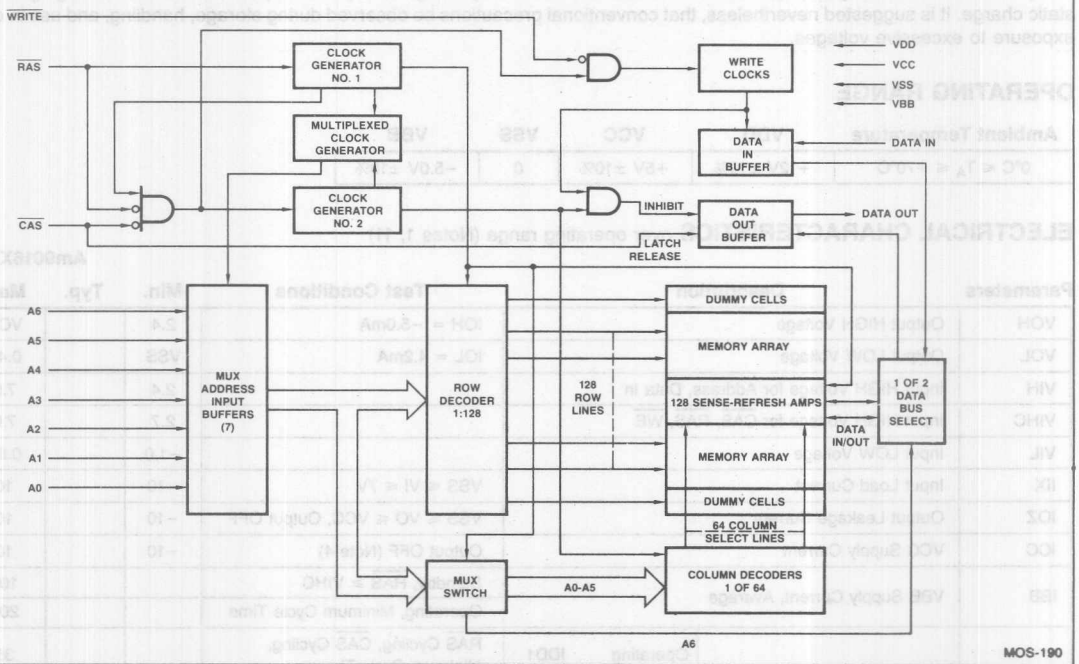
### GENERAL DESCRIPTION

The Am9016 is a high speed, 16k-bit, dynamic, read/write random access memory. It is organized as 16,384 words by 1 bit per word and is packaged in a standard 16-pin DIP. The basic memory element is a single transistor cell that stores charge on a small capacitor. This mechanism requires periodic refreshing of the memory cells to maintain stored information.

All input signals, including the two clocks, are TTL compatible. The Row Address Strobe ($\overline{RAS}$) loads the row address and the Column Address Strobe ($\overline{CAS}$) loads the column address. The row and column address signals share 7 input lines. Active cycles are initiated when $\overline{RAS}$ goes low, and standby mode is entered when $\overline{RAS}$ goes high. In addition to normal read and write cycles, other types of operations are available to improve versatility, performance, and power dissipation.

The three-state output buffer turns on when the column access time has elapsed and turns off after $\overline{CAS}$ goes high. Input and output data are the same polarity.

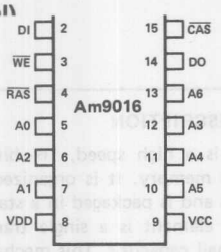
### BLOCK DIAGRAM




MOS-190

### ORDERING INFORMATION

| Ambient Temperature | Package Type | Access Time | | | |
|---|---|---|---|---|---|
| | | 300ns | 250ns | 200ns | 150ns |
| $0°C \leq T_A \leq +70°C$ | Hermetic DIP | AM9016CDC | AM9016DDC | AM9016EDC | AM9016FDC |
| | Molded DIP | AM9016CPC | AM9016DPC | AM9016EPC | AM9016FPC |




Top View
Pin 1 is marked for orientation.

| | |
|---|---|
| A0 – A6 | ADDRESS INPUTS |
| $\overline{CAS}$ | COLUMN ADDRESS STROBE |
| DI | DATA IN |
| DO | DATA OUT |
| $\overline{RAS}$ | ROW ADDRESS STROBE |
| VDD | POWER (+12V) |
| VCC | POWER (+5V) |
| VSS | GROUND |
| VBB | POWER (–5V) |
| $\overline{WE}$ | WRITE ENABLE |

MOS-191

## MAXIMUM RATINGS beyond which useful life may be impaired

| | |
|---|---|
| Storage Temperature | –65°C to +150°C |
| Ambient Temperature Under Bias | 0°C to +70°C |
| Voltage on Any Pin Relative to VBB | –0.5V to +20V |
| VDD and VCC Supply Voltages with Respect to VSS | –1.0V to +15.0V |
| VBB – VSS (VDD – VSS > 0V) | 0V |
| Power Dissipation | 1.0W |
| Short Circuit Output Current | 50mA |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulation of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling, and use in order to avoid exposure to excessive voltages.

## OPERATING RANGE

| Ambient Temperature | VDD | VCC | VSS | VBB |
|---|---|---|---|---|
| $0°C \leq T_A \leq +70°C$ | +12V ±10% | +5V ±10% | 0 | –5.0V ±10% |

## ELECTRICAL CHARACTERISTICS over operating range (Notes 1, 11)

| Parameters | Description | | Test Conditions | Am9016X Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| VOH | Output HIGH Voltage | | IOH = –5.0mA | 2.4 | | VCC | Volts |
| VOL | Output LOW Voltage | | IOL = 4.2mA | VSS | | 0.40 | Volts |
| VIH | Input HIGH Voltage for Address, Data In | | | 2.4 | | 7.0 | Volts |
| VIHC | Input HIGH Voltage for $\overline{CAS}$, $\overline{RAS}$, $\overline{WE}$ | | | 2.7 | | 7.0 | Volts |
| VIL | Input LOW Voltage | | | –1.0 | | 0.80 | Volts |
| IIX | Input Load Current | | VSS ≤ VI ≤ 7V | –10 | | 10 | µA |
| IOZ | Output Leakage Current | | VSS ≤ VO ≤ VCC, Output OFF | –10 | | 10 | µA |
| ICC | VCC Supply Current | | Output OFF (Note 4) | –10 | | 10 | µA |
| IBB | VBB Supply Current, Average | | Standby, $\overline{RAS} \geq$ VIHC | | | 100 | µA |
| | | | Operating, Minimum Cycle Time | | | 200 | |
| IDD | VDD Supply Current, Average | Operating IDD1 | $\overline{RAS}$ Cycling, $\overline{CAS}$ Cycling, Minimum Cycle Times | | | 35 | mA |
| | | Page Mode IDD4 | $\overline{RAS} \leq$ VIL, $\overline{CAS}$ Cycling, Minimum Cycle Times | | | 27 | |
| | | $\overline{RAS}$ Only Refresh IDD3 | $\overline{RAS}$ Cycling, $\overline{CAS} \geq$ VIHC, Minimum Cycle Times | | | 27 | |
| | | Standby IDD2 | $\overline{RAS} \geq$ VIHC | | | 1.5 | |
| CI | Input Capacitance | $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | Inputs at 0V, f = 1MHz, Nominal Supply Voltages | | | 10 | pF |
| | | Address, Data In | | | | 5.0 | |
| CO | Output Capacitance | | Output OFF | | | 7.0 | |

## SWITCHING CHARACTERISTICS over operating range (Notes 2, 3, 5, 10)

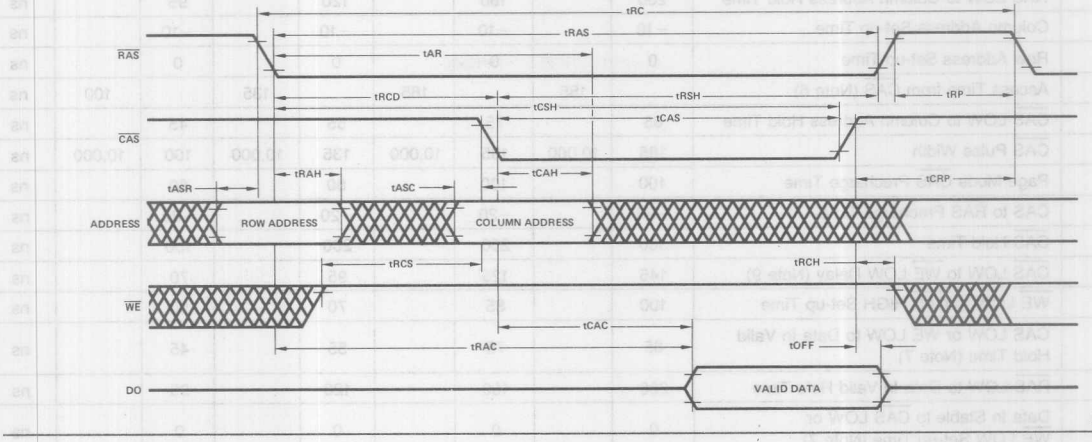
| Parameters | Description | Am9016C Min | Am9016C Max | Am9016D Min | Am9016D Max | Am9016E Min | Am9016E Max | Am9016F Min | Am9016F Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| tAR | $\overline{RAS}$ LOW to Column Address Hold Time | 200 | | 160 | | 120 | | 95 | | ns |
| tASC | Column Address Set-up Time | −10 | | −10 | | −10 | | −10 | | ns |
| tASR | Row Address Set-up Time | 0 | | 0 | | 0 | | 0 | | ns |
| tCAC | Access Time from $\overline{CAS}$ (Note 6) | | 185 | | 165 | | 135 | | 100 | ns |
| tCAH | $\overline{CAS}$ LOW to Column Address Hold Time | 85 | | 75 | | 55 | | 45 | | ns |
| tCAS | $\overline{CAS}$ Pulse Width | 185 | 10,000 | 165 | 10,000 | 135 | 10,000 | 100 | 10,000 | ns |
| tCP | Page Mode $\overline{CAS}$ Precharge Time | 100 | | 100 | | 80 | | 60 | | ns |
| tCRP | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | −20 | | −20 | | −20 | | −20 | | ns |
| tCSH | $\overline{CAS}$ Hold Time | 300 | | 250 | | 200 | | 150 | | ns |
| tCWD | $\overline{CAS}$ LOW to $\overline{WE}$ LOW Delay (Note 9) | 145 | | 125 | | 95 | | 70 | | ns |
| tCWL | $\overline{WE}$ LOW to $\overline{CAS}$ HIGH Set-up Time | 100 | | 85 | | 70 | | 50 | | ns |
| tDH | $\overline{CAS}$ LOW or $\overline{WE}$ LOW to Data In Valid Hold Time (Note 7) | 85 | | 75 | | 55 | | 45 | | ns |
| tDHR | $\overline{RAS}$ LOW to Data In Valid Hold Time | 200 | | 160 | | 120 | | 95 | | ns |
| tDS | Data In Stable to $\overline{CAS}$ LOW or $\overline{WE}$ LOW Set-up Time (Note 7) | 0 | | 0 | | 0 | | 0 | | ns |
| tOFF | $\overline{CAS}$ HIGH to Output OFF Delay | 0 | 60 | 0 | 60 | 0 | 50 | 0 | 40 | ns |
| tPC | Page Mode Cycle Time | 295 | | 275 | | 225 | | 170 | | ns |
| tRAC | Access Time from $\overline{RAS}$ (Note 6) | | 300 | | 250 | | 200 | | 150 | ns |
| tRAH | $\overline{RAS}$ LOW to Row Address Hold Time | 45 | | 35 | | 25 | | 20 | | ns |
| tRAS | $\overline{RAS}$ Pulse Width | 300 | 10,000 | 250 | 10,000 | 200 | 10,000 | 150 | 10,000 | ns |
| tRC | Random Read or Write Cycle Time | 460 | | 410 | | 375 | | 320 | | ns |
| tRCD | $\overline{RAS}$ LOW to $\overline{CAS}$ LOW Delay (Note 6) | 35 | 115 | 35 | 85 | 25 | 65 | 20 | 50 | ns |
| tRCH | Read Hold Time | 0 | | 0 | | 0 | | 0 | | ns |
| tRCS | Read Set-up Time | 0 | | 0 | | 0 | | 0 | | ns |
| tREF | Refresh Interval | | 2 | | 2 | | 2 | | 2 | ms |
| tRMW | Read Modify Write Cycle Time | 600 | | 500 | | 405 | | 320 | | ns |
| tRP | RAS Precharge Time | 150 | | 150 | | 120 | | 100 | | ns |
| tRSH | $\overline{CAS}$ LOW to $\overline{RAS}$ HIGH Delay | 185 | | 165 | | 135 | | 100 | | ns |
| tRWC | Read/Write Cycle Time | 525 | | 425 | | 375 | | 320 | | ns |
| tRWD | $\overline{RAS}$ LOW to $\overline{WE}$ LOW Delay (Note 9) | 260 | | 210 | | 160 | | 120 | | ns |
| tRWL | $\overline{WE}$ LOW to $\overline{RAS}$ HIGH Set-up Time | 100 | | 85 | | 70 | | 50 | | ns |
| tT | Transition Time | 3 | 50 | 3 | 50 | 3 | 50 | 3 | 35 | ns |
| tWCH | Write Hold Time | 85 | | 75 | | 55 | | 45 | | ns |
| tWCR | $\overline{RAS}$ LOW to Write Hold Time | 200 | | 160 | | 120 | | 95 | | ns |
| tWCS | $\overline{WE}$ LOW to $\overline{CAS}$ LOW Set-up Time (Note 9) | −20 | | −20 | | −20 | | −20 | | ns |
| tWP | Write Pulse Width | 85 | | 75 | | 55 | | 45 | | ns |

**NOTES**

1. Typical values are for $T_A$ = 25°C, nominal supply voltages and nominal processing parameters.
2. Signal transition times are assumed to be 5ns. Transition times are measured between specified high and low logic levels.
3. Timing reference levels for both input and output signals are the specified worst-case logic levels.
4. VCC is used in the output buffer only. ICC will therefore depend only on leakage current and output loading. When the output is ON and at a logic high level, VCC is connected to the Data Out pin through an equivalent resistance of approximately 135Ω. In standby mode VCC may be reduced to zero without affecting stored data or refresh operations.
5. Output loading is two standard TTL loads plus 100pF capacitance.
6. Both $\overline{RAS}$ and $\overline{CAS}$ must be low to read data. Access timing will depend on the relative positions of their falling edges. When tRCD is less than the maximum value shown, access time depends on $\overline{RAS}$ and tRAC governs. When tRCD is more than the maximum value shown access time depends on $\overline{CAS}$ and tCAC governs. The maximum value listed for tRCD is shown for reference purposes only and does not restrict operation of the part.
7. Timing reference points for data input set-up and hold times will depend on what type of write cycle is being performed and will be the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
8. At least eight initialization cycles that exercise $\overline{RAS}$ should be performed after power-up and before valid operations are begun.
9. The tWCS, tRWD and tCWD parameters are shown for reference purposes only and do not restrict the operating flexibility of the part. When the falling edge of $\overline{WE}$ follows the falling edge of $\overline{CAS}$ by at most tWCS, the data output buffer will remain off for the whole cycle and an "early write" cycle is defined. When the falling edge of $\overline{WE}$ follows the falling edges of $\overline{RAS}$ and $\overline{CAS}$ by at least tRWD and tCWD respectively, the Data Out from the addressed cell will be valid at the access time and a "read/write" cycle is defined. The falling edge of $\overline{WE}$ may also occur at intermediate positions, but the condition and validity of the Data Out signal will not be known.
10. Switching characteristics are listed in alphabetical order.
11. All voltages referenced to VSS.

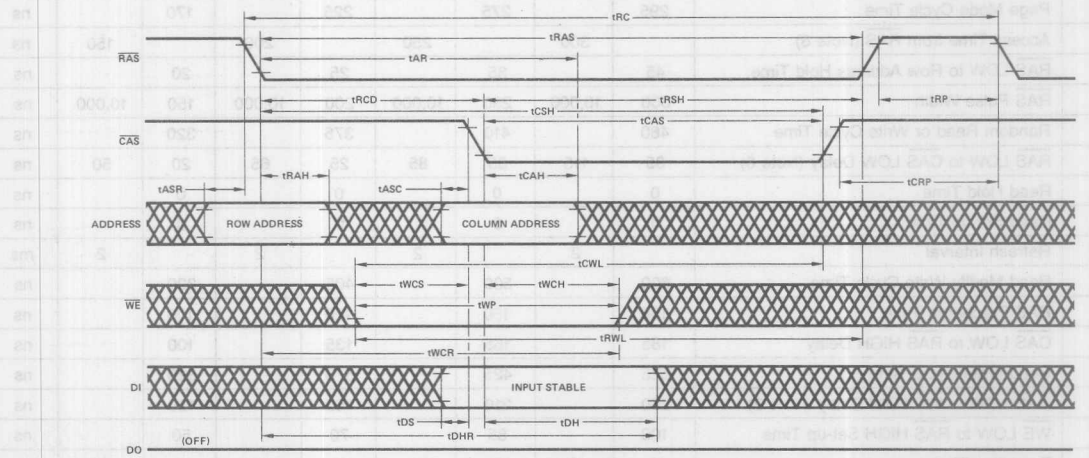
## SWITCHING WAVEFORMS

### READ CYCLE



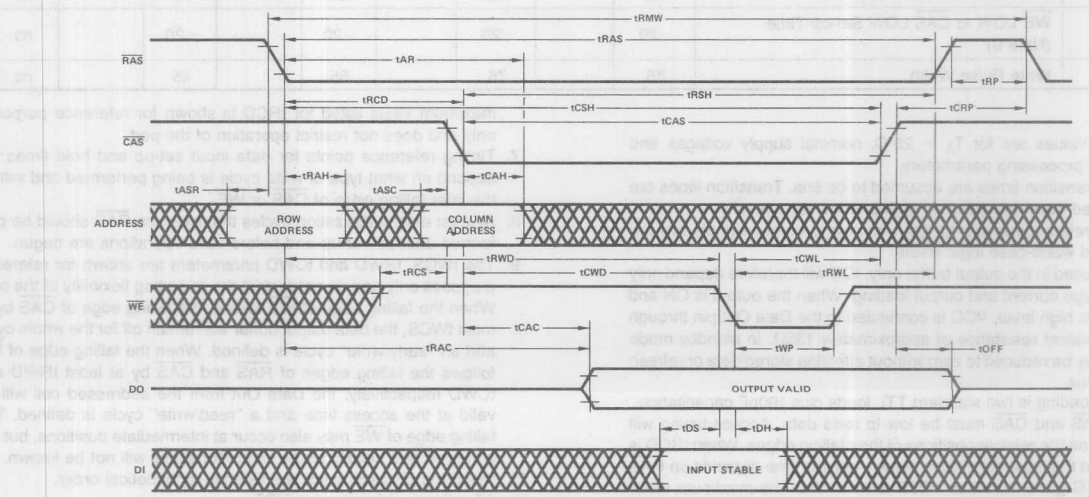

MOS-192

### WRITE CYCLE (EARLY WRITE)




MOS-193

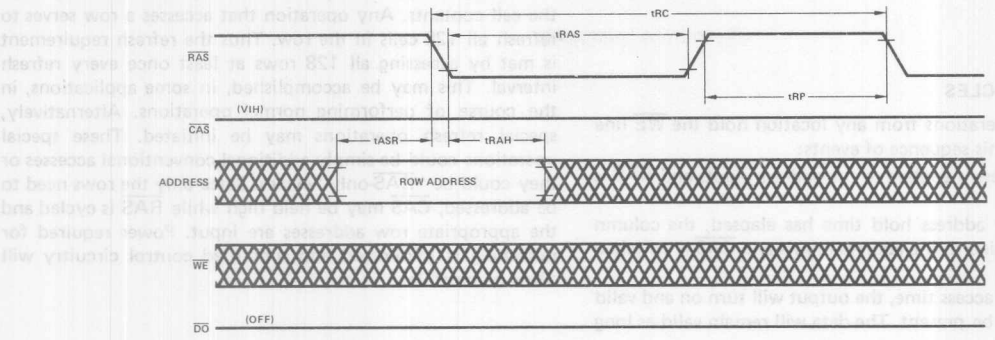
### READ-WRITE/READ-MODIFY-WRITE CYCLE




MOS-194

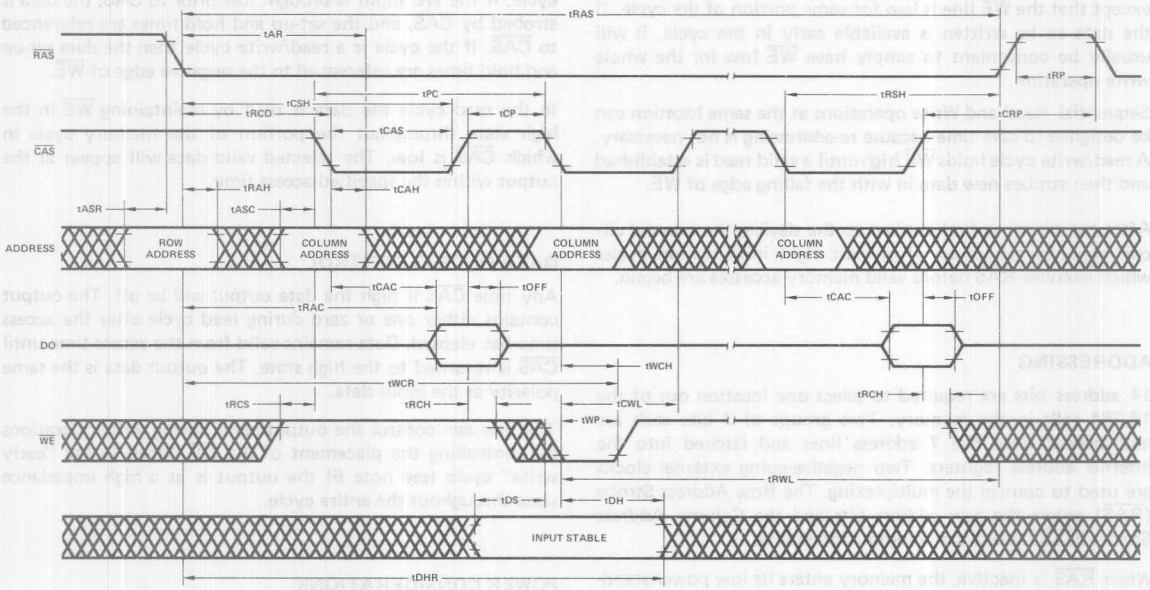
## SWITCHING WAVEFORMS (Cont.)

### $\overline{RAS}$ ONLY REFRESH CYCLE




MOS-195

### PAGE MODE CYCLE




MOS-196

applied with the device installed upside down it will be permanently damaged. Precautions should be taken to avoid this mishap.

## OPERATING CYCLES

Random read operations from any location hold the $\overline{WE}$ line high and follow this sequence of events:

1) The row address is applied to the address inputs and $\overline{RAS}$ is switched low.
2) After the row address hold time has elapsed, the column address is applied to the address inputs and $\overline{CAS}$ is switched low.
3) Following the access time, the output will turn on and valid read data will be present. The data will remain valid as long as $\overline{CAS}$ is low.
4) $\overline{CAS}$ and $\overline{RAS}$ are then switched high to end the operation. A new cycle cannot begin until the precharge period has elapsed.

Random write operations follow the same sequence of events, except that the $\overline{WE}$ line is low for some portion of the cycle. If the data to be written is available early in the cycle, it will usually be convenient to simply have $\overline{WE}$ low for the whole write operation.

Sequential Read and Write operations at the same location can be designed to save time because re-addressing is not necessary. A read/write cycle holds $\overline{WE}$ high until a valid read is established and then strobes new data in with the falling edge of $\overline{WE}$.

After the power is first applied to the device, the internal circuit requires execution of at least eight initialization cycles which exercise $\overline{RAS}$ before valid memory accesses are begun.

## ADDRESSING

14 address bits are required to select one location out of the 16,384 cells in the memory. Two groups of 7 bits each are multiplexed onto the 7 address lines and latched into the internal address registers. Two negative-going external clocks are used to control the multiplexing. The Row Address Strobe ($\overline{RAS}$) enters the row address bits and the Column Address Strobe ($\overline{CAS}$) enters the column address bits.

When $\overline{RAS}$ is inactive, the memory enters its low power standby mode. Once the row address has been latched, it need not be changed for successive operations within the same row, allowing high-speed page-mode operations.

Page-mode operations first establish the row address and then maintain $\overline{RAS}$ low while $\overline{CAS}$ is repetitively cycled and designated operations are performed. Any column address within the selected row may be accessed in any sequence. The maximum time that $\overline{RAS}$ can remain low is the factor limiting the number of page-mode operations that can be performed.

Multiplexed addressing does not introduce extra delays in the access path. By inserting the row address first and the column address second, the memory takes advantage of the fact that the delay path through the memory is shorter for column addresses. The column address does not propagate through the cell matrix as the row address does and it can therefore arrive somewhat later than the row address without impacting the access time.

The Am9016 is a dynamic memory and each cell must be refreshed at least once every refresh interval in order to maintain the cell contents. Any operation that accesses a row serves to refresh all 128 cells in the row. Thus the refresh requirement is met by accessing all 128 rows at least once every refresh interval. This may be accomplished, in some applications, in the course of performing normal operations. Alternatively, special refresh operations may be initiated. These special operations could be simply additional conventional accesses or they could be "$\overline{RAS}$-only" cycles. Since only the rows need to be addressed, $\overline{CAS}$ may be held high while $\overline{RAS}$ is cycled and the appropriate row addresses are input. Power required for refreshing is minimized and simplified control circuitry will often be possible.

## DATA INPUT/OUTPUT

Data is written into a selected cell by the combination of $\overline{WE}$ and $\overline{CAS}$ while $\overline{RAS}$ is low. The later negative transition of $\overline{WE}$ or $\overline{CAS}$ strobes the data into the internal register. In a write cycle, if the $\overline{WE}$ input is brought low prior to $\overline{CAS}$, the data is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the cycle is a read/write cycle then the data set-up and hold times are referenced to the negative edge of $\overline{WE}$.

In the read cycle the data is read by maintaining $\overline{WE}$ in the high state throughout the portion of the memory cycle in which $\overline{CAS}$ is low. The selected valid data will appear at the output within the specified access time.

## DATA OUTPUT CONTROL

Any time $\overline{CAS}$ is high the data output will be off. The output contains either one or zero during read cycle after the access time has elapsed. Data remains valid from the access time until $\overline{CAS}$ is returned to the high state. The output data is the same polarity as the input data.

The user can control the output state during write operations by controlling the placement of the $\overline{WE}$ signal. In the "early write" cycle (see note 9) the output is at a high impedance state throughout the entire cycle.

## POWER CONSIDERATIONS

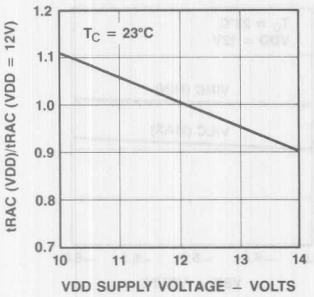
$\overline{RAS}$ and/or $\overline{CAS}$ can be decoded and used as a chip select signal for the Am9016 but overall system power is minimized if $\overline{RAS}$ is used for this purpose. The devices which do not receive $\overline{RAS}$ will be in low power standby mode regardless of the state of $\overline{CAS}$.

At all times the Absolute Maximum Rating Conditions must be observed. During power supply sequencing VBB should never be more positive than VSS when power is applied to VDD.

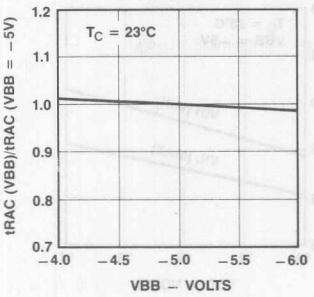
2

## TYPICAL CHARACTERISTICS

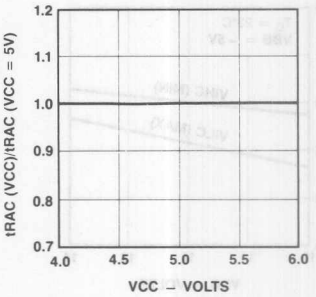
### Typical Access Time (Normalized) tRAC Versus VDD



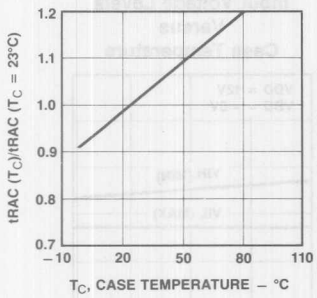

### Typical Access Time (Normalized) tRAC Versus VBB



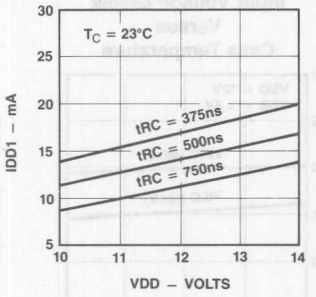

### Typical Access Time (Normalized) tRAC Versus VCC



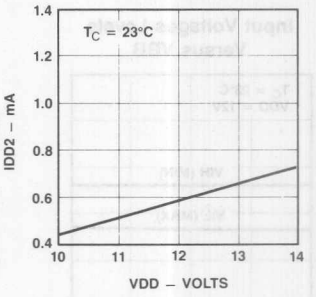

### Typical Access Time (Normalized) tRAC Versus Case Temperature



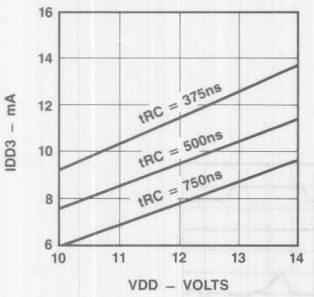

### Typical Operating Current IDD1 Versus VDD



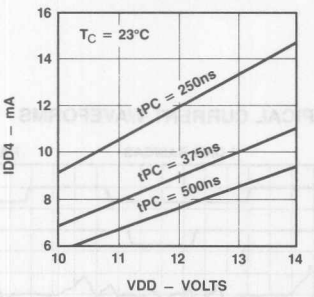

### Typical Standby Current IDD2 Versus VDD



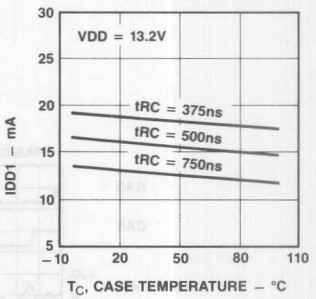

### Typical Refresh Current IDD3 Versus VDD



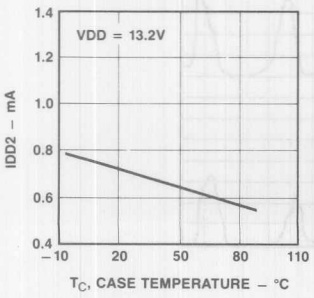

### Typical Page Mode Current IDD4 Versus VDD



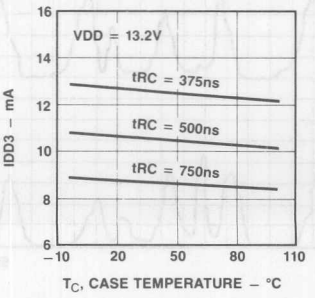

### Typical Operating Current IDD1 Versus Case Temperature



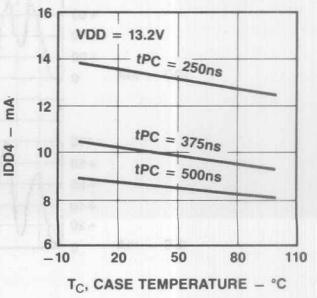

### Typical Standby Current IDD2 Versus Case Temperature




### Typical Refresh Current IDD3 Versus Case Temperature



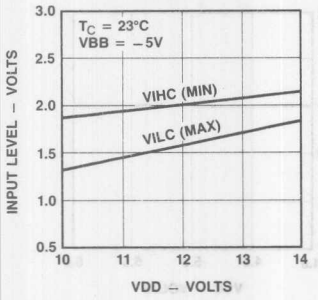

### Typical Page Mode Current IDD4 Versus Case Temperature



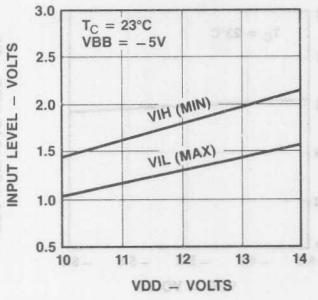

MOS-197

## TYPICAL CHARACTERISTICS (Cont.)

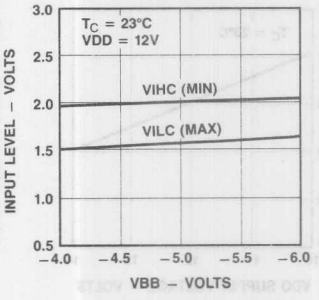
**Input Voltage Levels Versus VDD**



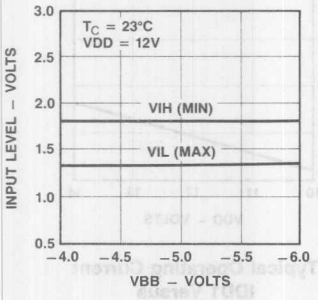

**Input Voltage Levels Versus VDD**



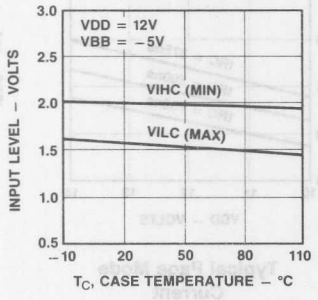

**Input Voltage Levels Versus VBB**



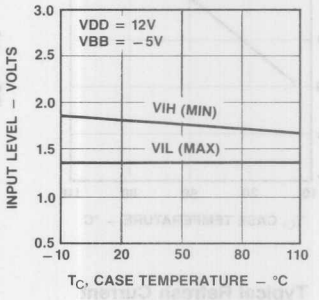

**Input Voltages Levels Versus VBB**




**Input Voltage Levels Versus Case Temperature**



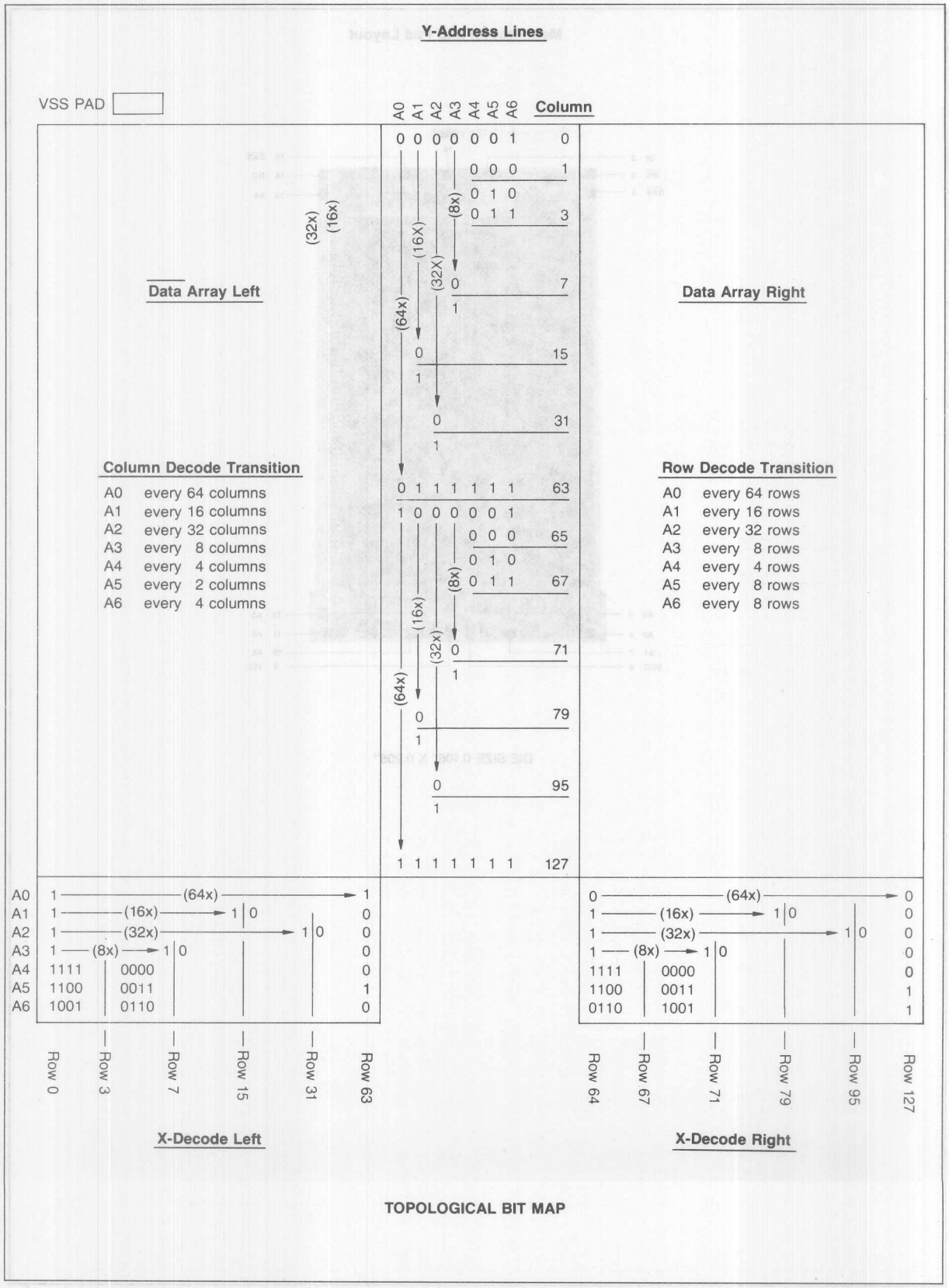

**Input Voltage Levels Versus Case Temperature**




## TYPICAL CURRENT WAVEFORMS

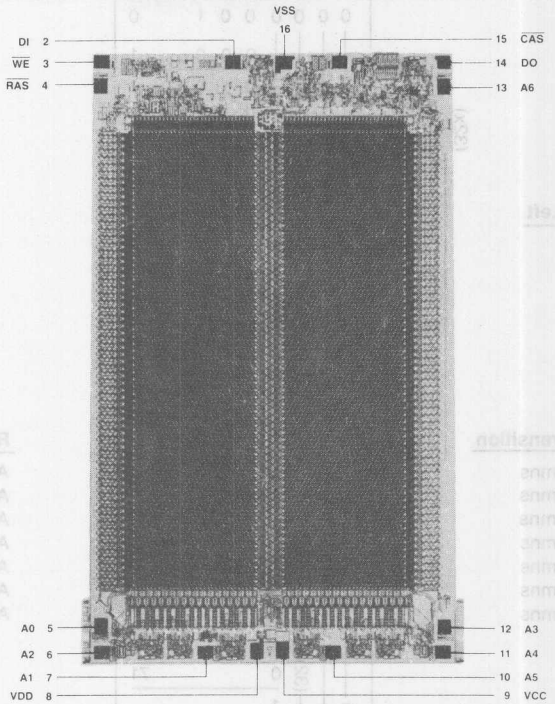



MOS-198




TOPOLOGICAL BIT MAP

## Metallization and Pad Layout




DIE SIZE 0.106" X 0.205"

# Am9044 • Am9244

## 4096 x 1 Static R/W Random Access Memory

2

### DISTINCTIVE CHARACTERISTICS

- **LOW OPERATING POWER (MAX)**
  **Am9044/Am9244 385mW (70mA)**
  **Am90L44/Am92L44 275mW (50mA)**
- **LOW STANDBY POWER (MAX)**
  **Am92L44 110mW (20mA)**
- Access times down to 200ns (max)
- Military temperature range available to 250ns (max)
- Am9044 is a direct plug-in replacement for 4044
- Am9244 pin and function compatible with Am9044 and 4044 plus $\overline{CS}$ power down feature
- Fully static – no clocking
- Identical access and cycle time
- High output drive – 4.0mA sink current @ 0.4V
- TTL identical interface logic levels
- 100% MIL-STD-883 reliability assurance testing

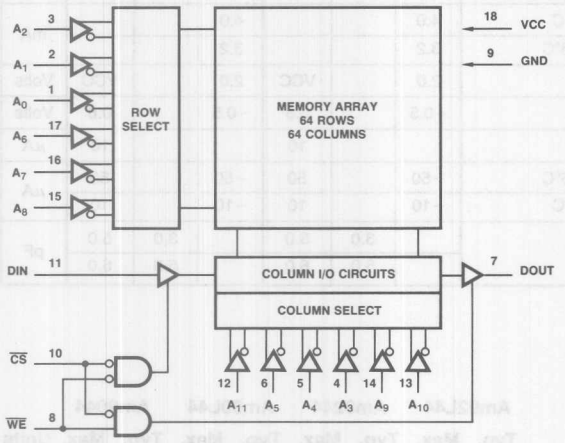
### GENERAL DESCRIPTION

The Am9044 and Am9244 are high performance, static, N-Channel, read/write, random access memories organized as 4096 x 1. Operation is from a single 5V supply, and all input/output levels are identical to standard TTL specifications. Low power versions of both devices are available with power savings of about 30%. The Am9044 and Am9244 are the same except that the Am9244 offers an automatic $\overline{CS}$ power down feature.

The Am9244 remains in a low power standby mode as long as $\overline{CS}$ remains high, thus reducing its power requirements. The Am9244 power decreases from 385mW to 165mW in the standby mode, and the Am92L44 from 275mW to 110mW. The $\overline{CS}$ input does not affect the power dissipation of the Am9044.

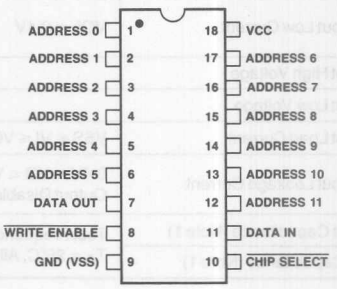
Data readout is not destructive and the same polarity as data input. $\overline{CS}$ provides for easy selection of an individual package when the outputs are OR-tied. The outputs of 4.0mA for Am9244 and Am9044 provide increased short circuit current for improved compacitive drive.

### BLOCK DIAGRAM




MOS-256

### CONNECTION DIAGRAM




Top View

Pin 1 is marked for orientation.

MOS-257

### ORDERING INFORMATION

| Ambient Temperature | Package Type | ICC Current Level | Access Times | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Am9044 | | | | Am9244 | | | |
| | | | 450ns | 300ns | 250ns | 200ns | 450ns | 300ns | 250ns | 200ns |
| 0°C ≤ $T_A$ ≤ +70°C | Plastic | 70mA | AM9044BPC | AM9044CPC | AM9044DPC | AM9044EPC | AM9244BPC | AM9244CPC | AM9244DPC | AM9244EPC |
| | | 50mA | AM90L44BPC | AM90L44CPC | AM90L44DPC | | AM92L44BPC | AM92L44CPC | AM92L44DPC | |
| | Hermetic | 70mA | AM9044BDC | AM9044CDC | AM9044DDC | AM9044EDC | AM9244BDC | AM9244CDC | AM9244DDC | AM9244EDC |
| | | 50mA | AM90L44BDC | AM90L44CDC | AM90L44DDC | | AM92L44BDC | AM92L44CDC | AM92L44DDC | |
| −55°C ≤ $T_A$ ≤ +125°C | Hermetic | 90mA | AM9044BDM | AM9044CDM | AM9044DDM | | AM9244BDM | AM9244CDM | AM9244DDM | |
| | | 60mA | AM90L44BDM | AM90L44CDM | | | AM92L44BDM | AM92L44CDM | | |

## MAXIMUM RATINGS beyond which useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| VCC with Respect to VSS | −0.5V to +7.0V |
| All Signal Voltages with Respect to VSS | −0.5V to +7.0V |
| Power Dissipation (Package Limitation) | 1.0W |
| DC Output Current | 10mA |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGE

| Part Number | Ambient Temperature | VSS | VCC | Part Number | Ambient Temperature | VSS | VCC |
|---|---|---|---|---|---|---|---|
| Am9044DC/PC<br>Am90L44DC/PC<br>Am9244DC/PC<br>Am92L44DC/PC | $0°C \leq T_A \leq +70°C$ | 0V | +5.0V ±10% | Am9044DM<br>Am90L44DM<br>Am9244DM<br>Am92L44DM | $-55°C \leq T_A \leq +125°C$ | 0V | +5.0V ±10% |

## ELECTRICAL CHARACTERISTICS over operating range

| Parameter | Description | Test Conditions | | | Am9244XX Am92L44XX Min. | Typ. | Max. | Am9044XX Am90L44XX Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| IOH | Output High Current | VOH = 2.4V | VCC = 4.5V | 70°C | −1.0 | | | −1.0 | | | mA |
| | | VOH = 2.4V | VCC = 4.5V | 125°C | −.4 | | | −.4 | | | |
| IOL | Output Low Current | VOL = 0.4V | | $T_A = +70°C$ | 4.0 | | | 4.0 | | | mA |
| | | | | $T_A = +125°C$ | 3.2 | | | 3.2 | | | |
| VIH | Input High Voltage | | | | 2.0 | | VCC | 2.0 | | VCC | Volts |
| VIL | Input Low Voltage | | | | −0.5 | | 0.8 | −0.5 | | 0.8 | Volts |
| IIX | Input Load Current | $VSS \leq VI \leq VCC$ | | | | | 10 | | | 10 | µA |
| IOZ | Output Leakage Current | $0.4V \leq VO \leq VCC$ Output Disabled | | $T_A = +125°C$ | −50 | | 50 | −50 | | 50 | µA |
| | | | | $T_A = +70°C$ | −10 | | 10 | −10 | | 10 | |
| CI | Input Capacitance (Note 1) | Test Frequency = 1.0MHz $T_A = 25°C$, All pins at 0V | | | | 3.0 | 5.0 | | 3.0 | 5.0 | pF |
| CI/O | I/O Capacitance (Note 1) | | | | | 5.0 | 6.0 | | 5.0 | 6.0 | |

## ELECTRICAL CHARACTERISTICS over operating range

| Parameter | Description | Test Conditions | | Am92L44 Typ. | Am92L44 Max. | Am9244 Typ. | Am9244 Max. | Am90L44 Typ. | Am90L44 Max. | Am9044 Typ. | Am9044 Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ICC | VCC Operating Supply Current | Max. VCC $\overline{CS} \leq$ VIL for Am9244/92L44 | $T_A = 0°C$ | | 50 | | 70 | | 50 | | 70 | mA |
| | | | $T_A = -55°C$ | | 60 | | 80 | | 60 | | 80 | |
| IPD | Automatic $\overline{CS}$ Power Down Current | Max. $V_{CC}$ ($\overline{CS} \geq V_{IH}$) | $T_A = 0°C$ | | 20 | | 30 | | – | | – | mA |
| | | | $T_A = -55°C$ | | 22 | | 33 | | – | | – | |

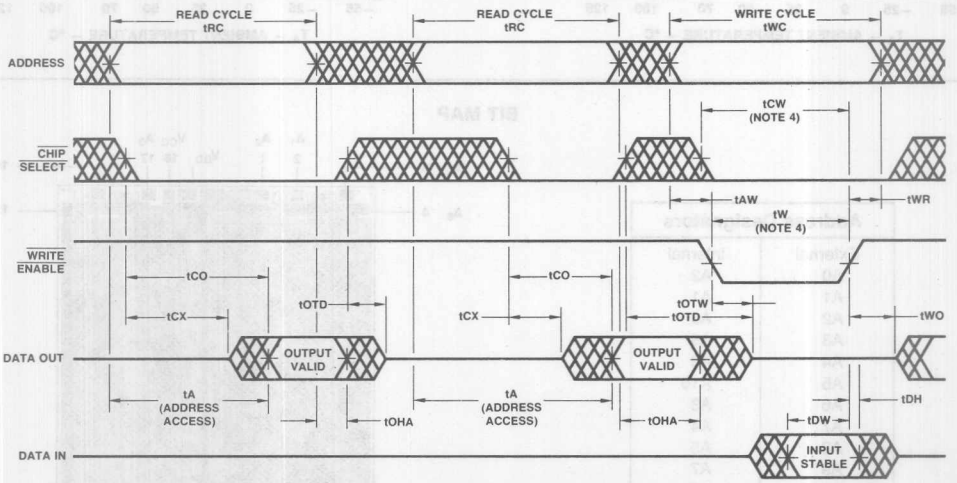
Notes:

1. Typical values are for $T_A$ = 25°C, nominal supply voltage and nominal processing parameters.
2. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
3. Test conditions assume signal transition times of 10ns or less, timing reference levels of 1.5V and output loading of one standard TTL gate plus 100pF.
4. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
5. Chip Select access time ($t_{CO}$) is longer for the Am9244 than for the Am9044. The specified address access time will be valid only when Chip Select is low soon enough for $t_{CO}$ to elapse.

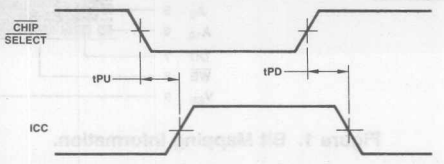
## SWITCHING CHARACTERISTICS over operating range (Note 3)

| Parameter | Description | | Am9044B Am9244B Min. | Am9044B Am9244B Max. | Am9044C Am9244C Min. | Am9044C Am9244C Max. | Am9044D Am9244D Min. | Am9044D Am9244D Max. | Am9044E Am9244E Min. | Am9044E Am9244E Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Read Cycle** | | | | | | | | | | | |
| tRC | Address Valid to Address Do Not Care Time (Read Cycle Time) | | 450 | | 300 | | 250 | | 200 | | ns |
| tA | Address Valid to Data Out Valid Delay (Address Access Time) | | | 450 | | 300 | | 250 | | 200 | ns |
| tCO | Chip Select Low to Data Out Valid (Note 5) | Am9044 | | 100 | | 100 | | 70 | | 70 | ns |
| | | Am9244 | | 450 | | 300 | | 250 | | 200 | ns |
| tCX | Chip Select Low to Data Out On | | 20 | | 20 | | 20 | | 20 | | ns |
| tOTD | Chip Select High to Data Out Off | | | 100 | | 80 | | 60 | | 60 | ns |
| tOHA | Address Unknown to Data Out Unknown Time | | 20 | | 20 | | 20 | | 20 | | ns |
| **Write Cycle** | | | | | | | | | | | |
| tWC | Address Valid to Address Do Not Care Time (Write Cycle Time) | | 450 | | 300 | | 250 | | 200 | | ns |
| tW | Write Enable Low to Write Enable High Time (Note 4) | Am9044 | 200 | | 150 | | 100 | | 100 | | ns |
| | | Am9244 | 250 | | 200 | | 150 | | 150 | | ns |
| tWR | Write Enable High to Address Do Not Care Time | | 0 | | 0 | | 0 | | 0 | | ns |
| tOTW | Write Enable Low to Data Out Off Delay | | | 100 | | 80 | | 60 | | 60 | ns |
| tDW | Data In Valid to Write Enable High Time | | 200 | | 150 | | 100 | | 100 | | ns |
| tDH | Write Enable Low to Data In Do Not Care Time | | 0 | | 0 | | 0 | | 0 | | ns |
| tAW | Address Valid to Write Enable Low Time | | 0 | | 0 | | 0 | | 0 | | ns |
| tPD | Chip Select High to Power Low Delay (Am9244 only) | | | 200 | | 150 | | 100 | | 100 | ns |
| tPU | Chip Select Low to Power High Delay (Am9244 only) | | 0 | | 0 | | 0 | | 0 | | ns |
| tCW | Chip Select Low to Write Enable High Time (Note 4) | Am9044 | 200 | | 150 | | 100 | | 100 | | ns |
| | | Am9244 | 250 | | 200 | | 150 | | 150 | | ns |
| tWO | Write Enable High To Output Turn On | | | 100 | | 100 | | 70 | | 70 | ns |

## SWITCHING WAVEFORMS



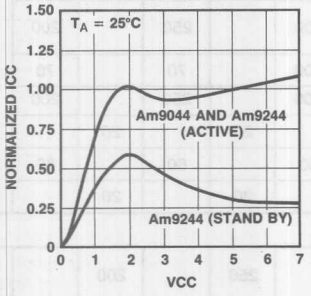

### POWER DOWN WAVEFORM (Am9244 ONLY)



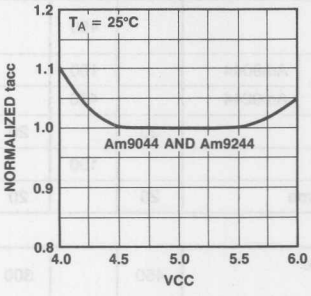

MOS-258

## TYPICAL CHARACTERISTICS

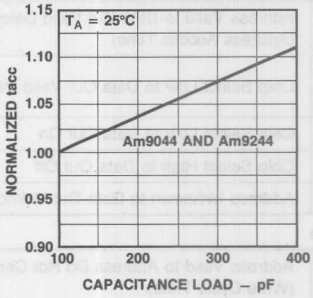
**Typical ICC Versus VCC Characteristics**



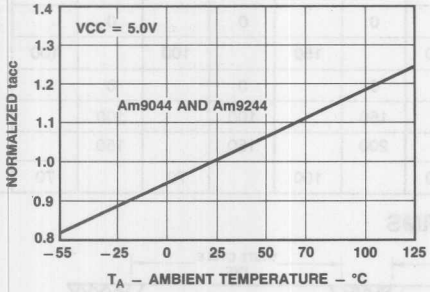

**Typical tacc Versus VCC Characteristics**



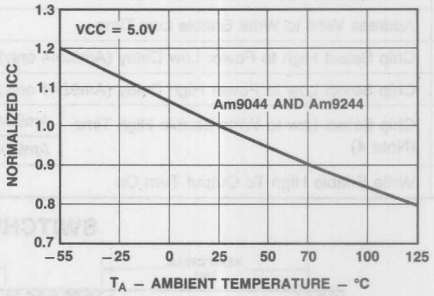

**Typical C Load Versus Normalized tacc Characteristics**




**Normalized tacc Versus Ambient Temperature**




**Normalized ICC Versus Ambient Temperature**




MOS-259

**BIT MAP**

| Address Designators | |
|---|---|
| External | Internal |
| A0 | A2 |
| A1 | A1 |
| A2 | A0 |
| A3 | A8 |
| A4 | A9 |
| A5 | A10 |
| A6 | A3 |
| A7 | A4 |
| A8 | A5 |
| A9 | A7 |
| A10 | A6 |
| A11 | A11 |

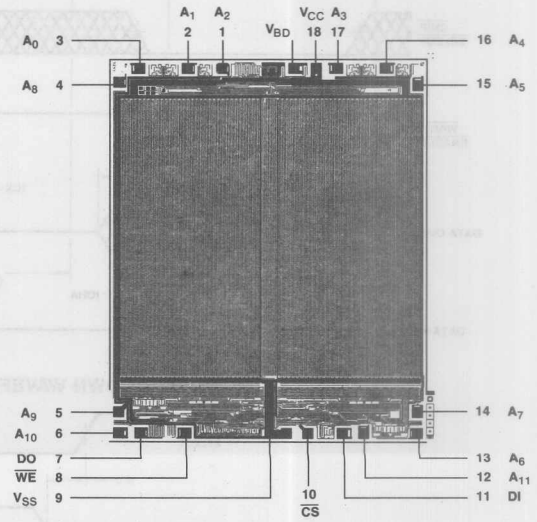



**Figure 1. Bit Mapping Information.**

# Am9101/Am91L01/Am2101 FAMILY

## 256x4 Static R/W Random Access Memories



| PART NUMBER | Am2101 | Am2101-2 | Am9101A<br>Am91L01A<br>Am2101-1 | Am9101B<br>Am91L01B | Am9101C<br>Am91L01C | Am9101D |
|---|---|---|---|---|---|---|
| ACCESS TIME | 1000ns | 650ns | 500ns | 400ns | 300ns | 250ns |

### DISTINCTIVE CHARACTERISTICS

- 256 x 4 organization
- Low operating power
  - 125mW Typ; 290mW maximum — standard power
  - 100mW Typ; 175mW maximum — low power
- DC standby mode reduces power up to 84%
- Logic voltage levels identical to TTL
- High output drive — two full TTL loads
- High noise immunity — full 400mV
- Single 5 volt power supply — tolerances: ±5% commercial, ±10% military
- Uniform switching characteristics — access times insensitive to supply variations, addressing patterns and data patterns
- Both military and commercial temperature ranges available
- Two chip enable inputs
- Output disable control
- Zero address set-up and hold times for simplified timing
- 100% MIL-STD-883 reliability assurance testing

### FUNCTIONAL DESCRIPTION

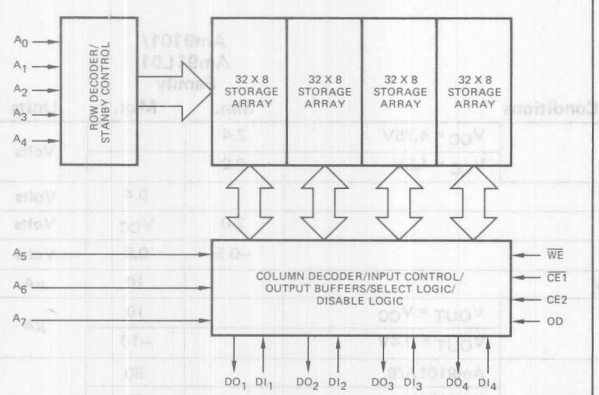
The Am9101/Am91L01 series of devices are high-performance, low-power, 1024-bit, static, read/write random access memories. They offer a wide range of access times including versions as fast as 200ns. Each memory is implemented as 256 words by 4 bits per word. This organization permits efficient design of small memory systems and allows finer resolution of incremental memory depth.

These memories may be operated in a DC standby mode for reductions of as much as 84 percent of the normal power dissipation. Data can be retained with a power supply as low as 1.5 volts. The low power Am91L01 series offer reduced power dissipation during normal operating conditions and even lower dissipation in the stand-by mode.

The Chip Enable input control signals act as high order address lines and they control the write amplifier and the output buffers. The Output Disable signal provides independent control over the output state of enabled chips.

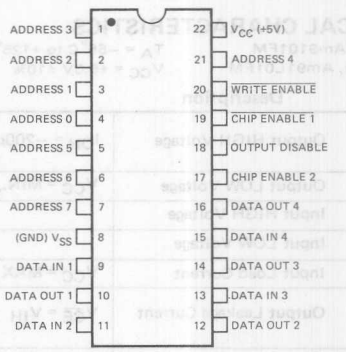
These devices are all fully static and no refresh operations or sense amplifiers or clocks are required. Input and output signal levels are identical to TTL specifications, providing simplified interfacing and high noise immunity. The outputs will drive two full TTL loads for increased fan-out and better bus interfacing capability.

### Am9101 BLOCK DIAGRAM




MOS-343

### CONNECTION DIAGRAM
Top View




Note: Flat Pack version available in 24-pin package.

MOS-344

### ORDERING INFORMATION

| Ambient Temperature Specification | Package Type | Power Type | Access Times | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | 1000ns | 650ns | 500ns | 400ns | 300ns | 250ns |
| 0°C to +70°C | Molded DIP | Standard | P2101 | P2101-2 | P2101-1<br>AM9101APC | AM9101BPC | AM9101CPC | AM9101DPC |
| | | Low | | | AM91L01APC | AM91L01BCP | AM91L01CPC | |
| | Hermetic DIP | Standard | C2101 | C2101-2 | C2101-1<br>AM9101ADC | AM9101BDC | AM9101CDC | AM9101DDC |
| | | Low | | | AM91L01ADC | AM91L01BDC | AM91L01CDC | |
| −55°C to +125°C | Hermetic DIP | Standard | | | AM9101ADM | AM9101BDM | AM9101CDM | |
| | | Low | | | AM91L01ADM | AM91L01BDM | AM91L01CDM | |
| | Hermetic Flat Pack | Standard | | | AM9101AFM | AM9101BFM | | |
| | | Low | | | AM91L01AFM | AM91L01BFM | | |

## MAXIMUM RATINGS above which the useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| $V_{CC}$ With Respect to $V_{SS}$, Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs | −0.5V to +7.0V |
| DC Input Voltage | −0.5V to +7.0V |
| Power Dissipation | 1.0W |

## ELECTRICAL CHARACTERISTICS

Am9101PC, Am9101DC
Am91L01PC, Am91L01DC
Am2101

$T_A$ = 0°C to +70°C
$V_{CC}$ = +5.0V ±5%

| Parameters | Description | Test Conditions | | | Am9101/Am91L01 Family Min. | Am9101/Am91L01 Family Max. | Am2101 Family Min. | Am2101 Family Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN. | | $I_{OH}$ = −200μA | 2.4 | | | | Volts |
| | | | | $I_{OH}$ = −150μA | | | 2.2 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN. | | $I_{OL}$ = 3.2mA | | 0.4 | | | Volts |
| | | | | $I_{OL}$ = 2.0mA | | | | 0.45 | |
| $V_{IH}$ | Input HIGH Voltage | | | | 2.0 | $V_{CC}$ | 2.2 | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Voltage | | | | −0.5 | 0.8 | −0.5 | 0.65 | Volts |
| $I_{LI}$ | Input Load Current | $V_{CC}$ = MAX., 0V ≤ $V_{IN}$ ≤ 5.25V | | | | 10 | | 10 | μA |
| $I_{LO}$ | Output Leakage Current | $V_{\overline{CE}} = V_{IH}$ | | $V_{OUT} = V_{CC}$ | | 5.0 | | 15 | μA |
| | | | | $V_{OUT}$ = 0.4V | | −10 | | −50 | |
| $I_{CC1}$ | Power Supply Current | Data out open $V_{CC}$ = Max. $V_{IN} = V_{CC}$ | $T_A$ = 25°C | Am9101A/B | | 50 | | 60 | mA |
| | | | | Am9101C/D/E | | 55 | | | |
| | | | | Am91L01A/B | | 31 | | | |
| | | | | Am91L01C | | 34 | | | |
| $I_{CC2}$ | | | $T_A$ = 0°C | Am9101A/B | | 55 | | 70 | |
| | | | | Am9101C/D/E | | 60 | | | |
| | | | | Am91L01A/B | | 33 | | | |
| | | | | Am91L01C | | 36 | | | |

## ELECTRICAL CHARACTERISTICS

Am9101DM, Am9101FM
Am91L01DM, Am91L01FM

$T_A$ = −55°C to +125°C
$V_{CC}$ = +5.0V ±10%

| Parameters | Description | Test Conditions | | | Am9101/Am91L01 Family Min. | Am9101/Am91L01 Family Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −200μA | | $V_{CC}$ = 4.75V | 2.4 | | Volts |
| | | | | $V_{CC}$ = 4.5V | 2.2 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 3.2mA | | | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | | | 2.0 | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Voltage | | | | −0.5 | 0.8 | Volts |
| $I_{LI}$ | Input Load Current | $V_{CC}$ = MAX., 0V ≤ $V_{IN}$ ≤ 5.5V | | | | 10 | μA |
| $I_{LO}$ | Output Leakage Current | $V_{\overline{CE}} = V_{IH}$ | | $V_{OUT} = V_{CC}$ | | 10 | μA |
| | | | | $V_{OUT}$ = 0.4V | | −10 | |
| $I_{CC1}$ | Power Supply Current | Data out open $V_{CC}$ = Max. $V_{IN} = V_{CC}$ | $T_A$ = 25°C | Am9101A/B | | 50 | mA |
| | | | | Am9101C | | 55 | |
| | | | | Am91L01A/B | | 31 | |
| | | | | Am91L01C | | 34 | |
| $I_{CC3}$ | | | $T_A$ = −55°C | Am9101A/B | | 60 | |
| | | | | Am9101C | | 65 | |
| | | | | Am91L01A/B | | 37 | |
| | | | | Am91L01C | | 40 | |

## CAPACITANCE

| Parameters | Description | Test Conditions | | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance, $V_{IN}$ = 0V | $T_A$ = 25°C, f = 1MHz | Am2101 | 4.0 | 8.0 | pF |
| | | | Am9101/Am91L01 | 3.0 | 6.0 | |
| $C_{OUT}$ | Output Capacitance, $V_{OUT}$ = 0V | | Am2101 | 8.0 | 12 | pF |
| | | | Am9101/Am91L01 | 6.0 | 9.0 | |

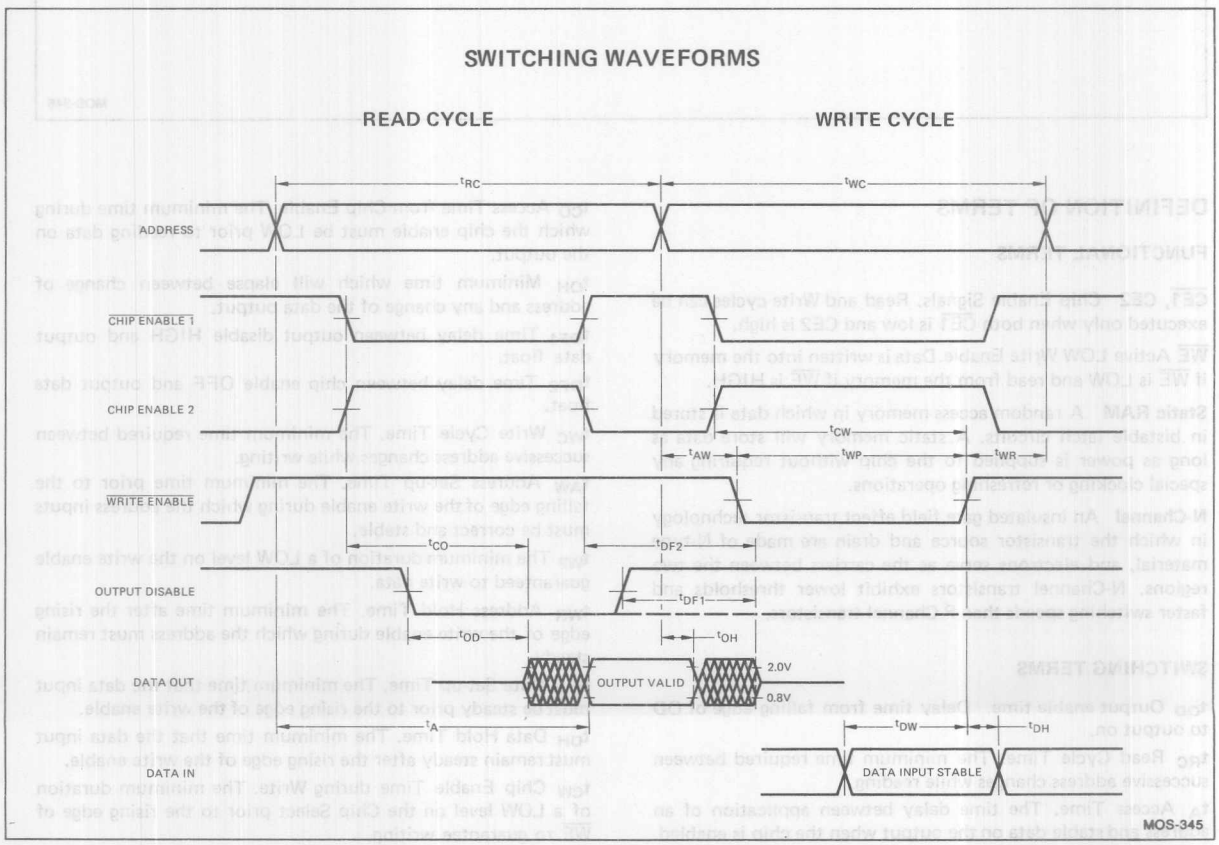
## SWITCHING CHARACTERISTICS over operating temperature and voltage range

Output Load = 1 TTL Gate + 100pF — $T_A$ = 0 to 70°C — $V_{CC}$ = +5V ±5%
Transition Times = 10ns — $T_A$ = −55 to +125°C — $V_{CC}$ = +5V ±10%
Input Levels, Output References = 0.8V and 2.0V

| Parameters | Description | 2101 | | 2101-2 | | 2101-1 | | 9101A 91L01A | | 9101B 91L01B | | 9101C 91L01C | | 9101D | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{RC}$ | Read Cycle Time | 1000 | | 650 | | 500 | | 500 | | 400 | | 300 | | 250 | | ns |
| $t_A$ | Access Time | | 1000 | | 650 | | 500 | | 500 | | 400 | | 300 | | 250 | ns |
| $t_{CO}$ | Chip Enable to Output ON Delay (Note 1) | | 800 | | 400 | | 350 | | 200 | | 175 | | 150 | | 125 | ns |
| $t_{OD}$ | Output Disable to Output ON Delay | | 700 | | 350 | | 300 | | 175 | | 150 | | 125 | | 100 | ns |
| $t_{OH}$ | Previous Read Data Valid with Respect to Address Change | 0 | | 0 | | 0 | | 40 | | 40 | | 40 | | 30 | | ns |
| $t_{DF1}$ | Output Disable to Output OFF Delay | 0 | 200 | 0 | 150 | 0 | 150 | 5.0 | 125 | 5.0 | 100 | 5.0 | 100 | 5.0 | 75 | ns |
| $t_{DF2}$ | Chip Enable to Output OFF Delay | 0 | 200 | 0 | 150 | 0 | 150 | 10 | 125 | 10 | 125 | 10 | 100 | 10 | 100 | ns |
| $t_{WC}$ | Write Cycle Time | 1000 | | 650 | | 500 | | 500 | | 400 | | 300 | | 250 | | ns |
| $t_{AW}$ | Address Set-up Time | 150 | | 150 | | 100 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{WP}$ | Write Pulse Width | 750 | | 400 | | 300 | | 175 | | 150 | | 125 | | 100 | | ns |
| $t_{CW}$ | Chip Enable Set-up Time (Note 1) | 900 | | 550 | | 400 | | 175 | | 150 | | 125 | | 100 | | ns |
| $t_{WR}$ | Address Hold Time | 50 | | 50 | | 50 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{DW}$ | Input Data Set-up Time | 700 | | 400 | | 280 | | 150 | | 125 | | 100 | | 85 | | ns |
| $t_{DH}$ | Input Data Hold Time | 100 | | 100 | | 100 | | 0 | | 0 | | 0 | | 0 | | ns |

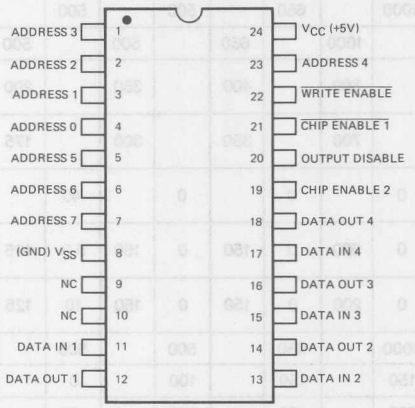
Note: 1. Both $\overline{CE1}$ and CE2 must be true to enable the chip.

### SWITCHING WAVEFORMS



## CONNECTION DIAGRAM
Top View

Flat Package




Pin 1 is marked for orientation.

MOS-346

## DEFINITION OF TERMS

### FUNCTIONAL TERMS

**$\overline{CE1}$, CE2** Chip Enable Signals. Read and Write cycles can be executed only when both $\overline{CE1}$ is low and CE2 is high.

**$\overline{WE}$** Active LOW Write Enable. Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if $\overline{WE}$ is HIGH.

**Static RAM** A random access memory in which data is stored in bistable latch circuits. A static memory will store data as long as power is supplied to the chip without requiring any special clocking or refreshing operations.

**N-Channel** An insulated gate field effect transistor technology in which the transistor source and drain are made of N-type material, and electrons serve as the carriers between the two regions. N-Channel transistors exhibit lower thresholds and faster switching speeds than P-Channel transistors.

### SWITCHING TERMS

**$t_{OD}$** Output enable time. Delay time from falling edge of OD to output on.

**$t_{RC}$** Read Cycle Time. The minimum time required between successive address changes while reading.

**$t_A$** Access Time. The time delay between application of an address and stable data on the output when the chip is enabled.

**$t_{CO}$** Access Time from Chip Enable. The minimum time during which the chip enable must be LOW prior to reading data on the output.

**$t_{OH}$** Minimum time which will elapse between change of address and any change of the data output.

**$t_{DF1}$** Time delay between output disable HIGH and output data float.

**$t_{DF2}$** Time delay between chip enable OFF and output data float.

**$t_{WC}$** Write Cycle Time. The minimum time required between successive address changes while writing.

**$t_{AW}$** Address Set-up Time. The minimum time prior to the falling edge of the write enable during which the address inputs must be correct and stable.

**$t_{WP}$** The minimum duration of a LOW level on the write enable guaranteed to write data.

**$t_{WR}$** Address Hold Time. The minimum time after the rising edge of the write enable during which the address must remain steady.

**$t_{DW}$** Data Set-up Time. The minimum time that the data input must be steady prior to the rising edge of the write enable.

**$t_{DH}$** Data Hold Time. The minimum time that the data input must remain steady after the rising edge of the write enable.

**$t_{CW}$** Chip Enable Time during Write. The minimum duration of a LOW level on the Chip Select prior to the rising edge of $\overline{WE}$ to guarantee writing.

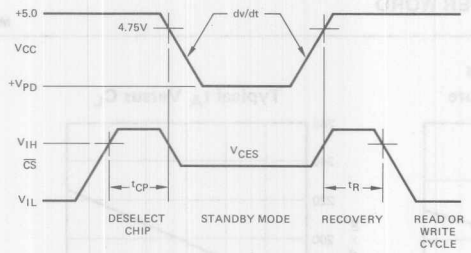
## POWER DOWN STANDBY OPERATION

The Am9101/Am91L01 Family is designed to maintain storage in a standby mode. The standby mode is entered by lowering $V_{CC}$ to around 1.5–2.0 volts (see table and graph below). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated backup power supply system, or, in a large system, memory pages not being accessed can be placed in standby to save power. A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

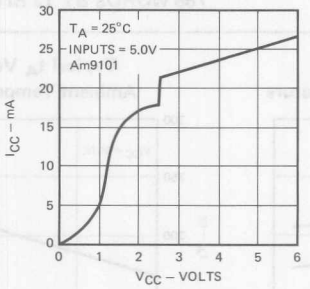
To ensure that the output of the device is in a high impedance OFF state during standby, the chip select should be held at $V_{IH}$ or $V_{CES}$ during the entire standby cycle.

## STANDBY OPERATING CONDITIONS OVER TEMPERATURE RANGE

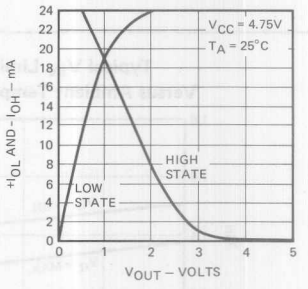
| Parameters | Description | Test Conditions | | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{PD}$ | $V_{CC}$ in Standby Mode | | | | 1.5 | | | |
| $I_{PD}$ | $I_{CC}$ in Standby Mode | $T_A = 0°C$, All Inputs = $V_{PD}$ | $V_{PD} = 1.5V$ | Am91L01 | | 11 | 25 | mA |
| | | | | Am9101 | | 13 | 31 | |
| | | | $V_{PD} = 2.0V$ | Am91L01 | | 13 | 31 | |
| | | | | Am9101 | | 17 | 41 | |
| | | $T_A = -55°C$, All Inputs = $V_{PD}$ | $V_{PD} = 1.5V$ | Am91L01 | | 11 | 28 | mA |
| | | | | Am9101 | | 13 | 34 | |
| | | | $V_{PD} = 2.0V$ | Am91L01 | | 13 | 34 | |
| | | | | Am9101 | | 17 | 46 | |
| dv/dt | Rate of Change of $V_{CC}$ | | | | | | 1.0 | V/μs |
| $t_R$ | Standby Recovery Time | | | | $t_{RC}$ | | | ns |
| $t_{CP}$ | Chip Deselect Time | | | | 0 | | | ns |
| $V_{CES}$ | $\overline{CE}$ Bias in Standby | | | | $V_{PD}$ | | | Volts |



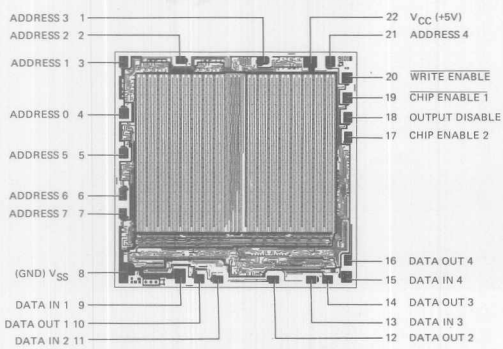

**Typical Power Supply Current Versus Voltage**




**Typical Output Current Versus Voltage**



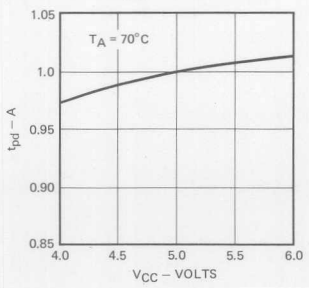

**Metallization and Pad Layout**



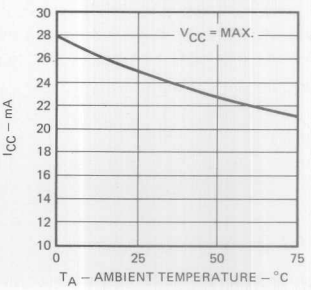

DIE SIZE 0.132" X 0.131"

(Pin numbers are for DIP configurations only)

**Access Time Versus $V_{CC}$ Normalized to $V_{CC}$ = +5.0 Volts**

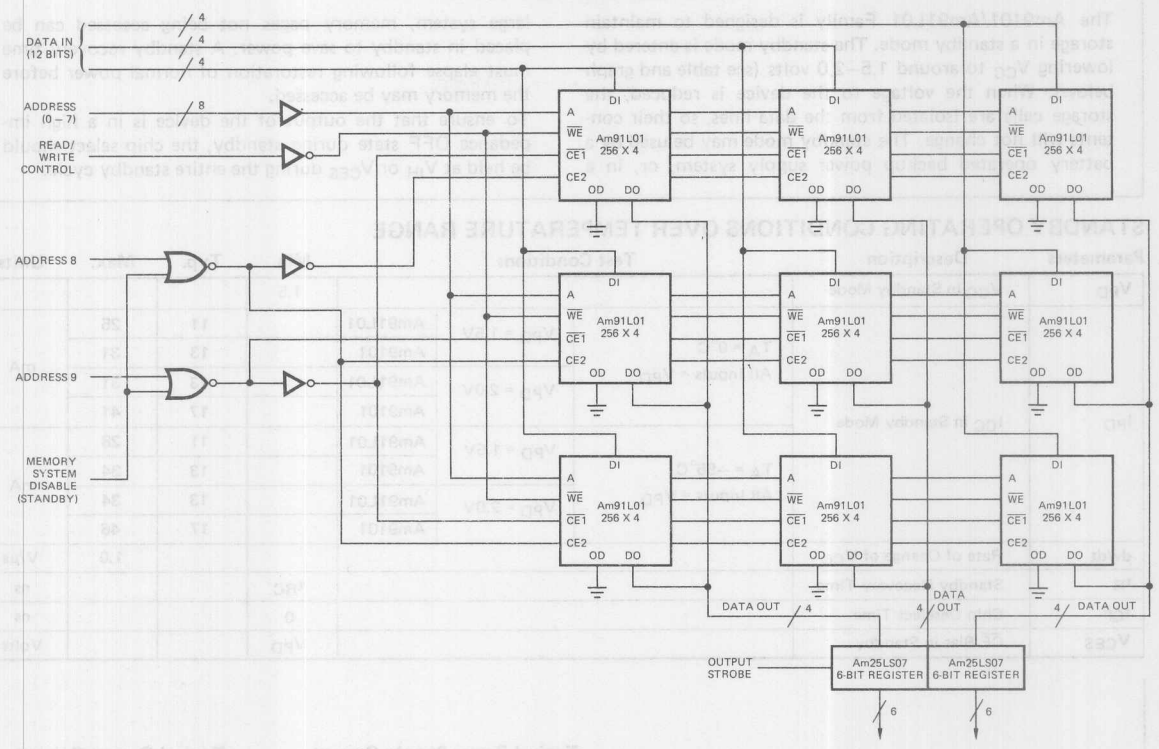



**Typical Power Supply Current Versus Ambient Temperature**




MOS-347

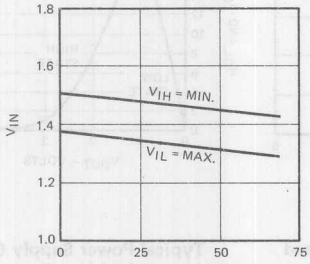
## APPLICATIONS



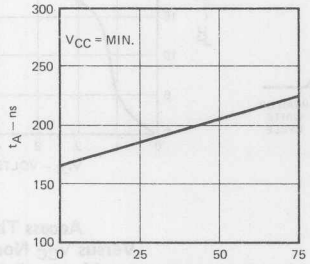

**MEMORY SYSTEM**
**768 WORDS BY 12 BITS PER WORD**

MOS-348

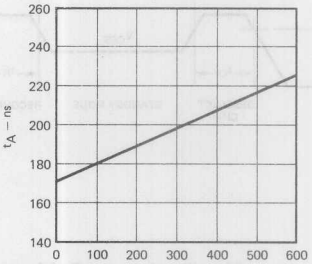
### Typical $V_{IN}$ Limits Versus Ambient Temperature




### Typical $t_A$ Versus Ambient Temperature




### Typical $t_A$ Versus $C_L$




MOS-349

# Am9111/Am91L11/Am2111 FAMILY

## 256x4 Static R/W Random Access Memories

2

| PART NUMBER | Am2111 | Am2111-2 | Am9111A<br>Am91L11A<br>Am2111-1 | Am9111B<br>Am91L11B | Am9111C<br>Am91L11C | Am9111D |
|---|---|---|---|---|---|---|
| ACCESS TIME | 1000ns | 650ns | 500ns | 400ns | 300ns | 250ns |

### DISTINCTIVE CHARACTERISTICS

- 256 x 4 organization for small memory systems
- Low operating power dissipation
  - 125mW Typ; 290mW maximum — standard power
  - 100mW Typ; 175mW maximum — low power
- DC standby mode reduces power up to 84%
- Logic voltage levels identical to TTL
- High output drive — two full TTL loads
- High noise immunity — full 400mV
- Single 5 volt power supply — tolerances: ±5% commercial, ±10% military
- Uniform switching characteristics — access times insensitive to supply variations, addressing patterns and data patterns
- Both military and commercial temperature ranges available
- Bussed input and output data on common pins.
- Output disable control
- Zero address set-up and hold times for simplified timing
- 100% MIL-STD-883 reliability assurance testing

### FUNCTIONAL DESCRIPTION

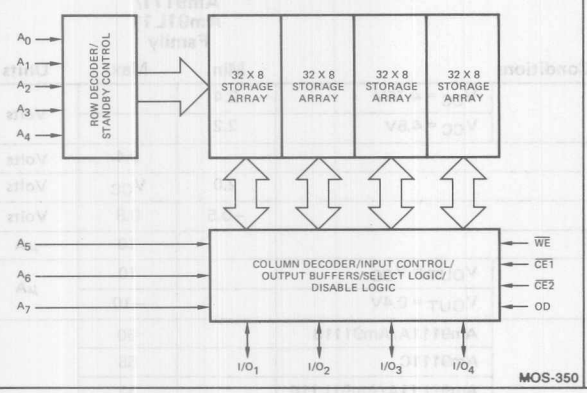
The Am9111/Am91L11 series of devices are high performance, low power, 1024-bit, static, read/write random access memories. They offer a wide range of access times including versions as fast as 200ns. Each memory is implemented as 256 words by 4 bits per word. This organization permits efficient design of small memory systems and allows finer resolution of incremental memory depth. The input data and output data signals are bussed together to share common I/O pins. This feature not only decreases the package size, but helps eliminate external logic in bus-oriented memory systems.

These memories may be operated in a DC standby mode for reductions of as much as 84% of the normal power dissipation. Data can be retained with a power supply as low as 1.5 volts. The low power Am91L11 series offer reduced power dissipation during normal operating conditions and even lower dissipation in the stand-by mode.

The Chip Enable input control signals act as high order address lines and they control the write amplifier and the output buffers. The Output Disable signal provides independent control over the output state of enabled chips.

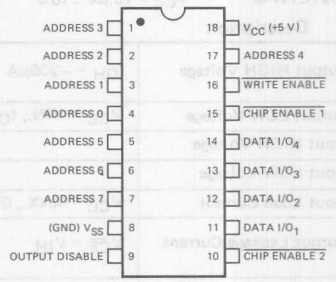
These devices are all fully static and no refresh operations or sense amplifiers or clocks are required. Input and output signal levels are identical to TTL specifications, providing simplified interfacing and high noise immunity. The outputs will drive two full TTL loads for increased fan-out and better bus interfacing capability.

### Am9111 BLOCK DIAGRAM




MOS-350

### CONNECTION DIAGRAM
Top View




Note: Flat Pack version available in 24-pin package.

MOS-351

### ORDERING INFORMATION

| Ambient Temperature Specification | Package Type | Power Type | Access Times | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | 1000ns | 650ns | 500ns | 400ns | 300ns | 250ns |
| 0°C to +70°C | Molded DIP | Standard | P2111 | P2111-2 | P2111-1<br>AM9111APC | AM9111BPC | AM9111CPC | AM9111DPC |
| | | Low | | | AM91L11APC | AM91L11BPC | AM91L11CPC | |
| | Hermetic DIP | Standard | C2111 | C2111-2 | C2111-1<br>AM9111ADC | AM9111BDC | AM9111CDC | AM9111DDC |
| | | Low | | | AM91L11ADC | AM91L11BDC | AM91L11CDC | |
| −55°C to +125°C | Hermetic DIP | Standard | | | AM9111ADM | AM9111BDM | AM9111CDM | |
| | | Low | | | AM91L11ADM | AM91L11BDM | AM91L11CDM | |
| | Hermetic Flat Pack | Standard | | | AM9111AFM | AM9111BFM | | |
| | | Low | | | AM91L11AFM | AM91L11BFM | | |

## MAXIMUM RATINGS above which the useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| $V_{CC}$ With Respect to $V_{SS}$, Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs | −0.5V to +7.0V |
| DC Input Voltage | −0.5V to +7.0V |
| Power Dissipation | 1.0W |

## ELECTRICAL CHARACTERISTICS

Am9111PC, Am9111DC, Am91L11PC, Am91L11DC, Am2111: $T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 5\%$

| Parameters | Description | Test Conditions | | | Am9111/Am91L11 Family Min. | Am9111/Am91L11 Family Max. | Am2111 Family Min. | Am2111 Family Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN. | | $I_{OH} = -200\mu A$ | 2.4 | | | | Volts |
| | | | | $I_{OH} = -150\mu A$ | | | 2.2 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN. | | $I_{OL} = 3.2mA$ | | 0.4 | | | Volts |
| | | | | $I_{OL} = 2.0mA$ | | | | 0.45 | |
| $V_{IH}$ | Input HIGH Voltage | | | | 2.0 | $V_{CC}$ | 2.2 | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Voltage | | | | −0.5 | 0.8 | −0.5 | 0.65 | Volts |
| $I_{LI}$ | Input Load Current | $V_{CC}$ = MAX., $0V \leq V_{IN} \leq 5.25V$ | | | | 10 | | 10 | µA |
| $I_{LO}$ | I/O Leakage Current | $V_{\overline{CE}} = V_{IH}$ | | $V_{OUT} = V_{CC}$ | | 5.0 | | 15 | µA |
| | | | | $V_{OUT} = 0.4V$ | | −10 | | −50 | |
| $I_{CC1}$ | Power Supply Current | Data out open, $V_{CC}$ = Max., $V_{IN} = V_{CC}$ | $T_A = 25°C$ | Am9111A/B | | 50 | | 60 | mA |
| | | | | Am9111C/D/E | | 55 | | | |
| | | | | Am91L11A/B | | 31 | | | |
| | | | | Am91L11C | | 34 | | | |
| $I_{CC2}$ | | | $T_A = 0°C$ | Am9111A/B | | 55 | | 70 | |
| | | | | Am9111C/D/E | | 60 | | | |
| | | | | Am91L11A/B | | 33 | | | |
| | | | | Am91L11C | | 36 | | | |

## ELECTRICAL CHARACTERISTICS

Am9111DM, Am9111FM, Am91L11DM, Am91L11FM: $T_A = -55°C$ to $+125°C$, $V_{CC} = +5.0V \pm 10\%$

| Parameters | Description | Test Conditions | | | Am9111/Am91L11 Family Min. | Am9111/Am91L11 Family Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -200\mu A$ | | $V_{CC} = 4.75V$ | 2.4 | | Volts |
| | | | | $V_{CC} = 4.5V$ | 2.2 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL} = 3.2mA$ | | | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | | | 2.0 | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Voltage | | | | −0.5 | 0.8 | Volts |
| $I_{LI}$ | Input Load Current | $V_{CC}$ = MAX., $0V \leq V_{IN} \leq 5.5V$ | | | | 10 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{\overline{CE}} = V_{IH}$ | | $V_{OUT} = V_{CC}$ | | 10 | µA |
| | | | | $V_{OUT} = 0.4V$ | | −10 | |
| $I_{CC1}$ | Power Supply Current | Data out open, $V_{CC}$ = Max., $V_{IN} = V_{CC}$ | $T_A = 25°C$ | Am9111A/Am9111B | | 50 | mA |
| | | | | Am9111C | | 55 | |
| | | | | Am91L11A/Am91L11B | | 31 | |
| | | | | Am91L11C | | 34 | |
| $I_{CC3}$ | | | $T_A = -55°C$ | Am9111A/Am9111B | | 60 | |
| | | | | Am9111C | | 65 | |
| | | | | Am91L11A/Am91L11B | | 37 | |
| | | | | Am91L11C | | 40 | |

## CAPACITANCE

| Parameters | Description | Test Conditions | | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance, $V_{IN} = 0V$ | $T_A = 25°C$, f = 1 mHz | Am2111 | 4.0 | 8.0 | pF |
| | | | Am9111/Am91L11 | 3.0 | 6.0 | |
| $C_{OUT}$ | Output Capacitance, $V_{OUT} = 0V$ | | Am2111 | 10 | 15 | pF |
| | | | Am9111/Am91L11 | 8.0 | 11 | |

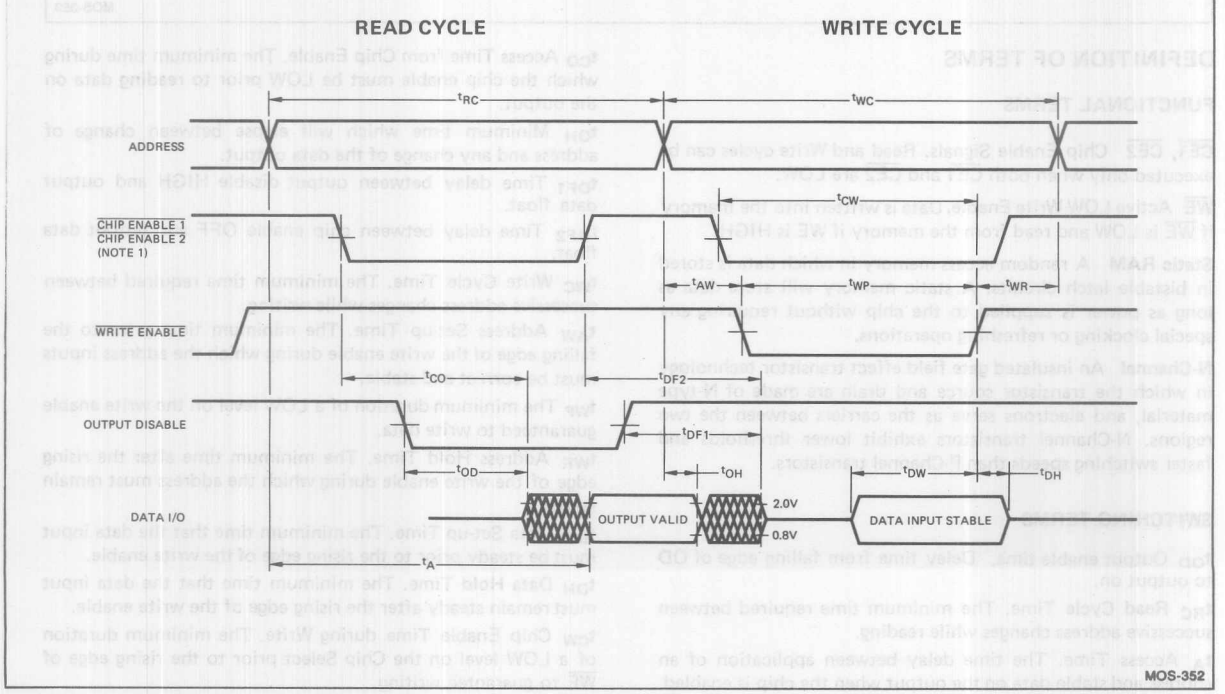
## SWITCHING CHARACTERISTICS over operating temperature and voltage range

Output Load = 1 TTL Gate + 100pF — $T_A$ = 0 to 70°C — $V_{CC}$ = +5V ±5%
Transition Times = 10ns — $T_A$ = −55 to +125°C — $V_{CC}$ = +5V ±10%
Input Levels, Output References = 0.8V and 2.0V

| Parameters | Description | 2111 Min | 2111 Max | 2111-2 Min | 2111-2 Max | 2111-1 Min | 2111-1 Max | 9111A 91L11A Min | 9111A 91L11A Max | 9111B 91L11B Min | 9111B 91L11B Max | 9111C 91L11C Min | 9111C 91L11C Max | 9111D Min | 9111D Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{RC}$ | Read Cycle Time | 1000 | | 650 | | 500 | | 500 | | 400 | | 300 | | 250 | | ns |
| $t_A$ | Access Time | | 1000 | | 650 | | 500 | | 500 | | 400 | | 300 | | 250 | ns |
| $t_{CO}$ | Chip Enable to Output ON Delay (Note 1) | | 800 | | 400 | | 350 | | 200 | | 175 | | 150 | | 125 | ns |
| $t_{OD}$ | Output Disable to Output ON Delay | | 700 | | 350 | | 300 | | 175 | | 150 | | 125 | | 100 | ns |
| $t_{OH}$ | Previous Read Data Valid with Respect to Address Change | 0 | | 0 | | 0 | | 40 | | 40 | | 40 | | 30 | | ns |
| $t_{DF1}$ | Output Disable to Output OFF Delay | 0 | 200 | 0 | 150 | 0 | 150 | 5.0 | 125 | 5.0 | 100 | 5.0 | 100 | 5.0 | 75 | ns |
| $t_{DF2}$ | Chip Enable to Output OFF Delay | 0 | 200 | 0 | 150 | 0 | 150 | 10 | 150 | 10 | 125 | 10 | 125 | 10 | 100 | ns |
| $t_{WC}$ | Write Cycle Time | 1000 | | 650 | | 500 | | 500 | | 400 | | 300 | | 250 | | ns |
| $t_{AW}$ | Address Set-up Time | 150 | | 150 | | 100 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{WP}$ | Write Pulse Width | 750 | | 400 | | 300 | | 175 | | 150 | | 125 | | 100 | | ns |
| $t_{CW}$ | Chip Enable Set-up Time (Note 1) | 900 | | 550 | | 400 | | 175 | | 150 | | 125 | | 100 | | ns |
| $t_{WR}$ | Address Hold Time | 50 | | 50 | | 50 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{DW}$ | Input Data Set-up Time | 700 | | 400 | | 280 | | 150 | | 125 | | 100 | | 85 | | ns |
| $t_{DH}$ | Input Data Hold Time | 100 | | 100 | | 100 | | 0 | | 0 | | 0 | | 0 | | ns |

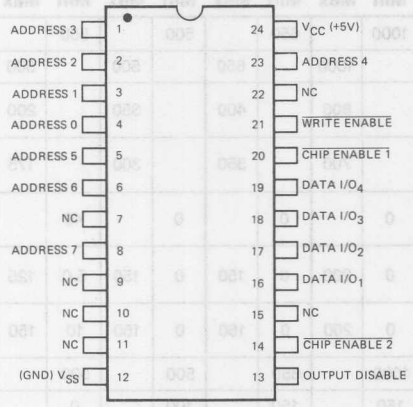
Note: 1. Both $\overline{CE1}$ and $\overline{CE2}$ must be LOW to enable the chip.

## SWITCHING WAVEFORMS



## CONNECTION DIAGRAM
Top View

Flat Package




Pin 1 is marked for orientation.

MOS-353

## DEFINITION OF TERMS

### FUNCTIONAL TERMS

$\overline{CE1}$, $\overline{CE2}$ Chip Enable Signals. Read and Write cycles can be executed only when both $\overline{CE1}$ and $\overline{CE2}$ are LOW.

$\overline{WE}$ Active LOW Write Enable. Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if WE is HIGH.

**Static RAM** A random access memory in which data is stored in bistable latch circuits. A static memory will store data as long as power is supplied to the chip without requiring any special clocking or refreshing operations.

**N-Channel** An insulated gate field effect transistor technology in which the transistor source and drain are made of N-type material, and electrons serve as the carriers between the two regions. N-Channel transistors exhibit lower thresholds and faster switching speeds than P-Channel transistors.

### SWITCHING TERMS

$t_{OD}$ Output enable time. Delay time from falling edge of OD to output on.

$t_{RC}$ Read Cycle Time. The minimum time required between successive address changes while reading.

$t_A$ Access Time. The time delay between application of an address and stable data on the output when the chip is enabled.

$t_{CO}$ Access Time from Chip Enable. The minimum time during which the chip enable must be LOW prior to reading data on the output.

$t_{OH}$ Minimum time which will elapse between change of address and any change of the data output.

$t_{DF1}$ Time delay between output disable HIGH and output data float.

$t_{DF2}$ Time delay between chip enable OFF and output data float.

$t_{WC}$ Write Cycle Time. The minimum time required between successive address changes while writing.

$t_{AW}$ Address Set-up Time. The minimum time prior to the falling edge of the write enable during which the address inputs must be correct and stable.

$t_{WP}$ The minimum duration of a LOW level on the write enable guaranteed to write data.

$t_{WR}$ Address Hold Time. The minimum time after the rising edge of the write enable during which the address must remain steady.

$t_{DW}$ Data Set-up Time. The minimum time that the data input must be steady prior to the rising edge of the write enable.

$t_{DH}$ Data Hold Time. The minimum time that the data input must remain steady after the rising edge of the write enable.

$t_{CW}$ Chip Enable Time during Write. The minimum duration of a LOW level on the Chip Select prior to the rising edge of $\overline{WE}$ to guarantee writing.

2

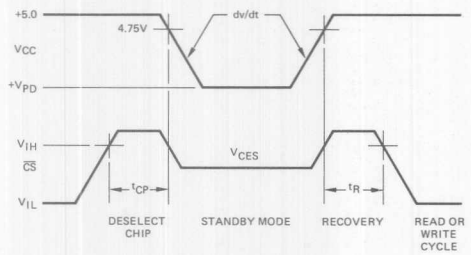
## POWER DOWN STANDBY OPERATION

The Am9111/Am91L11 Family is designed to maintain storage in a standby mode. The standby mode is entered by lowering $V_{CC}$ to around 1.5–2.0 volts (see table and graph below). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated backup power supply system, or, in a large system, memory pages not being accessed can be placed in standby to save power. A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

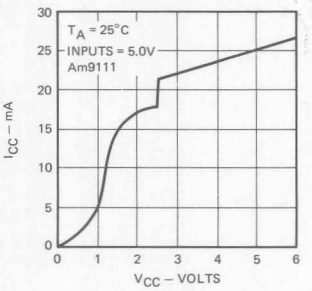
To ensure that the output of the device is in a high impedance OFF state during standby, the chip select should be held at $V_{IH}$ or $V_{CES}$ during the entire standby cycle.

## STANDBY OPERATING CONDITIONS OVER TEMPERATURE RANGE

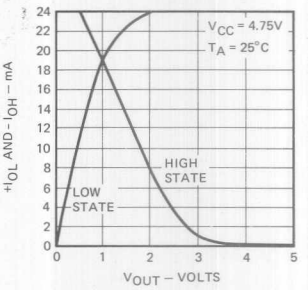
| Parameters | Description | Test Conditions | | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{PD}$ | $V_{CC}$ in Standby Mode | | | | 1.5 | | | |
| $I_{PD}$ | $I_{CC}$ in Standby Mode | $T_A = 0°C$, All Inputs = $V_{PD}$ | $V_{PD} = 1.5V$ | Am91L11 | | 11 | 25 | mA |
| | | | | Am9111 | | 13 | 31 | |
| | | | $V_{PD} = 2.0V$ | Am91L11 | | 13 | 31 | |
| | | | | Am9111 | | 17 | 41 | |
| | | $T_A = -55°C$, All Inputs = $V_{PD}$ | $V_{PD} = 1.5V$ | Am91L11 | | 11 | 28 | mA |
| | | | | Am9111 | | 13 | 34 | |
| | | | $V_{PD} = 2.0V$ | Am91L11 | | 13 | 34 | |
| | | | | Am9111 | | 17 | 46 | |
| dv/dt | Rate of Change of $V_{CC}$ | | | | | | 1.0 | V/μs |
| $t_R$ | Standby Recovery Time | | | | $t_{RC}$ | | | ns |
| $t_{CP}$ | Chip Deselect Time | | | | 0 | | | ns |
| $V_{CES}$ | $\overline{CE}$ Bias in Standby | | | | $V_{PD}$ | | | Volts |



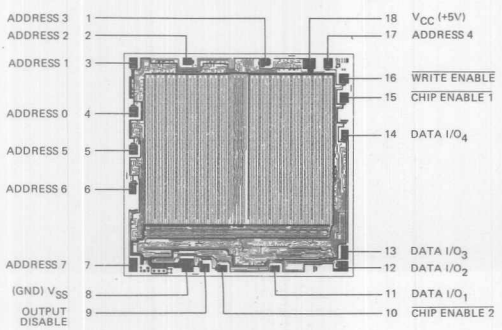

**Typical Power Supply Current Versus Voltage**




**Typical Output Current Versus Voltage**



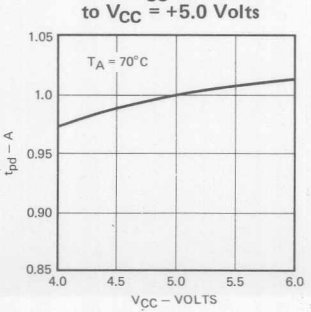

**Metallization and Pad Layout**



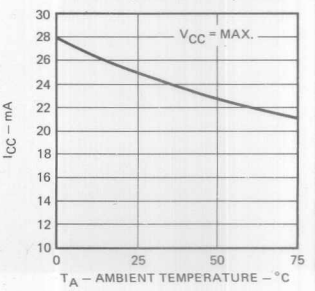

DIE SIZE: 0.132" X 0.131"

(Pin numbers shown are for DIP versions only)

**Access Time Versus $V_{CC}$ Normalized to $V_{CC}$ = +5.0 Volts**




**Typical Power Supply Current Versus Ambient Temperature**



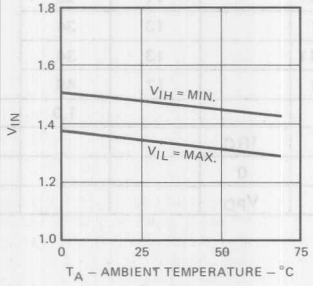

MOS-354

supply, all TTL interface, no clocks, no sensing, no refreshing, military temperature range available, low power versions available, high speed, high output drive, etc. In addition, the Am9111 series features a 256 x 4 organization with common pins used for both Data In and Data Out signals.

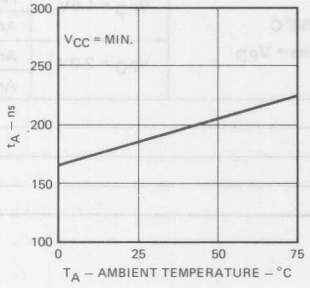
This bussed I/O approach cuts down the package pin count allowing the design of higher density memory systems. It also provides a direct interface to bus-oriented systems, eliminating bussing logic that could otherwise be required. Most microprocessor systems, for example, transfer information on a bidirectional data bus. The Am9111 memories can connect

contention for the bus lines, and to simplify tri-state bus control in the external circuitry. If the chip is enabled and the output is enabled and the memory is in the Read state, then the output buffers will be impressing data on the bus lines. At that point, if the external system tries to drive the bus with data, in preparation for a write operation, there will be conflict for domination of the bus lines. The Output Disable signal allows the user direct control over the output buffers, independent of the state of the memory. Although there are alternative ways to resolve the conflict, normally Output Disable will be held high during a write operation.

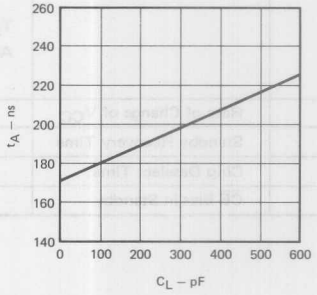
**Typical $V_{IN}$ Limits Versus Ambient Temperature**




**Typical $t_A$ Versus Ambient Temperature**




**Typical $t_A$ Versus $C_L$**




MOS-355

# Am9112/Am91L12 FAMILY

## 256x4 Static R/W Random Access Memories

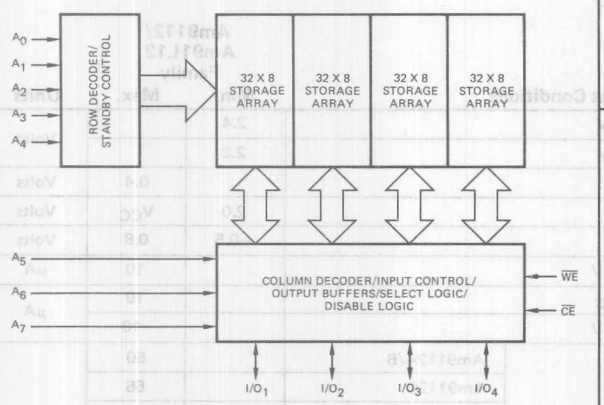
2

| Part Number | Am2112 | Am2112-2 | Am9112A Am91L12A | Am9112B Am91L12B | Am9112C Am91L12C | Am9112D |
|---|---|---|---|---|---|---|
| Access Time | 1000ns | 650ns | 500ns | 400ns | 300ns | 250ns |

### Distinctive Characteristics

- 256 x 4 organization
- 16-pin standard DIP
- Low operating power dissipation
  - 125mW Typ; 290mW maximum — standard power
  - 100mW Typ; 175mW maximum — low power
- DC standby mode reduces power up to 84%
  - 20mW Typ; 47mW maximum
- Logic voltage levels identical to TTL
- High output drive — two full TTL loads guaranteed
- High noise immunity — full 400mV
- Uniform switching characteristics — access times insensitive to supply variations, address patterns and data patterns.
- Single +5V power supply — tolerances ±5% commercial, ±10% military
- Bus oriented I/O data
- Zero address, set-up, and hold times guaranteed for simpler timing
- Direct plug-in replacement for 2112 type devices
- 100% MIL-STD-883 reliability assurance testing

### Am9112 BLOCK DIAGRAM




MOS-356

### FUNCTIONAL DESCRIPTION

The Am9112/Am91L12 series of products are high performance, low power, 1024-bit, static read/write random access memories. They offer a range of speeds and power dissipations including versions as fast as 200ns and as low as 100mW typical.

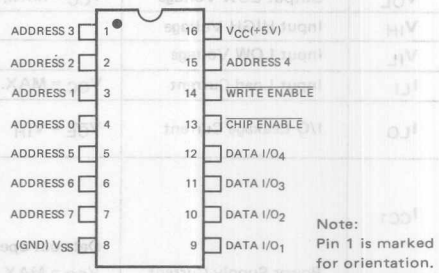
Each memory is implemented as 256 words by 4-bits per word. This organization allows efficient design of small memory systems and permits finer resolution of incremental memory word size relative to 1024 by 1 devices. The output and input data signals are internally bussed together and share 4 common I/O pins. This feature keeps the package size small and provides a simplified interface to bus-oriented systems.

The Am9112/Am91L12 memories may be operated in a DC standby mode for reductions of as much as 84% of the normal operating power dissipation. Though the memory cannot be operated, data can be retained in the storage cells with a power supply as low as 1.5 volts. The Am91L12 versions offer reduced power during normal operating conditions as well as even lower dissipation in standby mode.

The eight Address inputs are decoded to select 1-of-256 locations within the memory. The Chip Enable input acts as a high-order address in multiple chip systems. It also controls the write amplifier and the output buffers in conjunction with the Write Enable input. When $\overline{CE}$ is low and $\overline{WE}$ is high, the write amplifiers are disabled, the output buffers are enabled and the memory will execute a read cycle. When $\overline{CE}$ is low and $\overline{WE}$ is low, the write amplifiers are enabled, the output buffers are disabled and the memory will execute a write cycle. When $\overline{CE}$ is high both the write amplifiers and the output buffers are disabled.

These memories are fully static and require no refresh operations or sense amplifiers or clocks. All input and output voltage levels are identical to standard TTL specifications, including the power supply.

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

MOS-357

### ORDERING INFORMATION

| Ambient Temperature Specification | Package Type | Power Type | Access Times | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | 1000ns | 650ns | 500ns | 400ns | 300ns | 250ns |
| 0°C to +70°C | Molded DIP | Standard | P2112 | P2112-2 | AM9112APC | AM9112BPC | AM9112CPC | AM9112DPC |
| | | Low | | | AM91L12APC | AM91L12BPC | AM91L12CPC | |
| | Hermetic DIP | Standard | C2112 | C2112-2 | AM9112ADC | AM9112BDC | AM9112CDC | AM9112DDC |
| | | Low | | | AM91L12ADC | AM91L12BDC | AM91L12CDC | |
| −55°C to +125°C | Hermetic DIP | Standard | | | AM9112ADM | AM9112BDM | AM9112CDM | |
| | | Low | | | AM91L12ADM | AM91L12BDM | AM91L12CDM | |
| | Hermetic Flat Pack | Standard | | | AM9112AFM | AM9112BFM | | |
| | | Low | | | AM91L12AFM | AM91L12BFM | | |

## MAXIMUM RATINGS above which the useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| $V_{CC}$ With Respect to $V_{SS}$, Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs | −0.5V to +7.0V |
| DC Input Voltage | −0.5V to +7.0V |
| Power Dissipation | 1.0W |

## ELECTRICAL CHARACTERISTICS

Am9112PC, Am9112DC $T_A = 0°C$ to $+70°C$
Am91L12PC, Am91L12DC $V_{CC} = +5V \pm 5\%$

| Parameters | Description | Test Conditions | | | Am9112/Am91L12 Family Min. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH} = -200\mu A$ | | | 2.4 | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 3.2mA | | | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | | | 2.0 | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Voltage | | | | −0.5 | 0.8 | Volts |
| $I_{LI}$ | Input Load Current | $V_{CC}$ = MAX., $0V \leq V_{IN} \leq 5.25V$ | | | | 10 | µA |
| $I_{LO}$ | I/O Leakage Current | $V_{\overline{CE}} = V_{IH}$ | $V_{OUT} = V_{CC}$ | | | 5.0 | µA |
| | | | $V_{OUT} = 0.4V$ | | | −10 | |
| $I_{CC1}$ | Power Supply Current | Data out open $V_{CC}$ = MAX. $V_{IN} = V_{CC}$ | $T_A = 25°C$ | Am9112A/B | | 50 | mA |
| | | | | Am9112C/D/E | | 55 | |
| | | | | Am91L12A/B | | 31 | |
| | | | | Am91L12C | | 34 | |
| $I_{CC2}$ | | | $T_A = 0°C$ | Am9112A/B | | 55 | |
| | | | | Am9112C/D/E | | 60 | |
| | | | | Am91L12A/B | | 33 | |
| | | | | Am91L12C | | 36 | |

## ELECTRICAL CHARACTERISTICS

Am9112DM, Am9112FM $T_A = -55°C$ to $+125°C$
Am91L12DM, Am91L12FM $V_{CC} = +5.0V \pm 10\%$

| Parameters | Description | Test Conditions | | | Am9112/Am91L12 Family Min. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -200\mu A$ | $V_{CC} = 4.75V$ | | 2.4 | | Volts |
| | | | $V_{CC} = 4.50V$ | | 2.2 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 3.2mA | | | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | | | 2.0 | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Voltage | | | | −0.5 | 0.8 | Volts |
| $I_{LI}$ | Input Load Current | $V_{CC}$ = MAX., $0V \leq V_{IN} \leq 5.5V$ | | | | 10 | µA |
| $I_{LO}$ | I/O Leakage Current | $V_{\overline{CE}} = V_{IH}$ | $V_{OUT} = V_{CC}$ | | | 10 | µA |
| | | | $V_{OUT} = 0.4V$ | | | −10 | |
| $I_{CC1}$ | Power Supply Current | Data out open $V_{CC}$ = MAX. $V_{IN} = V_{CC}$ | $T_A = 25°C$ | Am9112A/B | | 50 | mA |
| | | | | Am9112C | | 55 | |
| | | | | Am91L12A/B | | 31 | |
| | | | | Am91L12C | | 34 | |
| $I_{CC3}$ | | | $T_A = -55°C$ | Am9112A/B | | 60 | |
| | | | | Am9112C | | 65 | |
| | | | | Am91L12A/B | | 37 | |
| | | | | Am91L12C | | 40 | |

## CAPACITANCE

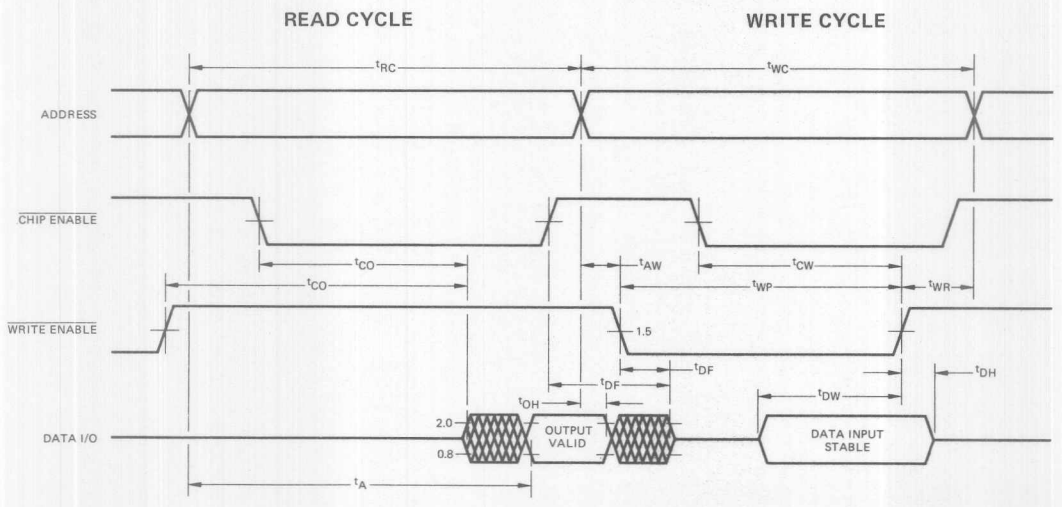
| Parameters | Description | Test Conditions | | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance, $V_{IN}$ = 0V | $T_A = 25°C$, f = 1 mHz | Am2112 | 4.0 | 8.0 | pF |
| | | | Am9112/Am91L12 | 3.0 | 6.0 | |
| $C_{OUT}$ | Output Capacitance, $V_{OUT}$ = 0V | | Am2112 | 10 | 18 | pF |
| | | | Am9112/Am91L12 | 8.0 | 11 | |

## SWITCHING CHARACTERISTICS over operating temperature and voltage range

Output Load = 1 TTL Gate +100pF
Transition Times = 10ns
Input Levels, Output References = 0.8V and 2.0V

| Parameters | Description | Am9112A Am91L12A Min | Am9112A Am91L12A Max | Am9112B Am91L12B Min | Am9112B Am91L12B Max | Am9112C Am91L12C Min | Am9112C Am91L12C Max | Am9112D Min | Am9112D Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{RC}$ | Read Cycle Time | 500 | | 400 | | 300 | | 250 | | ns |
| $t_A$ | Access Time | | 500 | | 400 | | 300 | | 250 | ns |
| $t_{CO}$ | Output Enabled to Output ON Delay (Note 1) | 5.0 | 175 | 5.0 | 150 | 5.0 | 125 | 5.0 | 100 | ns |
| $t_{OH}$ | Previous Read Data Valid with Respect to Address Change | 40 | | 40 | | 40 | | 30 | | ns |
| $t_{DF}$ | Output Disabled to Output OFF Delay (Note 2) | 5.0 | 125 | 5.0 | 100 | 5.0 | 100 | 5.0 | 75 | ns |
| $t_{WC}$ | Write Cycle Time | 500 | | 400 | | 300 | | 250 | | ns |
| $t_{AW}$ | Address Set-up Time | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{WR}$ | Address Hold Time | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{WP}$ | Write Pulse Width (Note 3) | 175 | | 150 | | 125 | | 100 | | ns |
| $t_{CW}$ | Chip Enable Set-up Time | 175 | | 150 | | 125 | | 100 | | ns |
| $t_{DW}$ | Input Data Set-up Time | 150 | | 125 | | 100 | | 85 | | ns |
| $t_{DH}$ | Input Data Hold Time (Note 4) | 0 | | 0 | | 0 | | 0 | | ns |

## SWITCHING WAVEFORMS (Note 5)




Notes: 1. Output is enabled and $t_{CO}$ commences only with both $\overline{CE}$ LOW and $\overline{WE}$ HIGH.
2. Output is disabled and $t_{DF}$ defined from either the rising edge of $\overline{CE}$ or the falling edge of $\overline{WE}$.
3. Minimum $t_{WP}$ is valid when $\overline{CE}$ has been HIGH at least $t_{DF}$ before $\overline{WE}$ goes LOW. Otherwise $t_{WP(min.)} = t_{DW(min.)} + t_{DF(max.)}$.
4. When $\overline{WE}$ goes HIGH at the end of the write cycle, it will be possible to turn on the output buffers if $\overline{CE}$ is still LOW. The data out will be the same as the data just written and so will not conflict with input data that may still be on the I/O bus.
5. See "Application Information" section of this specification.

MOS-358

## DEFINITION OF TERMS

### FUNCTIONAL TERMS

$\overline{CE}$ Active LOW Chip Enable. Data can be read from or written into the memory only if $\overline{CE}$ is LOW.

$\overline{WE}$ Active LOW Write Enable. Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if $\overline{WE}$ is HIGH.

**Static RAM** A random access memory in which data is stored in bistable latch circuits. A static memory will store data as long as power is supplied to the chip without requiring any special clocking or refreshing operations.

**N-Channel** An insulated gate field effect transistor technology in which the transistor source and drain are made of N-type material, and electrons serve as the carriers between the two regions. N-Channel transistors exhibit lower thresholds and faster switching speeds than P-Channel transistors.

### SWITCHING TERMS

$t_{RC}$ Read Cycle Time. The minimum time required between successive address changes while reading.

$t_A$ Access Time. The time delay between application of an address and stable data on the output when the chip is enabled.

$t_{CO}$ Output Enable Time. The time during which $\overline{CE}$ must be LOW and $\overline{WE}$ must be HIGH prior to data on the output.

$t_{OH}$ Minimum time which will elapse between change of address and any change on the data output.

$t_{DF}$ Time which will elapse between a change on the chip enable or the right enable and on data outputs being driven to a floating status.

$t_{WC}$ Write Cycle Time. The minimum time required between successive address changes while writing.

$t_{AW}$ Address Set-up Time. The minimum time prior to the falling edge of the write enable during which the address inputs must be correct and stable.

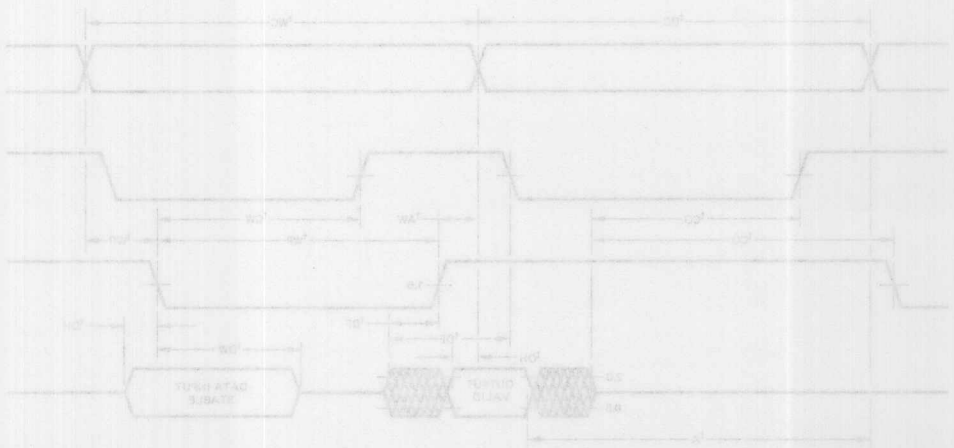
$t_{WP}$ The minimum duration of a LOW level on the write enable guaranteed to write data.

$t_{WR}$ Address Hold Time. The minimum time after the rising edge of the write enable during which the address must remain steady.

$t_{DW}$ Data Set-up Time. The minimum time that the data input must be steady prior to the rising edge of the write enable.

$t_{DH}$ Data Hold Time. The minimum time that the data input must remain steady after the rising edge of the write enable.

$t_{CW}$ Chip Enable Time During Write. The minimum duration of a LOW level on the Chip Select while the write enable is LOW to guarantee writing.



## POWER DOWN STANDBY OPERATION

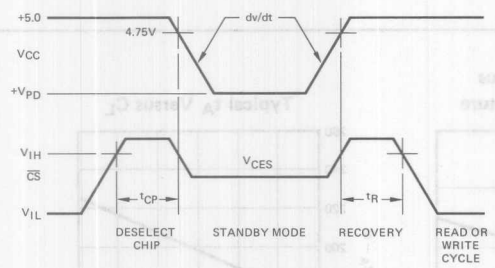
The Am9112/Am91L12 Family is designed to maintain storage in a standby mode. The standby mode is entered by lowering $V_{CC}$ to around 1.5–2.0 volts (see table and graph below). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated backup power supply system, or, in a large system, memory pages not being accessed can be placed in standby to save power. A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

To ensure that the output of the device is in a high impedance OFF state during standby, the chip select should be held at $V_{IH}$ or $V_{CES}$ during the entire standby cycle.

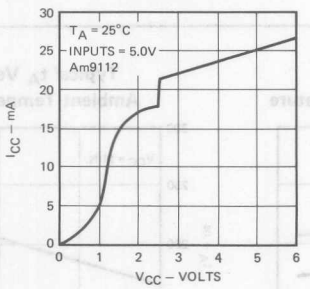
2

## STANDBY OPERATING CONDITIONS OVER TEMPERATURE RANGE

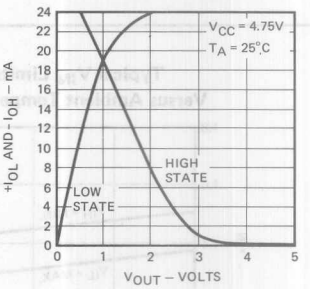
| Parameters | Description | Test Conditions | | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{PD}$ | $V_{CC}$ in Standby Mode | | | | 1.5 | | | |
| $I_{PD}$ | $I_{CC}$ in Standby Mode | $T_A = 0°C$, All Inputs = $V_{PD}$ | $V_{PD}$ = 1.5V | Am91L12 | | 11 | 25 | mA |
| | | | | Am9112 | | 13 | 31 | |
| | | | $V_{PD}$ = 2.0V | Am91L12 | | 13 | 31 | |
| | | | | Am9112 | | 17 | 41 | |
| | | $T_A = -55°C$, All Inputs = $V_{PD}$ | $V_{PD}$ = 1.5V | Am91L12 | | 11 | 28 | mA |
| | | | | Am9112 | | 13 | 34 | |
| | | | $V_{PD}$ = 2.0V | Am91L12 | | 13 | 34 | |
| | | | | Am9112 | | 17 | 46 | |
| dv/dt | Rate of Change of $V_{CC}$ | | | | | | 1.0 | V/μs |
| $t_R$ | Standby Recovery Time | | | | $t_{RC}$ | | | ns |
| $t_{CP}$ | Chip Deselect Time | | | | 0 | | | ns |
| $V_{CES}$ | $\overline{CE}$ Bias in Standby | | | | $V_{PD}$ | | | Volts |



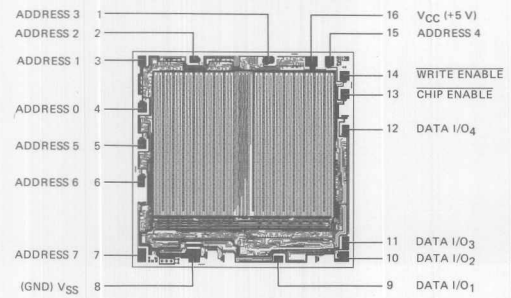

**Typical Power Supply Current Versus Voltage**




**Typical Output Current Versus Voltage**

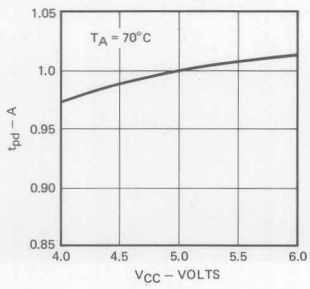



**Metallization and Pad Layout**

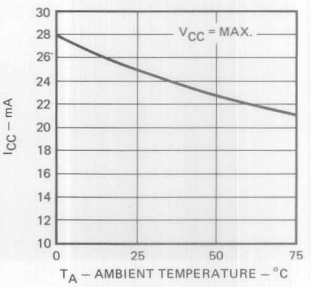



DIE SIZE 0.132" X 0.131"

**Access Time Versus $V_{CC}$ Normalized to $V_{CC}$ = +5.0 Volts**




**Typical Power Supply Current Versus Ambient Temperature**




MOS-359

## APPLICATION INFORMATION

These memory products provide all of the advantages of AMD's other static N-channel memory circuits: +5 only power supply, all TTL interface, no clocks, no sensing, no refreshing, military temperature range available, low power versions available, high speed, high output drive, etc. In addition, the Am9112 series features a 256 x 4 organization with common pins used for both Data In and Data Out signals.

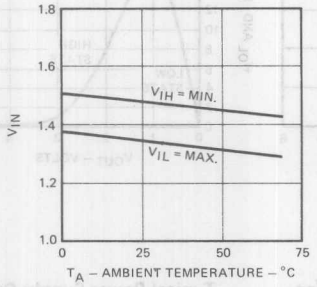
This bussed I/O approach keeps the package pin count low allowing the design of higher density memory systems. It also provides a direct interface to bus-oriented systems, eliminating bussing logic that could otherwise be required. Most microprocessor systems, for example, transfer information on a bidirectional data bus. The Am9112 memories can connect directly to such a processor since the common I/O pins act as a bidirectional data bus.

If the chip is enabled ($\overline{CE}$ low) and the memory is in the Read state ($\overline{WE}$ high), the output buffers will be turned on and will be driving data on the I/O bus lines. If the external system tries to drive the bus with data, there may be contention for control of the data lines and large current surges can result. Since the condition can occur at the beginning of a write cycle, it is important that incoming data to be written not be entered until the output buffers have been turned off.

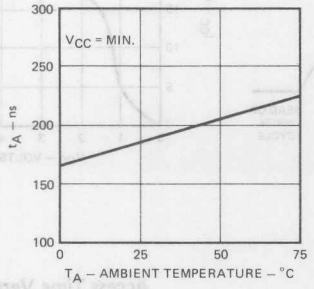
These operational suggestions for write cycles may be of some help for memory system designs:

1. For systems where $\overline{CE}$ is always low or is derived directly from addresses and so is low for the whole cycle, make sure $t_{WP}$ is at least $t_{DW} + t_{DF}$ and delay the input data until $t_{DF}$ following the falling edge of $\overline{WE}$. With zero address set-up and hold times it will often be convenient to make $\overline{WE}$ a cycle-width level ($t_{WP} = t_{WC}$) so that the only subcycle timing required is the delay of the input data.
2. For systems where $\overline{CE}$ is high for at least $t_{DF}$ preceding the falling edge of $\overline{WE}$, $t_{WP}$ may assume the minimum specified value. When $\overline{CE}$ is high for $t_{DF}$ before the start of the cycle, then no other subcycle timing is required and $\overline{WE}$ and data-in may be cycle-width levels.
3. Notice that because both $\overline{CE}$ and $\overline{WE}$ must be low to cause a write to take place, either signal can be used to determine the effective write pulse. Thus, $\overline{WE}$ could be a level with $\overline{CE}$ becoming the write timing signal. In such a case, the data set-up and hold times are specified with respect to the rising edge of $\overline{CE}$. The value of the data set-up time remains the same and the value of the data hold time should change to a minimum of 25ns.

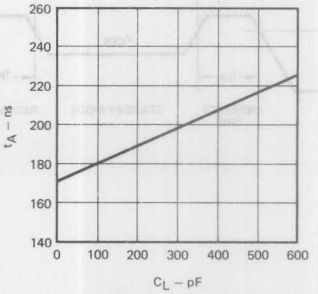
**Typical $V_{IN}$ Limits Versus Ambient Temperature**




**Typical $t_A$ Versus Ambient Temperature**




**Typical $t_A$ Versus $C_L$**




MOS-360

# Am9114 • Am9124

## 1024 x 4 Static R/W Random Access Memory

2

### DISTINCTIVE CHARACTERISTICS

- **LOW OPERATING POWER (MAX)**
  - **Am9124/Am9114 368mW (70mA)**
  - **Am91L24/Am91L14 262mW (50mA)**
- **LOW STANDBY POWER (MAX)**
  - **Am9124 158mW (30mA)**
  - **Am91L24 105mW (20mA)**
- Access times down to 200ns (max)
- Military temperature range available to 300ns (max)
- Am9114 is a direct plug-in replacement for 2114
- Am9124 pin and function compatible with Am9114 and 2114, plus $\overline{CS}$ power down feature
- Fully static – no clocking
- Identical access and cycle time
- High output drive –
  4.0mA sink current @ 0.4V – 9124
  3.2mA sink current @ 0.4V – 9114
- TTL identical input/output levels
- 100% MIL-STD-883 reliability assurance testing

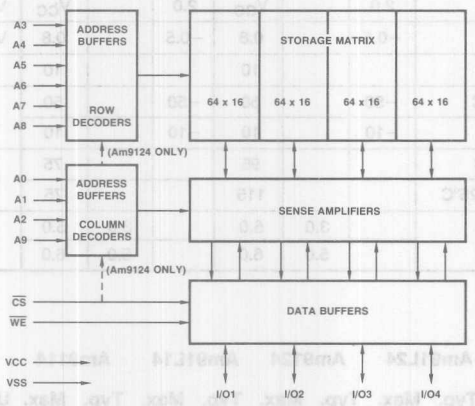
### GENERAL DESCRIPTION

The Am9114 and Am9124 are high performance, static, N-Channel, read/write, random access memories organized as 1024 x 4. Operation is from a single 5V supply, and all input/output levels are identical to standard TTL specifications. Low power versions of both devices are available with power savings of over 30%. The Am9114 and Am9124 are the same except that the Am9124 offers an automatic $\overline{CS}$ power down feature.

The Am9124 remains in a low power standby mode as long as $\overline{CS}$ remains high, thus reducing its power requirements. The Am9124 power decreases from 368mW to 158mW in the standby mode, and the Am91L24 from 262mW to 105mW. The $\overline{CS}$ input does not affect the power dissipation of the Am9114. (See Figure 1, page 4).

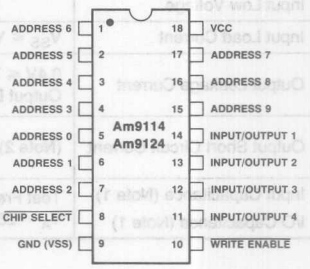
Data readout is not destructive and the same polarity as data input. $\overline{CS}$ provides for easy selection of an individual package when the outputs are OR-tied. The outputs of 4.0mA for Am9124 and 3.2mA for Am9114 provides increased short circuit current for improved capacitive drive.

### BLOCK DIAGRAM




MOS-066

### CONNECTION DIAGRAM




Top View
Pin 1 is marked for orientation.

MOS-067

### ORDERING INFORMATION

| Ambient Temperature | Package Type | ICC Current Level | Access Times | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | Am9114 | | | Am9124 (Power Down Option) | | |
| | | | 450ns | 300ns | 200ns | 450ns | 300ns | 200ns |
| 0°C ≤ $T_A$ ≤ 70°C | Plastic | 70mA | Am9114BPC | Am9114CPC | Am9114EPC | Am9124BPC | Am9124CPC | Am9124EPC |
| | | 50mA | Am91L14BPC | Am91L14CPC | | Am91L24BPC | Am91L24CPC | |
| | Hermetic | 70mA | Am9114BDC | Am9114CDC | Am9114EDC | Am9124BDC | Am9124CDC | Am9124EDC |
| | | 50mA | Am91L14BDC | Am91L14CDC | | Am91L24BDC | Am91L24CDC | |
| −55°C ≤ $T_A$ ≤ +125°C | Hermetic | 80mA | Am9114BDM | Am9114CDM | | Am9124BDM | Am9124CDM | |
| | | 60mA | Am91L14BDM | Am91L14CDM | | Am91L24BDM | Am91L24CDM | |

## MAXIMUM RATINGS beyond which useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| $V_{CC}$ with Respect to $V_{SS}$ | −0.5V to +7.0V |
| All Signal Voltages with Respect to $V_{SS}$ | −0.5V to +7.0V |
| Power Dissipation (Package Limitation) | 1.0W |
| DC Output Current | 10mA |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGE

| Part Number | Ambient Temperature | $V_{SS}$ | $V_{CC}$ | Part Number | Ambient Temperature | $V_{SS}$ | $V_{CC}$ |
|---|---|---|---|---|---|---|---|
| Am9114DC/PC<br>Am91L14DC/PC<br>Am9124DC/PC<br>Am91L24DC/PC | $0°C \leq T_A \leq +70°C$ | 0V | +5.0V ± 5% | Am9114DM<br>Am91L14DM<br>Am9124DM<br>Am91L24DM | $-55°C \leq T_A \leq +125°C$ | 0V | +5.0V ± 10% |

## ELECTRICAL CHARACTERISTICS over operating range

| Parameter | Description | Test Conditions | | Am9124XX Am91L24XX Min. | Typ. | Max. | Am9114XX Am91L14XX Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| $I_{OH}$ | Output High Current | $V_{OH}$ = 2.4V | $V_{CC}$ = 4.75V | −1.4 | | | −1.0 | | | mA |
| | | $V_{OH}$ = 2.2V | $V_{CC}$ = 4.5V | −1.0 | | | −1.0 | | | |
| $I_{OL}$ | Output Low Current | $V_{OL}$ = 0.4V | $T_A$ = +70°C | 4.0 | | | 3.2 | | | mA |
| | | | $T_A$ = +125°C | 3.2 | | | 2.4 | | | |
| $V_{IH}$ | Input High Voltage | | | 2.0 | | $V_{CC}$ | 2.0 | | $V_{CC}$ | Volts |
| $V_{IL}$ | Input Low Voltage | | | −0.5 | | 0.8 | −0.5 | | 0.8 | Volts |
| $I_{IX}$ | Input Load Current | $V_{SS} \leq V_I \leq V_{CC}$ | | | | 10 | | | 10 | μA |
| $I_{OZ}$ | Output Leakage Current | $0.4V \leq V_O \leq V_{CC}$ Output Disabled | $T_A$ = +125°C | −50 | | 50 | −50 | | 50 | μA |
| | | | $T_A$ = +70°C | −10 | | 10 | −10 | | 10 | |
| $I_{OS}$ | Output Short Circuit Current | (Note 2) | 0°C to +70°C | | | 95 | | | 75 | mA |
| | | | −55°C to +125°C | | | 115 | | | 75 | |
| CI | Input Capacitance (Note 1) | Test Frequency = 1.0MHz $T_A$ = 25°C, All pins at 0V | | | 3.0 | 5.0 | | 3.0 | 5.0 | pF |
| CI/O | I/O Capacitance (Note 1) | | | | 5.0 | 6.0 | | 5.0 | 6.0 | |

## ELECTRICAL CHARACTERISTICS over operating range

| Parameter | Description | Test Conditions | | Am91L24 Typ. | Max. | Am9124 Typ. | Max. | Am91L14 Typ. | Max. | Am9114 Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | Max. $V_{CC}$, $\overline{CS} \leq V_{IL}$ for Am9124/91L24 | $T_A$ = 25°C | 40 | | 60 | | 40 | | 60 | | mA |
| | | | $T_A$ = 0°C | | 50 | | 70 | | 50 | | 70 | |
| | | | $T_A$ = −55°C | | 60 | | 80 | | 60 | | 80 | |
| $I_{PD}$ | Automatic $\overline{CS}$ Power Down Current | Max. $V_{CC}$ ($\overline{CS} \geq V_{IH}$) | $T_A$ = 25°C | 15 | | 24 | | | – | | – | mA |
| | | | $T_A$ = 0°C | | 20 | | 30 | | – | | – | |
| | | | $T_A$ = −55°C | | 22 | | 33 | | – | | – | |

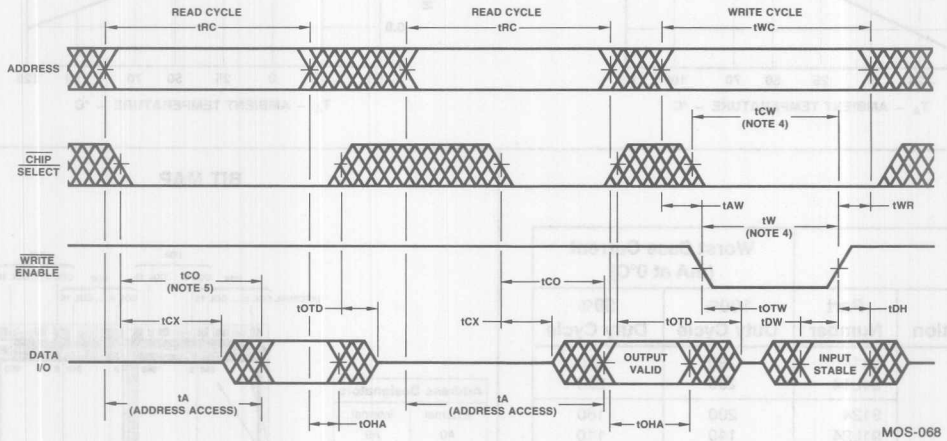
Notes:

1. Typical values are for $T_A$ = 25°C, nominal supply voltage and nominal processing parameters.
2. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
3. Test conditions assume signal transition times of 10ns or less, timing reference levels of 1.5V and output loading of one standard TTL gate plus 100pF.
4. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
5. Chip Select access time ($t_{CO}$) is longer for the Am9124 than for the Am9114. The specified address access time will be valid only when Chip Select is low soon enough for $t_{CO}$ to elapse.

## SWITCHING CHARACTERISTICS over operating range (Note 3)

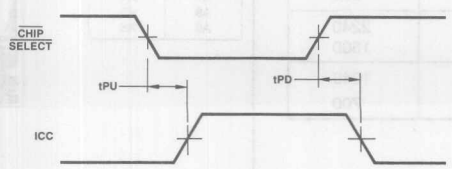
| Parameter | Description | | Am9114B Am9124B Min. | Am9114B Am9124B Max. | Am9114C Am9124C Min. | Am9114C Am9124C Max. | Am9114E Am9124E Min. | Am9114E Am9124E Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| **Read Cycle** | | | | | | | | | |
| tRC | Address Valid to Address Do Not Care Time (Read Cycle Time) | | 450 | | 300 | | 200 | | ns |
| tA | Address Valid to Data Out Valid Delay (Address Access Time) | | | 450 | | 300 | | 200 | |
| tCO | Chip Select Low to Data Out Valid (Note 5) | Am9114 | | 120 | | 100 | | 70 | |
| | | Am9124 | | 420 | | 280 | | 185 | |
| tCX | Chip Select Low to Data Out On | | 20 | | 20 | | 20 | | |
| tOTD | Chip Select High to Data Out Off | | | 100 | | 80 | | 60 | |
| tOHA | Address Unknown to Data Out Unknown Time | | 50 | | 50 | | 50 | | |
| **Write Cycle** | | | | | | | | | |
| tWC | Address Valid to Address Do Not Care Time (Write Cycle Time) | | 450 | | 300 | | 200 | | ns |
| tW | Write Enable Low to Write Enable High Time (Note 4) | Am9114 | 200 | | 150 | | 120 | | |
| | | Am9124 | 250 | | 200 | | 150 | | |
| tWR | Write Enable High to Address Do Not Care Time | | 0 | | 0 | | 0 | | |
| tOTW | Write Enable Low to Data Out Off Delay | | | 100 | | 80 | | 60 | |
| tDW | Data In Valid to Write Enable High Time | | 200 | | 150 | | 120 | | |
| tDH | Write Enable Low to Data In Do Not Care Time | | 0 | | 0 | | 0 | | |
| tAW | Address Valid to Write Enable Low Time | | 0 | | 0 | | 0 | | |
| tPD | Chip Select High to Power Low Delay (Am9124 only) | | | 200 | | 150 | | 100 | |
| tPU | Chip Select Low to Power High Delay (Am9124 only) | | 0 | | 0 | | 0 | | |
| tCW | Chip Select Low to Write Enable High Time (Note 4) | Am9114 | 200 | | 150 | | 120 | | |
| | | Am9124 | 250 | | 200 | | 150 | | |

## SWITCHING WAVEFORMS




MOS-068

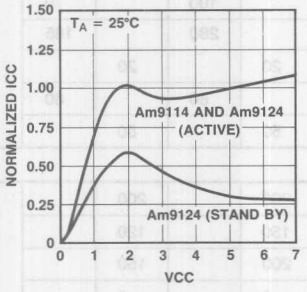
## POWER DOWN WAVEFORM (Am9124 ONLY)



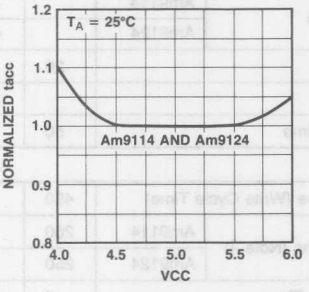

MOS-069

## TYPICAL CHARACTERISTICS

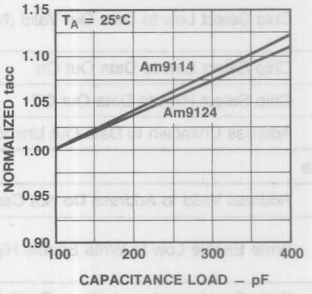
**Typical ICC Versus VCC Characteristics**



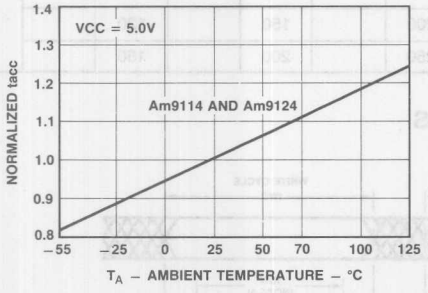

**Typical tacc Versus VCC Characteristics**



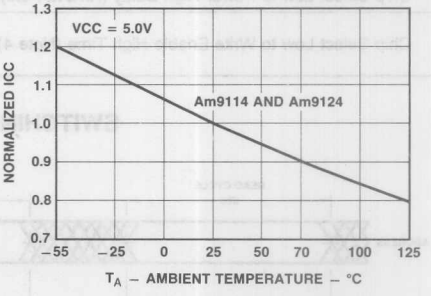

**Typical C Load Versus Normalized tacc Characteristics**




**Normalized tacc Versus Ambient Temperature**




**Normalized ICC Versus Ambient Temperature**




MOS-361

| Configuration | Part Number | Worst Case Current (mA at 0°C) 100% Duty Cycle | 50% Duty Cycle |
|---|---|---|---|
| 2K x 8 | 9114 | 280 | 280 |
| | 91L14 | 200 | 200 |
| | 9124 | 200 | 160 |
| | 91L24 | 140 | 110 |
| 4K x 12 | 9114 | 840 | 840 |
| | 91L14 | 600 | 600 |
| | 9124 | 480 | 420 |
| | 91L24 | 330 | 285 |
| 8K x 16 | 9114 | 2240 | 2240 |
| | 91L14 | 1600 | 1600 |
| | 9124 | 1120 | 1040 |
| | 91L24 | 760 | 700 |

Figure 1. Supply Current Advantages of Am9124.

**BIT MAP**

| Address Designators | |
|---|---|
| External | Internal |
| A0 | A9 |
| A1 | A8 |
| A2 | A7 |
| A3 | A0 |
| A4 | A1 |
| A5 | A2 |
| A6 | A3 |
| A7 | A4 |
| A8 | A5 |
| A9 | A6 |

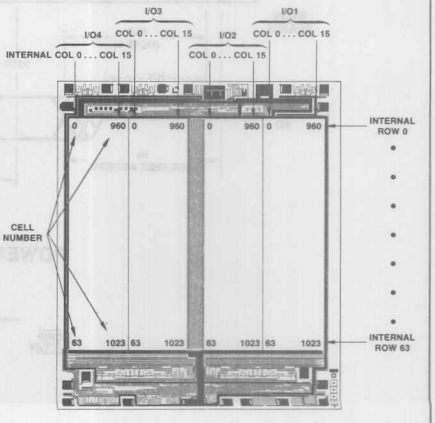



Figure 2. Bit Mapping Information.

# Am9130 • Am91L30

## 1024 x 4 Static R/W Random Access Memories

2

### DISTINCTIVE CHARACTERISTICS

- 1k x 4 organization
- Fully static data storage – no refreshing
- Single +5V power supply
- High-speed – access times down to 200ns max.
- Low operating power
  - 578mW max., 9130
  - 368mW max., 91L30
- Interface logic levels identical to TTL
- High noise immunity – 400mV worst-case
- High output drive – two standard TTL loads
- DC power-down mode – reduces power by >80%
- Single phase, low voltage, low capacitance clock
- Static clock may be stopped in either state
- Data register on-chip
- Address register on-chip
- Steady power drain – no large surges
- Unique Memory Status signal
  - improves performance
  - self clocking operation
- Full MIL temperature range available
- 100% MIL-STD-883 reliability assurance testing

### GENERAL DESCRIPTION

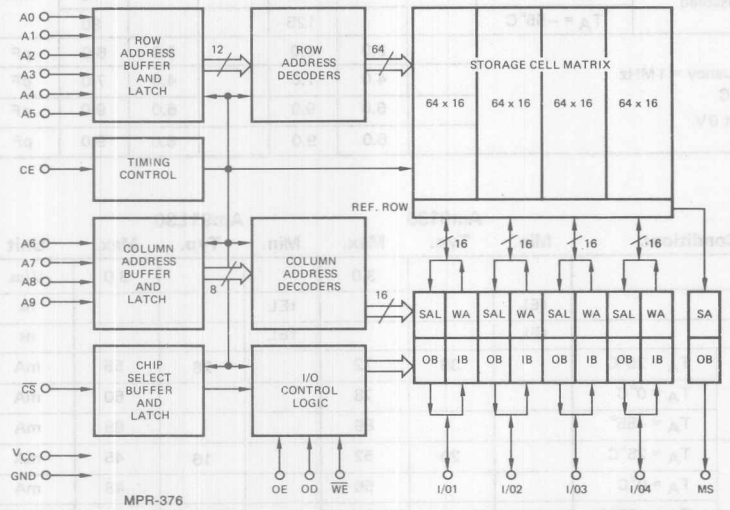
The Am9130 and Am91L30 products are high performance, adaptive, low-power, 4k-bit, static, read/write random access memories. They are implemented as 1024 words by 4 bits per word. Only a single +5V power supply is required for normal operation. A DC power-down mode reduces power while retaining data with a supply voltage as low as 1.5V.

All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive two full TTL loads or more than eight low-power Schottky loads.

Operational cycles are initiated when the Chip Enable clock goes HIGH. When the read or write is complete, Chip Enable goes LOW to preset the memory for the next cycle. Address and Chip Select signals are latched on-chip to simplify system timing. Output data is also latched and is available until the next operating cycle. The $\overline{WE}$ signal is HIGH for all read operations and is LOW during the Chip Enable time to perform a write. Data In and Data Out signals share common I/O pins.

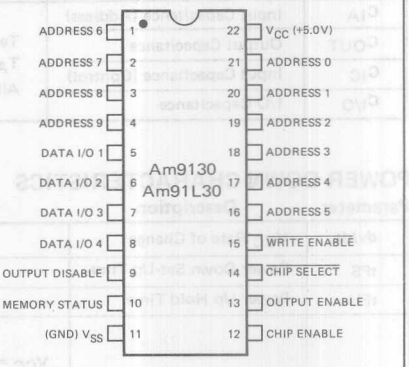
Memory Status is an output signal that indicates when data is actually valid and when the preset interval is complete. It can be used to generate the CE input and to improve the memory performance.

### BLOCK DIAGRAM




MPR-376

### CONNECTION DIAGRAM




Top View

Pin 1 is marked for orientation.

MPR-377

### ORDERING INFORMATION

| Package Type | Ambient Temperature | Power Type | Access Time | | | | |
|---|---|---|---|---|---|---|---|
| | | | 500ns | 400ns | 300ns | 250ns | 200ns |
| Molded | $0°C \leq T_A \leq +70°C$ | STD | AM9130APC | AM9130BPC | AM9130CPC | AM9130DPC | AM9130EPC |
| | | LOW | AM91L30APC | AM91L30BPC | AM91L30CPC | AM91L30DPC | |
| Hermetic DIP | $0°C \leq T_A \leq +70°C$ | STD | AM9130ADC | AM9130BDC | AM9130CDC | AM9130DDC | AM9130EDC |
| | | LOW | AM91L30ADC | AM91L30BDC | AM91L30CDC | AM91L30DDC | |
| | $-55°C \leq T_A \leq +125°C$ | STD | AM9130ADM | AM9130BDM | AM9130CDM | | |
| | | LOW | AM91L30ADM | AM91L30BDM | AM91L30CDM | | |

| | |
|---|---|
| $V_{CC}$ with Respect to $V_{SS}$ | −0.5 V to +7.0 V |
| All Signal Voltages with Respect to $V_{SS}$ | −0.5 V to +7.0 V |
| Power Dissipation | 1.25 W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

| OPERATING RANGE | | POWER-DOWN RANGE | | | |
|---|---|---|---|---|---|
| $V_{CC}$ | $V_{SS}$ | $V_{CC}$ | $V_{SS}$ | Ambient Temperature | Part Number |
| $4.75V \leq V_{CC} \leq 5.25V$ | 0V | $1.5V \leq V_{CC} \leq 5.25V$ | 0V | $0°C \leq T_A \leq +70°C$ | AM91X30XDC |
| $4.50V \leq V_{CC} \leq 5.50V$ | 0V | $1.5V \leq V_{CC} \leq 5.50V$ | 0V | $-55°C \leq T_A \leq +125°C$ | AM91X30XDM |

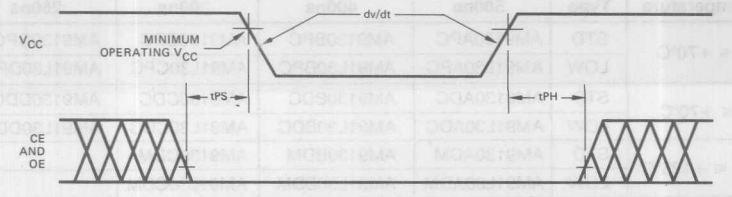
## ELECTRICAL CHARACTERISTICS over operating range (Note 1)

| Parameters | Description | Test Conditions | | Am9130 Min. | Am9130 Typ. | Am9130 Max. | Am91L30 Min. | Am91L30 Typ. | Am91L30 Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -200\mu A$ | $V_{CC} = 4.75V$ | 2.4 | | | 2.4 | | | Volts |
| | | | $V_{CC} = 4.5V$ | 2.2 | | | 2.2 | | | |
| $V_{OL}$ | Output LOW Voltage | $I_{OL} = 3.2mA$ | | | | 0.4 | | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | | $V_{CC}$ | 2.0 | | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Voltage | | | −0.5 | | 0.8 | −0.5 | | 0.8 | Volts |
| $I_{LI}$ | Input Load Current | $V_{SS} \leq V_{IN} \leq V_{CC}$ | | | | 10 | | | 10 | μA |
| $I_{LO}$ | Output Leakage Current | $V_{SS} \leq V_{OUT} \leq V_{CC}$, Output disabled | | | | 10 | | | 10 | μA |
| $I_{CC}$ | $V_{CC}$ Supply Current | Max. $V_{CC}$, Output disabled | $T_A = 25°C$ | | 50 | 100 | | 40 | 65 | mA |
| | | | $T_A = 0°C$ | | | 110 | | | 70 | |
| | | | $T_A = -55°C$ | | | 125 | | | 80 | |
| $C_{IA}$ | Input Capacitance (Address) | Test frequency = 1 MHz, $T_A = 25°C$, All pins at 0V | | | 3.0 | 6.0 | | 3.0 | 6.0 | pF |
| $C_{OUT}$ | Output Capacitance | | | | 4.0 | 7.0 | | 4.0 | 7.0 | pF |
| $C_{IC}$ | Input Capacitance (Control) | | | | 6.0 | 9.0 | | 6.0 | 9.0 | pF |
| $C_{I/O}$ | I/O Capacitance | | | | 6.0 | 9.0 | | 6.0 | 9.0 | pF |

## POWER DOWN CHARACTERISTICS

| Parameter | Description | Test Conditions | | Am9130 Min. | Am9130 Typ. | Am9130 Max. | Am91L30 Min. | Am91L30 Typ. | Am91L30 Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| dv/dt | $V_{CC}$ Rate of Change | | | | | 3.0 | | | 3.0 | V/μs |
| tPS | Power Down Set-Up Time | | | tEL | | | tEL | | | ns |
| tPH | Power Up Hold Time | | | tEL | | | tEL | | | ns |
| $I_{PD}$ | $I_{CC}$ in Standby (Note 2) | $V_{CC} = 2.0V$ | $T_A = 25°C$ | | 36 | 72 | | 28 | 55 | mA |
| | | | $T_A = 0°C$ | | | 78 | | | 60 | mA |
| | | | $T_A = -55°$ | | | 89 | | | 68 | mA |
| | | $V_{CC} = 1.5V$ | $T_A = 25°C$ | | 20 | 52 | | 16 | 45 | mA |
| | | | $T_A = 0°C$ | | | 56 | | | 48 | mA |
| | | | $T_A = -55°C$ | | | 64 | | | 55 | mA |

### POWER DOWN WAVEFORM




MPR-378

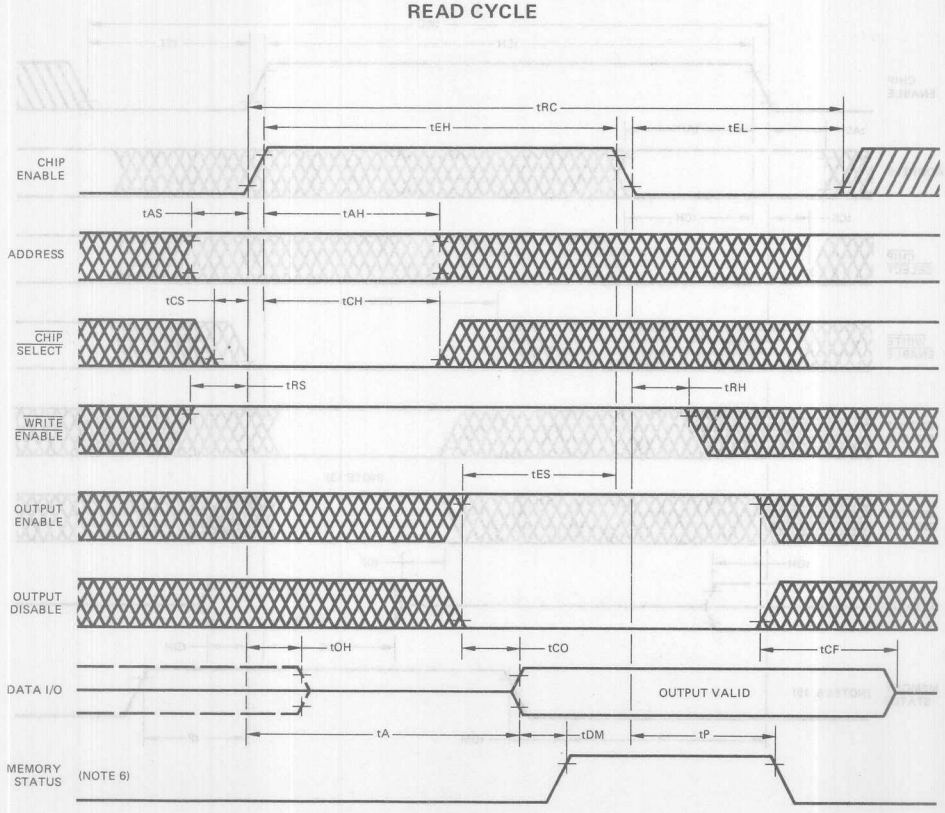
## SWITCHING CHARACTERISTICS over operating range

**READ CYCLE** (Notes 7, 8, 9)

| Parameter | Description | Am9130A / Am91L30A Min. | Am9130A / Am91L30A Max. | Am9130B / Am91L30B Min. | Am9130B / Am91L30B Max. | Am9130C / Am91L30C Min. | Am9130C / Am91L30C Max. | Am9130D / Am91L30D Min. | Am9130D / Am91L30D Max. | Am9130E Min. | Am9130E Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| tRC | Read Cycle Time (Note 5) | 770 | | 620 | | 470 | | 395 | | 320 | | ns |
| tA | Access Time (Note 3) (CE to Output Valid Delay) | | 500 | | 400 | | 300 | | 250 | | 200 | ns |
| tEH | Chip Enable HIGH Time (Note 14) | 500 | | 400 | | 300 | | 250 | | 200 | | ns |
| tEL | Chip Enable LOW Time (Note 14) | 250 | | 200 | | 150 | | 125 | | 100 | | ns |
| tCH | Chip Enable to Chip Select Hold Time | 200 | | 170 | | 150 | | 130 | | 120 | | ns |
| tAH | Chip Enable to Address Hold Time | 200 | | 170 | | 150 | | 130 | | 120 | | ns |
| tCS | Chip Select to CE Set-Up Time (Note 4) | –5 | | –5 | | –5 | | –5 | | –5 | | ns |
| tAS | Address to Chip Enable Set-Up Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tRS | Read to Chip Enable Set-Up Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tRH | Chip Enable to Read Hold Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tOH | Chip Enable to Output OFF Delay (Note 3) | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tCF | OE or OD to Output OFF Delay (Note 11) | | 200 | | 165 | | 135 | | 115 | | 100 | ns |
| tCO | OE or OD to Output ON Delay (Note 11) | | 220 | | 185 | | 150 | | 125 | | 110 | ns |
| tES | Output Enable to CE LOW Set-Up Time (Note 12) | 90 | | 75 | | 60 | | 55 | | 50 | | ns |
| tDM | Data Out to Memory Status Delay | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tP | Internal Preset Interval (Note 14) | | tEL | | tEL | | tEL | | tEL | | tEL | ns |

## SWITCHING WAVEFORMS

### READ CYCLE




MPR-379

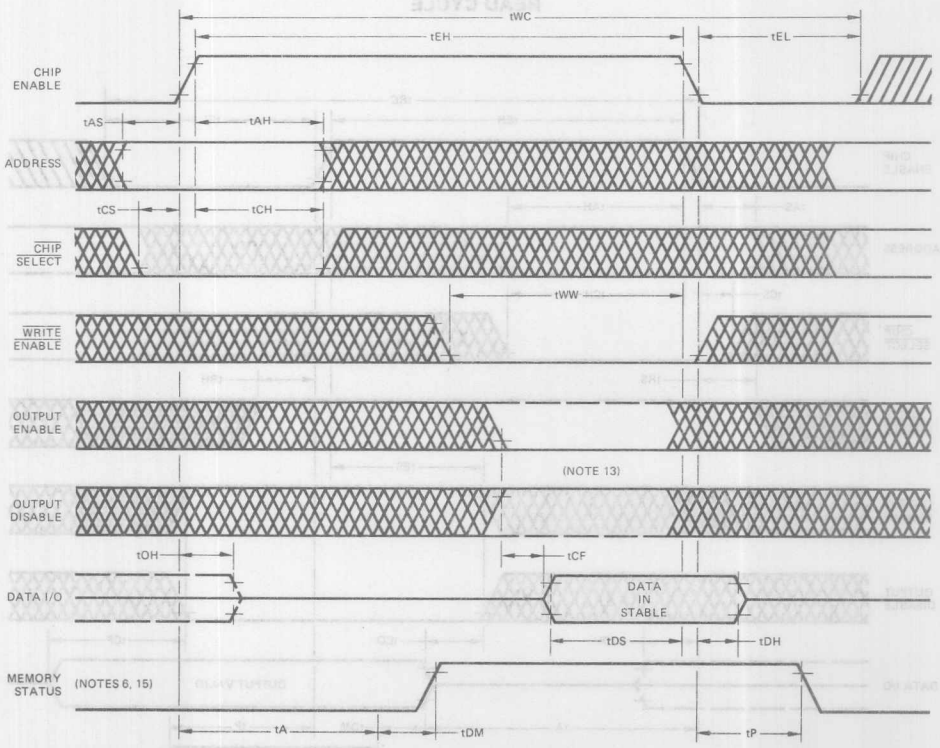
## SWITCHING CHARACTERISTICS over operating range

**WRITE CYCLE** (Notes 7, 8, 9)

| Parameter | Description | Am9130A Am91L30A Min. | Am9130A Am91L30A Max. | Am9130B Am91L30B Min. | Am9130B Am91L30B Max. | Am9130C Am91L30C Min. | Am9130C Am91L30C Max. | Am9130D Am91L30D Min. | Am9130D Am91L30D Max. | Am9130E Min. | Am9130E Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| tWC | Write Cycle Time (Note 5) | 770 | | 620 | | 470 | | 395 | | 320 | | ns |
| tA | Access Time (CE to Output ON Delay) | | 500 | | 400 | | 300 | | 250 | | 200 | ns |
| tEH | Chip Enable HIGH Time (Notes 14, 15) | 500 | | 400 | | 300 | | 250 | | 200 | | ns |
| tEL | Chip Enable LOW Time (Notes 14, 15) | 250 | | 200 | | 150 | | 125 | | 100 | | ns |
| tAS | Address to Chip Enable Set-Up Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tAH | Chip Enable to Address Hold Time | 200 | | 170 | | 150 | | 130 | | 120 | | ns |
| tCS | Chip Select to CE Set-Up Time (Note 4) | –5 | | –5 | | –5 | | –5 | | – 5 | | ns |
| tCH | Chip Enable to Chip Select Hold Time | 200 | | 170 | | 150 | | 130 | | 120 | | ns |
| tWW | Write Pulse Width (Note 10) | 200 | | 165 | | 135 | | 115 | | 100 | | ns |
| tDS | Data Input Set-Up Time (Note 10) | 200 | | 165 | | 135 | | 115 | | 100 | | ns |
| tDH | Data Input Hold Time (Note 10) | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tDM | Data Out to Memory Status Delay | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tP | Internal Preset Interval | | tEL | | tEL | | tEL | | tEL | | tEL | ns |

## SWITCHING WAVEFORMS

**WRITE CYCLE**




MPR-380

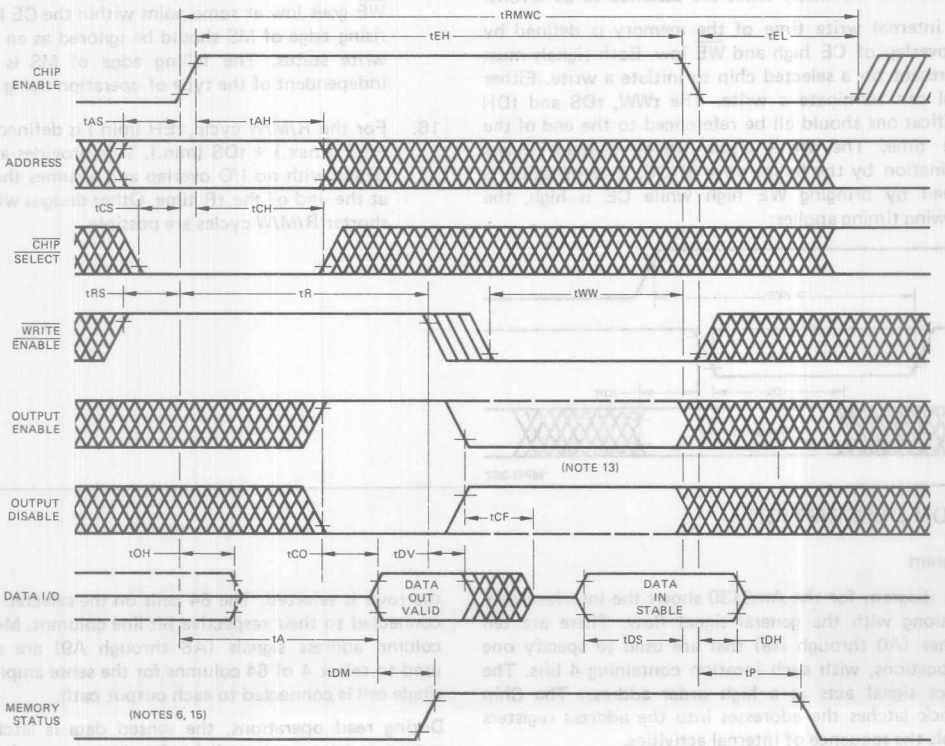
## SWITCHING CHARACTERISTICS over operating range

### READ/MODIFY/WRITE CYCLE (Notes 7, 8, 9)

| Parameter | Description | Am9130A Am91L30A Min. | Am9130A Am91L30A Max. | Am9130B Am91L30B Min. | Am9130B Am91L30B Max. | Am9130C Am91L30C Min. | Am9130C Am91L30C Max. | Am9130D Am91L30D Min. | Am9130D Am91L30D Max. | Am9130E Min. | Am9130E Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| tRMWC | R/M/W Cycle Time (Notes 5, 16) | 1170 | | 950 | | 740 | | 625 | | 520 | | ns |
| tA | Access Time (CE to Output Valid Delay) | | 500 | | 400 | | 300 | | 250 | | 200 | ns |
| tEH | Chip Enable HIGH Time (Notes 14, 15) | 900 | | 730 | | 570 | | 480 | | 400 | | ns |
| tEL | Chip Enable LOW Time (Notes 14, 15) | 250 | | 200 | | 150 | | 125 | | 100 | | ns |
| tCH | Chip Enable to Chip Select Hold Time | 200 | | 170 | | 150 | | 130 | | 120 | | ns |
| tAH | Chip Enable to Address Hold Time | 200 | | 170 | | 150 | | 130 | | 120 | | ns |
| tCS | Chip Select to CE Set-Up Time (Note 4) | –5 | | –5 | | –5 | | –5 | | – 5 | | ns |
| tAS | Address to Chip Enable Set-Up Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tRS | Read to Chip Enable Set-Up Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tOH | Chip Enable to Output OFF Delay | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tDH | Data Input Hold Time (Note 10) | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tDS | Data Input Set-Up Time (Note 10) | 200 | | 165 | | 135 | | 115 | | 100 | | ns |
| tWW | Write Pulse Width (Note 10) | 200 | | 165 | | 135 | | 115 | | 100 | | ns |
| tCF | OE or OD to Output OFF Delay (Note 11) | | 200 | | 165 | | 135 | | 115 | | 100 | ns |
| tCO | OE or OD to Output ON Delay (Note 11) | | 220 | | 185 | | 150 | | 125 | | 110 | ns |
| tDV | Data Valid after Write Delay | 10 | | 10 | | 10 | | 10 | | 10 | | ns |
| tR | Read Mode Hold Time | tA | | tA | | tA | | tA | | tA | | ns |
| tDM | Data Out to Memory Status Delay | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tP | Internal Preset Interval | | tEL | | tEL | | tEL | | tEL | | tEL | ns |

## SWITCHING CHARACTERISTICS

### READ/MODIFY/WRITE CYCLE




MPR-381

nominal processing parameters, nominal supply voltage and the specific ambient temperature shown.

2. Typical power-down supply current values are specified for nominal processing parameters, the specific supply voltage shown and the specific ambient temperature shown.

3. At any operating temperature the minimum access time, tA(min.), will be greater than the maximum CE to output OFF delay, tOH(max.).

4. The negative value shown indicates that the Chip Select input may become valid as late as 5ns following the start of the Chip Enable rising edge.

5. The worst-case cycle times are the sum of CE rise time, tEH, CE fall time and tEL. The cycle time values shown include the worst-case tEH and tEL requirements and assume CE transition times of 10ns.

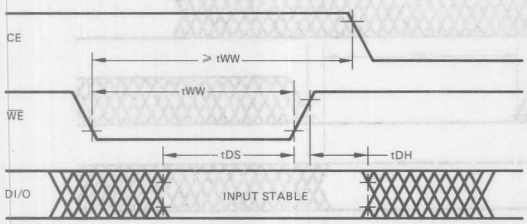
6. The Memory Status signal is a two-state output and is not affected by the Output Disable or Output Enable signals. If the output data buffers are turned off, Memory Status will continue to reflect the internal status of the memory.

7. Output loading is assumed to be one standard TTL gate plus 50pF of capacitance.

8. Timing reference levels for both input and output signals are 0.8V and 2.0V.

9. CE and $\overline{WE}$ transition times are assumed to be $\leqslant$10ns.

10. The internal write time of the memory is defined by the overlap of CE high and $\overline{WE}$ low. Both signals must be present on a selected chip to initiate a write. Either signal can terminate a write. The tWW, tDS and tDH specifications should all be referenced to the end of the write time. The Write Cycle timing diagram shows termination by the falling edge of CE. If termination is defined by bringing $\overline{WE}$ high while CE is high, the following timing applies:



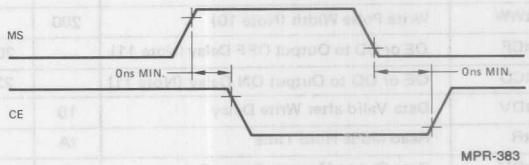

MPR-382

valid only when Output Enable is high and Output Disable is low. OE and OD perform the same function with opposite control polarity.

12. The output data buffer should be enabled before the falling edge of CE in order to read output information. When the output is disabled and CE is low, the output data register is cleared.

13. Input and output data are the same polarity.

14. The Chip Enable waveform requirements may be defined by the Memory Status output waveform. For a read cycle, the basic CE requirement is that tEH $\geqslant$ tA and tEL $\geqslant$ tP:




MPR-383

15. The Memory Status output functions as if all operations are read cycles. If a write cycle begins with $\overline{WE}$ low and Data In stable at the time CE goes high, the rising edge of MS may be used as an indication that the write is complete and CE may be brought low. In a cycle where $\overline{WE}$ goes low at some point within the CE high time, the rising edge of MS should be ignored as an indication of write status. The falling edge of MS is always valid independent of the type of operation being performed.

16. For the R/M/W cycle, tEH (min.) is defined as tR (min.) +tCF (max.) + tDS (min.). This provides a conservative design with no I/O overlap and assumes that tCF begins at the end of the tR time. Other designs with somewhat shorter R/M/W cycles are possible.

## FUNCTION DESCRIPTION

### Block Diagram

The block diagram for the Am9130 shows the interface connections along with the general signal flow. There are ten address lines (A0 through A9) that are used to specify one of 1024 locations, with each location containing 4 bits. The Chip Select signal acts as a high order address. The Chip Enable clock latches the addresses into the address registers and controls the sequence of internal activities.

The row address signals (A0 through A5) and their inversions are distributed to the 64 row address decoders where one of the rows is selected. The 64 cells on the selected row are then connected to their respective bit line columns. Meanwhile, the column address signals (A6 through A9) are decoded and used to select 4 of 64 columns for the sense amplifiers. Thus a single cell is connected to each output path.

During read operations, the sensed data is latched into the output register and is available for the balance of the operating cycle. During write operations, the write amplifier is turned on and drives the input data onto the sense lines, up the column

bit lines and into the selected cell. Read and write data are the same polarity.

The data buffer is three-state and unselected chips have their outputs turned off so that several may be wire-ored together. The Output Enable and Output Disable signals provide asynchronous controls for turning off the output buffers.

Within the storage matrix there is an extra row of simulated cells. This reference row is selected on every operating cycle in addition to the addressed row and provides internal timing signals that control the data flow through the memory. The Memory Status output signal is derived from the reference row and uses the same designs for its sense and buffer circuits as used by the data bits.

### Chip Enable

The Chip Enable input is a control clock that coordinates all internal activities. The rising edge of CE begins each cycle and strobes the Address and Chip Select signals into the on-chip register. Internal timing signals are derived from CE and from transitions of the address latches and the reference cells.

When the actual access time of the part has been reached (or a write operation is complete), CE may be switched low if desired. The worst-case time as specified in the data sheet may be used to determine the access. Alternatively, the access or write-complete time indicated by the rising edge of the Memory Status output signal may be used.

When CE goes low, the internal preset operation begins. The memory is ready for a new cycle only after the preset is complete. The worst-case CE low time specified in the data sheet may be used to determine the preset interval. Alternatively, the actual preset time is indicated as complete when Memory Status goes low.

There are no restrictions on the maximum times that CE may remain in either state so the clock may be extended or stopped whenever convenient. After power-on and before beginning a valid operation, the clock should be brought low to initially preset the memory.

### Address and Chip Select

The Address inputs are latched into the on-chip address register by the rising edge of CE. Addresses must be held stable for the specified minimum time following the rising edge of CE in order to be properly loaded into the register. Following the address hold time, the address inputs are ignored by the memory until the next cycle is initiated.

The Chip Select input acts as a high order address for use when the system word capacity is larger than that of an individual chip. It allows the Address lines to be wired in parallel to all chips with the CS lines then used to select one active row of chips at a time. Unselected chips have their output buffers off so that selected chips wired to the same data lines can dominate the output bus. Only selected chips can perform write operations.

CS is latched in the same way that Addresses are. Once a memory is selected or deselected, it will remain that way until a new cycle with new select information begins.

### Write Enable

The Write Enable line controls the read or write condition of the devices. When the CE clock is low, the WE signal may be in any state without affecting the memory. WE does not affect the status of the output buffer.

To execute a read cycle, WE is held high while CE is high. To perform a write operation, the WE line is switched low while CE is high. Only a narrow write pulse width is required to successfully write into a cell. In many cases, however, it will be convenient to leave the WE line low during the whole cycle.

A write cycle can take place only when three conditions are met: The chip is selected, CE is high, and WE is low. This means that if either CE goes low or WE goes high, the writing is terminated.

### Data In and Data Out

The requirements for incoming data during a write operation show a minimum set-up time with respect to the termination of the write. Termination occurs when either WE goes high or CE goes low. If incoming data changes during a write operation, the information finally written in the cell will be that stable data preceeding the termination by the set-up time. Since the data being written during a write cycle is impressed on the sense amplifier inputs, the output data will be the same as the input once the write is established.

During a read cycle, once all of the addressing is complete and the cell information has propagated through the sense amplifier, it enters the output data register. The read information can also flow through to the output if the buffer is enabled. As long as CE is high, the addressing remains valid and the output data will be stable. When CE goes low to begin the internal preset operation, the output information is latched into the data register. It will remain latched and stable as long as CE is low. If the output is disabled when CE is low, the output data register is cleared. At the start of every cycle when CE goes high, the output data latch is cleared in preparation for new information to come from the sense amplifier, and the output buffer is turned off.

OE and OD are designed to provide asynchronous control of the output buffer independent of the synchronous Chip Select control. The OE and OD control lines perform the same internal function except that one is inverted from the other. If either OE is low or OD is high, the output buffer will turn off. If the CS input is latched low and OE is high and OD is low, then the output buffer can turn on when data is available.

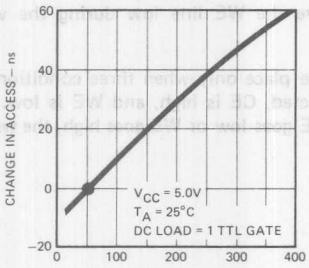
### Memory Status

The Memory Status output is derived from the actual performance of the reference row of cells. Since the reference row is always doing a read operation, the MS output will appear in every operating cycle, whether a read or write is being performed. MS uses the same output circuitry as used in the data path. The result is that Memory Status tracks very closely the true operating performance of the memory.

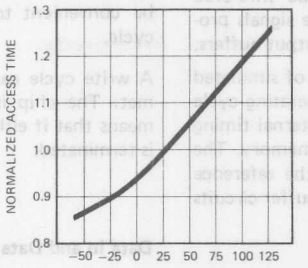
The rising edge of MS indicates when output data is valid and tracks changes in access time with changing operating conditions. The rising edge also specifies the end of the time that CE must be held high for a read. CE may be high as long as desired, but may safely go low any time after MS goes high. The falling edge of MS occurs after CE goes low and the internal preset period is complete. It indicates that CE may go high to begin a new cycle. See the Am9130/40 Application Note for details.

## CHARACTERISTICS

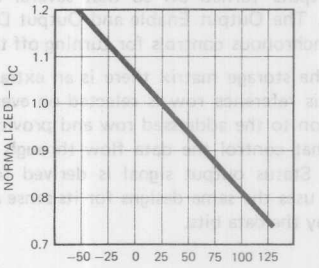
### Access Change Versus Capacitive Load



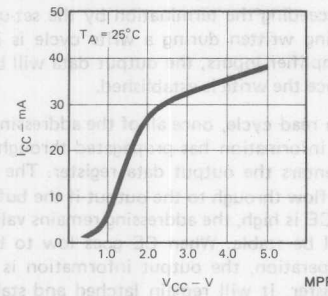

### Access Time Versus Ambient Temperature



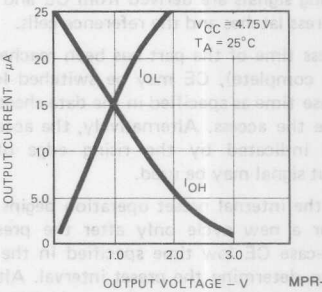

### Supply Current Versus Ambient Temperature



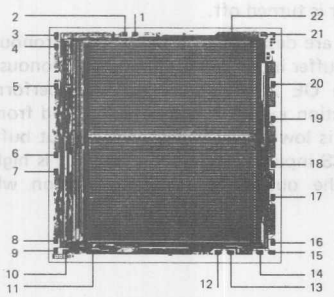

### Typical $I_{CC}$ Versus $V_{CC}$




### Typical Output Currents Versus Output Voltage

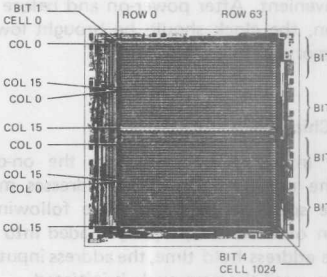



### Metallization and Pad Layout




DIE SIZE 0.192" X 0.197"

### Bit Map




For bit mapping purposes:
Row address LSB = A5, MSB = A0
Column address LSB = A6, MSB = A9

# Am9131 • Am91L31

## 1024 x 4 Static R/W Random Access Memories

2

### DISTINCTIVE CHARACTERISTICS

- 1k X 4 organization
- Fully static data storage — no refreshing
- Single +5V power supply
- High-speed — access times down to 200ns max.
- Low operating power
  - 578mW max., 9131
  - 368mW max., 91L31
- Interface logic levels identical to TTL
- High noise immunity — 400mV worst-case
- High output drive — two standard TTL loads
- DC power-down mode — reduces power by >80%
- Single phase, low voltage, low capacitance clock
- Static clock may be stopped in either state
- Data register on-chip
- Address register on-chip
- Steady power drain — no large surges
- Full MIL temperature range available
- 100% MIL-STD-883 reliability assurance testing

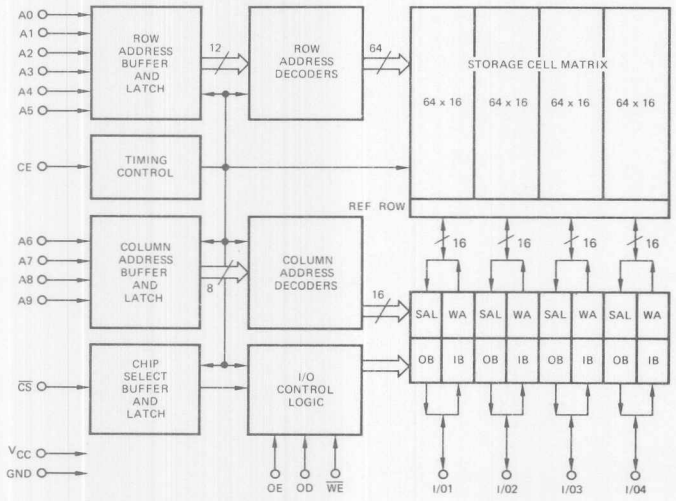
### GENERAL DESCRIPTION

The Am9131 and Am91L31 products are high performance, low-power, 4k-bit, static, read/write random access memories. They are implemented as 1024 words by 4 bits per word. Only a single +5V power supply is required for normal operation. A DC power-down mode reduces power while retaining data with a supply voltage as low as 1.5V.

All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive two full TTL loads or more than eight low-power Schottky loads.

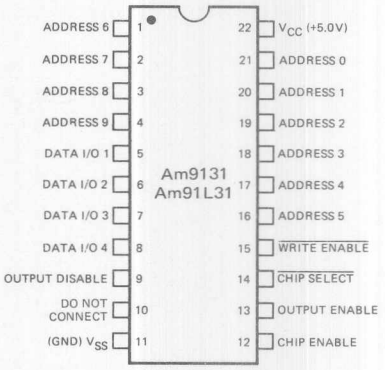
Operational cycles are initiated when the Chip Enable clock goes HIGH. When the read or write is complete, Chip Enable goes LOW to preset the memory for the next cycle. Address and Chip Select signals are latched on-chip to simplify system timing. Output data is also latched and is available until the next operating cycle. The $\overline{WE}$ signal is HIGH for all read operations and is LOW during the Chip Enable time to perform a write. Data In and Data Out signals share common I/O pins.

### BLOCK DIAGRAM




MOS-362

### CONNECTION DIAGRAM




**Top View**

Pin 1 is marked for orientation.

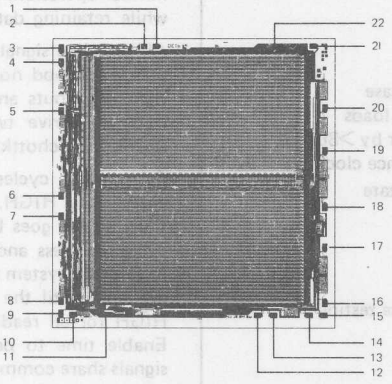
MOS-363

### ORDERING INFORMATION

| Package Type | Ambient Temperature | Power Type | Access Time | | | | |
|---|---|---|---|---|---|---|---|
| | | | 500ns | 400ns | 300ns | 250ns | 200ns |
| Hermetic DIP | $0°C \leq T_A \leq +70°C$ | STD | Am9131ADC | Am9131BDC | Am9131CDC | Am9131DDC | Am9131EDC |
| | | LOW | Am91L31ADC | Am91L31BDC | Am91L31CDC | Am91L31DDC | |
| | $-55°C \leq T_A \leq +125°C$ | STD | Am9131ADM | Am9131BDM | Am9131CDM | | |
| | | LOW | Am91L31ADM | Am91L31BDM | Am91L31CDM | | |

The Am9131 and Am91L31 memories are identical in every respect to their counterparts in the Am9130 and Am91L30 family, with the single exception that the Memory Status output is not functional. Pin 10 on the Am9131/L31 products should not be used and should not be connected to any external circuit. Please refer to the Am9130/L30 data sheet for the electrical and switching characteristics of the Am9131/L31.

**Metallization and Pad Layout**




DIE SIZE 0.192" x 0.197"

# Am9140 • Am91L40

## 4096 x 1 Static R/W Random Access Memories

2

### DISTINCTIVE CHARACTERISTICS

- 4k x 1 organization
- Fully static data storage – no refreshing
- Single +5V power supply
- High-speed – access times down to 200ns max.
- Low operating power
  - 578mW max., 9140
  - 368mW max., 91L40
- Interface logic levels identical to TTL
- High noise immunity – 400mV worst-case
- High output drive – two standard TTL loads
- DC power-down mode – reduces power by >80%
- Single phase, low voltage, low capacitance clock
- Static clock may be stopped in either state
- Data register on-chip
- Address register on-chip
- Steady power drain – no large surges
- Unique Memory Status signal
  - improves performance
  - self clocking operation
- Full MIL temperature range available
- 100% MIL-STD-883 reliability assurance testing

### GENERAL DESCRIPTION

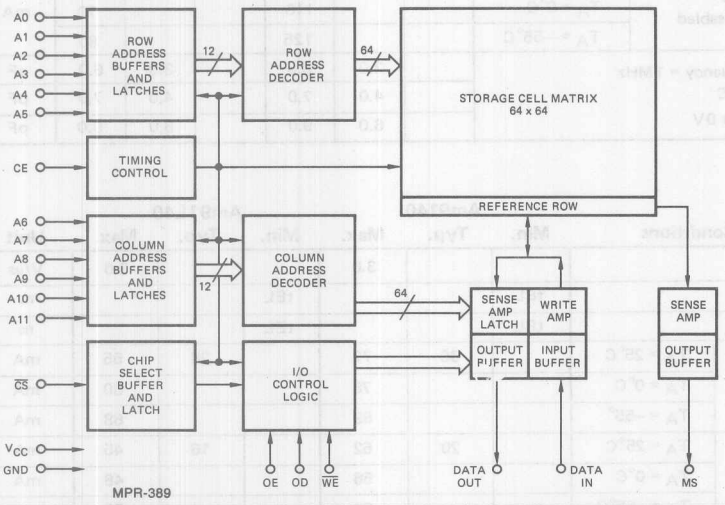
The Am9140 and Am91L40 products are high performance, adaptive, low-power, 4k-bit, static, read/write random access memories. They are implemented as 4096 words by 1 bits per word. Only a single +5V power supply is required for normal operation. A DC power-down mode reduces power while retaining data with a supply voltage as low as 1.5V.

All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive two full TTL loads or more than eight low-power Schottky loads.

Operational cycles are initiated when the Chip Enable clock goes HIGH. When the read or write is complete, Chip Enable goes LOW to preset the memory for the next cycle. Address and Chip Select signals are latched on-chip to simplify system timing. Output data is also latched and is available until the next operating cycle. The $\overline{WE}$ signal is HIGH for all read operations and is LOW during the Chip Enable time to perform a write.

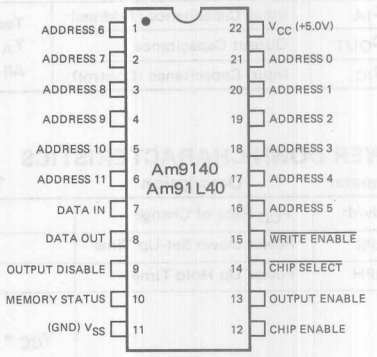
Memory Status is an output signal that indicates when data is actually valid and when the preset interval is complete. It can be used to generate the CE input and to improve the memory performance.

### BLOCK DIAGRAM




MPR-389

### CONNECTION DIAGRAM




**Top View**

Pin 1 is marked for orientation.

MPR-390

### ORDERING INFORMATION

| Package Type | Power Ambient Temperature | Type | Access Time 500ns | 400ns | 300ns | 250ns | 200ns |
|---|---|---|---|---|---|---|---|
| Molded | $0°C \leq T_A \leq +70°C$ | STD | AM9140APC | AM9140BPC | AM9140CPC | AM9140DPC | AM9140EPC |
| | | LOW | AM91L40APC | AM91L40BPC | AM91L40CPC | AM91L40DPC | |
| Hermetic DIP | $0°C \leq T_A \leq +70°C$ | STD | AM9140ADC | AM9140BDC | AM9140CDC | AM9140DDC | AM9140EDC |
| | | LOW | AM91L40ADC | AM91L40BDC | AM91L40CDC | AM91L40DDC | |
| | $-55°C \leq T_A \leq +125°C$ | STD | AM9140ADM | AM9140BDM | AM9140CDM | | |
| | | LOW | AM91L40ADM | AM91L40BDM | AM91L40CDM | | |

## MAXIMUM RATINGS above which the useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| $V_{CC}$ with Respect to $V_{SS}$ | −0.5V to +7.0V |
| All Signal Voltages with Respect to $V_{SS}$ | −0.5V to +7.0V |
| Power Dissipation | 1.25W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

| OPERATING RANGE | | POWER DOWN RANGE | | | |
|---|---|---|---|---|---|
| $V_{CC}$ | $V_{SS}$ | $V_{CC}$ | $V_{SS}$ | Ambient Temperature | Part Number |
| $4.75V \leq V_{CC} \leq 5.25V$ | 0V | $1.5V \leq V_{CC} \leq 5.25V$ | 0V | $0°C \leq T_A \leq +70°C$ | AM91X40XDC |
| $4.50V \leq V_{CC} \leq 5.50V$ | 0V | $1.5V \leq V_{CC} \leq 5.50V$ | 0V | $-55°C \leq T_A \leq +125°C$ | AM91X40XDM |

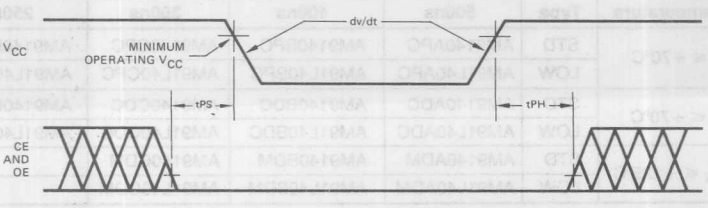
## ELECTRICAL CHARACTERISTICS over operating range (Note 1)

| Parameters | Description | Test Conditions | | Am9140 Min. | Am9140 Typ. | Am9140 Max. | Am91L40 Min. | Am91L40 Typ. | Am91L40 Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -200\mu A$ | $V_{CC} = 4.75V$ | 2.4 | | | 2.4 | | | Volts |
| | | | $V_{CC} = 4.5V$ | 2.2 | | | 2.2 | | | |
| $V_{OL}$ | Output LOW Voltage | $I_{OL} = 3.2mA$ | | | | 0.4 | | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | | $V_{CC}$ | 2.0 | | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Voltage | | | −0.5 | | 0.8 | −0.5 | | 0.8 | Volts |
| $I_{LI}$ | Input Load Current | $V_{SS} \leq V_{IN} \leq V_{CC}$ | | | | 10 | | | 10 | $\mu A$ |
| $I_{LO}$ | Output Leakage Current | $V_{SS} \leq V_{OUT} \leq V_{CC}$, Output disabled | | | | 10 | | | 10 | $\mu A$ |
| $I_{CC}$ | $V_{CC}$ Supply Current | Max. $V_{CC}$, Output disabled | $T_A = 25°C$ | | 50 | 100 | | 40 | 65 | mA |
| | | | $T_A = 0°C$ | | | 110 | | | 70 | |
| | | | $T_A = -55°C$ | | | 125 | | | 80 | |
| $C_{IA}$ | Input Capacitance (Address) | Test frequency = 1 MHz, $T_A = 25°C$, All pins at 0V | | | 3.0 | 6.0 | | 3.0 | 6.0 | pF |
| $C_{OUT}$ | Output Capacitance | | | | 4.0 | 7.0 | | 4.0 | 7.0 | pF |
| $C_{IC}$ | Input Capacitance (Control) | | | | 6.0 | 9.0 | | 6.0 | 9.0 | pF |

## POWER DOWN CHARACTERISTICS

| Parameter | Description | Test Conditions | | Am9140 Min. | Am9140 Typ. | Am9140 Max. | Am91L40 Min. | Am91L40 Typ. | Am91L40 Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| dv/dt | $V_{CC}$ Rate of Change | | | | | 3.0 | | | 3.0 | V/μs |
| tPS | Power Down Set-Up Time | | | tEL | | | tEL | | | ns |
| tPH | Power Up Hold Time | | | tEL | | | tEL | | | ns |
| $I_{PD}$ | $I_{CC}$ in Standby (Note 2) | $V_{CC} = 2.0V$ | $T_A = 25°C$ | | 36 | 72 | | 28 | 55 | mA |
| | | | $T_A = 0°C$ | | | 78 | | | 60 | mA |
| | | | $T_A = -55°$ | | | 89 | | | 68 | mA |
| | | $V_{CC} = 1.5V$ | $T_A = 25°C$ | | 20 | 52 | | 16 | 45 | mA |
| | | | $T_A = 0°C$ | | | 56 | | | 48 | mA |
| | | | $T_A = -55°C$ | | | 64 | | | 55 | mA |

### POWER DOWN WAVEFORM




MPR-391

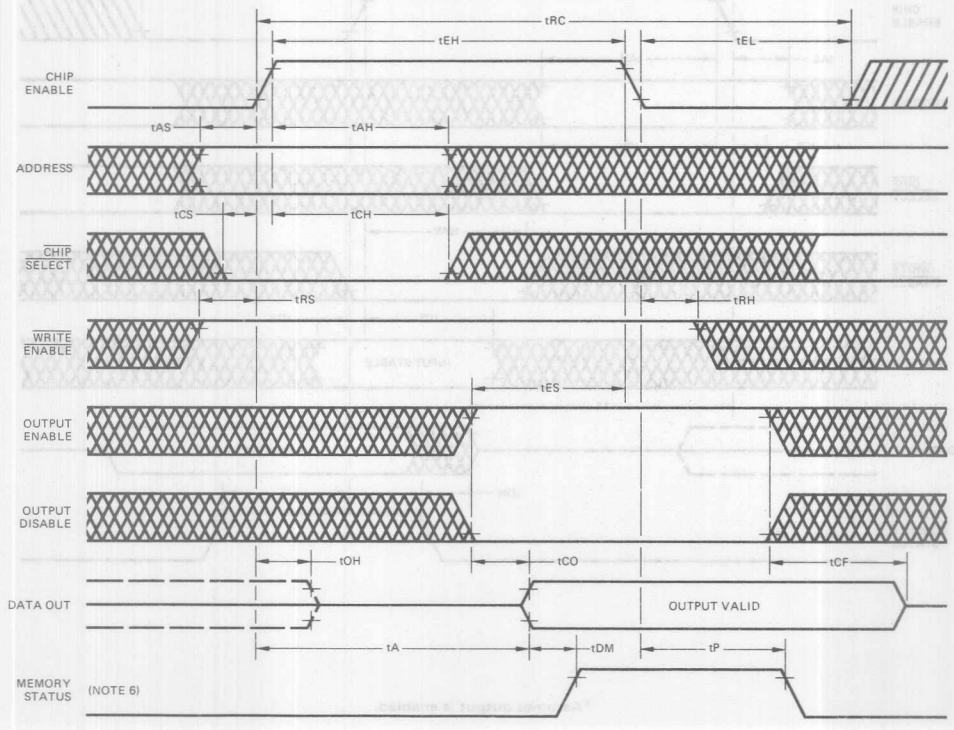
## SWITCHING CHARACTERISTICS over operating range

**READ CYCLE** (Notes 7, 8, 9)

| Parameter | Description | Am9140A Am91L40A Min. | Am9140A Am91L40A Max. | Am9140B Am91L40B Min. | Am9140B Am91L40B Max. | Am9140C Am91L40C Min. | Am9140C Am91L40C Max. | Am9140D Am91L40D Min. | Am9140D Am91L40D Max. | Am9140E Min. | Am9140E Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| tRC | Read Cycle Time (Note 5) | 770 | | 620 | | 470 | | 395 | | 320 | | ns |
| tA | Access Time (Note 3) (CE to Output Valid Delay) | | 500 | | 400 | | 300 | | 250 | | 200 | ns |
| tEH | Chip Enable HIGH Time (Note 14) | 500 | | 400 | | 300 | | 250 | | 200 | | ns |
| tEL | Chip Enable LOW Time (Note 14) | 250 | | 200 | | 150 | | 125 | | 100 | | ns |
| tCH | Chip Enable to Chip Select Hold Time | 200 | | 170 | | 150 | | 130 | | 120 | | ns |
| tAH | Chip Enable to Address Hold Time | 200 | | 170 | | 150 | | 130 | | 120 | | ns |
| tCS | Chip Select to CE Set-Up Time (Note 4) | –5 | | –5 | | –5 | | –5 | | –5 | | ns |
| tAS | Address to Chip Enable Set-Up Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tRS | Read to Chip Enable Set-Up Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tRH | Chip Enable to Read Hold Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tOH | Chip Enable to Output OFF Delay (Note 3) | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tCF | OE or OD to Output OFF Delay (Note 11) | | 200 | | 165 | | 135 | | 115 | | 100 | ns |
| tCO | OE or OD to Output ON Delay (Note 11) | | 220 | | 185 | | 150 | | 125 | | 110 | ns |
| tES | Output Enable to CE LOW Set-Up Time (Note 12) | 90 | | 75 | | 60 | | 55 | | 50 | | ns |
| tDM | Data Out to Memory Status Delay | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tP | Internal Preset Interval (Note 14) | | tEL | | tEL | | tEL | | tEL | | tEL | ns |

## SWITCHING WAVEFORMS

### READ CYCLE




MPR-392

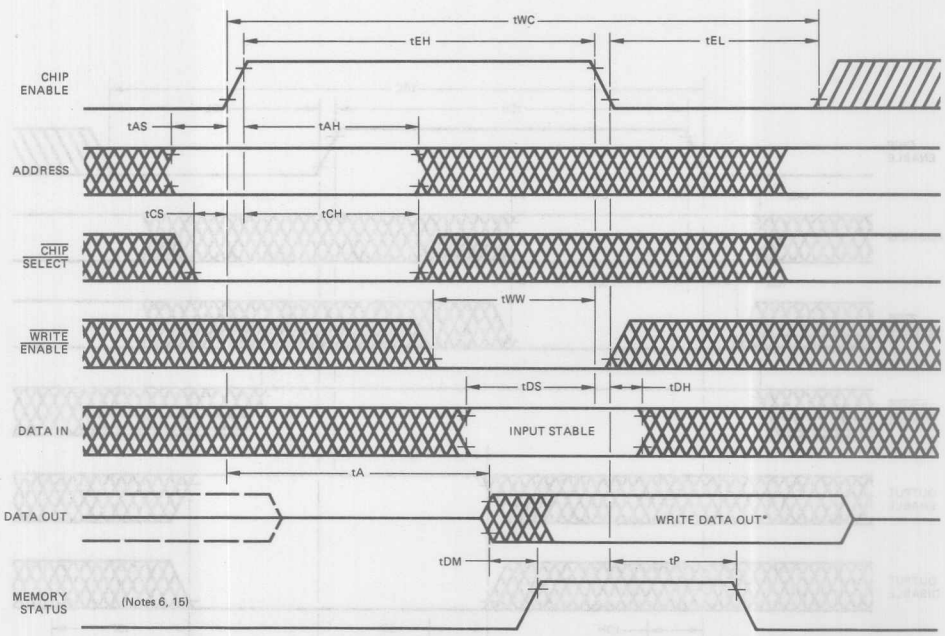
## SWITCHING CHARACTERISTICS over operating range

### WRITE CYCLE (Notes 7, 8, 9)

| Parameter | Description | Am9140A Am91L40A Min. | Am9140A Am91L40A Max. | Am9140B Am91L40B Min. | Am9140B Am91L40B Max. | Am9140C Am91L40C Min. | Am9140C Am91L40C Max. | Am9140D Am91L40D Min. | Am9140D Am91L40D Max. | Am9140E Min. | Am9140E Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| tWC | Write Cycle Time (Note 5) | 770 | | 620 | | 470 | | 395 | | 320 | | ns |
| tA | Access Time (CE to Output ON Delay) | | 500 | | 400 | | 300 | | 250 | | 200 | ns |
| tEH | Chip Enable HIGH Time (Notes 14, 15) | 500 | | 400 | | 300 | | 250 | | 200 | | ns |
| tEL | Chip Enable LOW Time (Notes 14, 15) | 250 | | 200 | | 150 | | 125 | | 100 | | ns |
| tAS | Address to Chip Enable Set-Up Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tAH | Chip Enable to Address Hold Time | 200 | | 170 | | 150 | | 130 | | 120 | | ns |
| tCS | Chip Select to CE Set-Up Time (Note 4) | –5 | | –5 | | –5 | | –5 | | – 5 | | ns |
| tCH | Chip Enable to Chip Select Hold Time | 200 | | 170 | | 150 | | 130 | | 120 | | ns |
| tWW | Write Pulse Width (Note 10) | 200 | | 165 | | 135 | | 115 | | 100 | | ns |
| tDS | Data Input Set-Up Time (Note 10) | 200 | | 165 | | 135 | | 115 | | 100 | | ns |
| tDH | Data Input Hold Time (Note 10) | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tDM | Data Out to Memory Status Delay | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tP | Internal Preset Interval | | tEL | | tEL | | tEL | | tEL | | tEL | ns |

## SWITCHING WAVEFORMS

### WRITE CYCLE




*Assumes output is enabled.

MPR-393

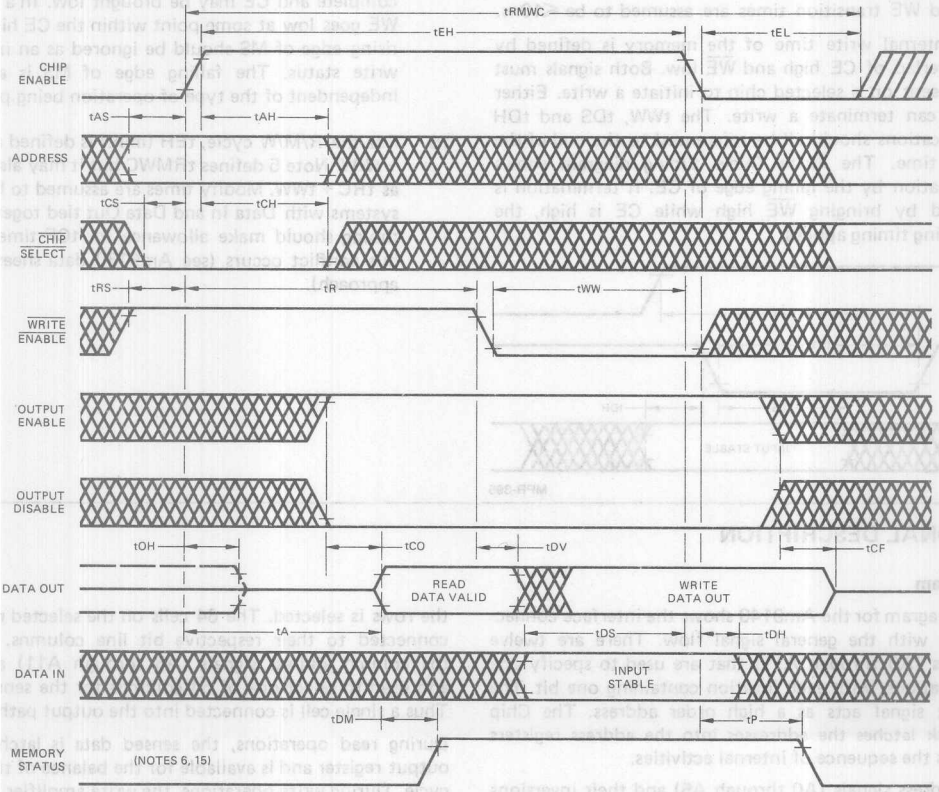
## SWITCHING CHARACTERISTICS over operating range

### READ/MODIFY/WRITE CYCLE (Notes 7, 8, 9)

| Parameter | Description | Am9140A Am91L40A Min. | Am9140A Am91L40A Max. | Am9140B Am91L40B Min. | Am9140B Am91L40B Max. | Am9140C Am91L40C Min. | Am9140C Am91L40C Max. | Am9140D Am91L40D Min. | Am9140D Am91L40D Max. | Am9140E Min. | Am9140E Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| tRMWC | R/M/W Cycle Time (Notes 5, 16) | 970 | | 785 | | 605 | | 510 | | 420 | | ns |
| tA | Access Time (CE to Output Valid Delay) | | 500 | | 400 | | 300 | | 250 | | 200 | ns |
| tEH | Chip Enable HIGH Time (Notes 14, 15) | 700 | | 565 | | 435 | | 365 | | 300 | | ns |
| tEL | Chip Enable LOW Time (Notes 14, 15) | 250 | | 200 | | 150 | | 125 | | 100 | | ns |
| tCH | Chip Enable to Chip Select Hold Time | 200 | | 170 | | 150 | | 130 | | 120 | | ns |
| tAH | Chip Enable to Address Hold Time | 200 | | 170 | | 150 | | 130 | | 120 | | ns |
| tCS | Chip Select to CE Set-Up Time (Note 4) | −5 | | −5 | | −5 | | −5 | | −5 | | ns |
| tAS | Address to Chip Enable Set-Up Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tRS | Read to Chip Enable Set-Up Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tOH | Chip Enable to Output OFF Delay | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tDH | Data Input Hold Time (Note 10) | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tDS | Data Input Set-Up Time (Note 10) | 200 | | 165 | | 135 | | 115 | | 100 | | ns |
| tWW | Write Pulse Width (Note 10) | 200 | | 165 | | 135 | | 115 | | 100 | | ns |
| tCF | OE or OD to Output OFF Delay (Note 11) | | 200 | | 165 | | 135 | | 115 | | 100 | ns |
| tCO | OE or OD to Output ON Delay (Note 11) | | 220 | | 185 | | 150 | | 125 | | 110 | ns |
| tDV | Data Valid after Write Delay | 10 | | 10 | | 10 | | 10 | | 10 | | ns |
| tR | Read Mode Hold Time | tA | | tA | | tA | | tA | | tA | | ns |
| tDM | Data Out to Memory Status Delay | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| tP | Internal Preset Interval | | tEL | | tEL | | tEL | | tEL | | tEL | ns |

## SWITCHING WAVEFORMS

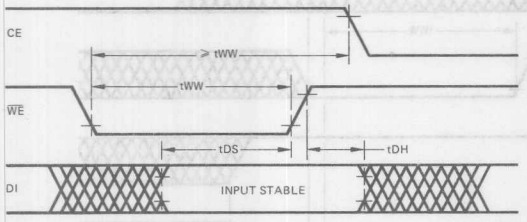
### READ/MODIFY/WRITE CYCLE




MPR-394

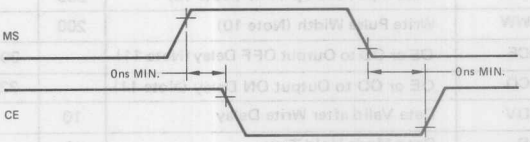
## NOTES:

1. Typical operating supply current values are specified for nominal processing parameters, nominal supply voltage and the specific ambient temperature shown.
2. Typical power-down supply current values are specified for nominal processing parameters, the specific supply voltage shown and the specific ambient temperature shown.
3. At any operating temperature the minimum access time, tA(min.), will be greater than the maximum CE to output OFF delay, tOH(max.).
4. The negative value shown indicates that the Chip Select input may become valid as late as 5.0ns following the start of the Chip Enable rising edge.
5. The worst-case cycle times are the sum of CE rise time, tEH, CE fall time and tEL. The cycle time values shown include the worst-case tEH and tEL requirements and assume CE transition times of 10ns.
6. The Memory Status signal is a two-state output and is not affected by the Output Disable or Output Enable signals. If the output data buffers are turned off, Memory Status will continue to reflect the internal status of the memory.
7. Output loading is assumed to be one standard TTL gate plus 50pF of capacitance.
8. Timing reference levels for both input and output signals are 0.8V and 2.0V.
9. CE and $\overline{WE}$ transition times are assumed to be ≤10ns.
10. The internal write time of the memory is defined by the overlap of CE high and $\overline{WE}$ low. Both signals must be present on a selected chip to initiate a write. Either signal can terminate a write. The tWW, tDS and tDH specifications should all be referenced to the end of the write time. The Write Cycle timing diagram shows termination by the falling edge of CE. If termination is defined by bringing $\overline{WE}$ high while CE is high, the following timing applies:




MPR-395

11. The output data buffer can be ON and output data valid only when Output Enable is high and Output Disable is low. OE and OD perform the same function with opposite control polarity.
12. The output data buffer should be enabled before the falling edge of CE in order to read output information. When the output is disabled and CE is low, the output data register is cleared.
13. Input and output data are the same polarity.
14. The Chip Enable waveform requirements may be defined by the Memory Status output waveform. For a read cycle, the basic CE requirement is that tEH ≥ tA and tEL ≥ tP:




MPR-396

15. The Memory Status output functions as if all operations are read cycles. If a write cycle begins with $\overline{WE}$ low and Data In stable at the time CE goes high, the rising edge of MS may be used as an indication that the write is complete and CE may be brought low. In a cycle where $\overline{WE}$ goes low at some point within the CE high time, the rising edge of MS should be ignored as an indication of write status. The falling edge of MS is always valid independent of the type of operation being performed.
16. For the R/M/W cycle, tEH (min.) is defined as tR (min.) + tWW. Note 5 defines tRMWC but it may also be viewed as tRC + tWW. Modify times are assumed to be zero. For systems with Data In and Data Out tied together R/M/W timing should make allowance for tCF time so that no bus conflict occurs (see Am9130 data sheet for timing approach).

## FUNCTIONAL DESCRIPTION

### Block Diagram

The block diagram for the Am9140 shows the interface connections along with the general signal flow. There are twelve address lines (A0 through A11) that are used to specify one of 4096 locations, with each location containing one bit. The Chip Select signal acts as a high order address. The Chip Enable clock latches the addresses into the address registers and controls the sequence of internal activities.

The row address signals (A0 through A5) and their inversions are distributed to the 64 row address decoders where one of the rows is selected. The 64 cells on the selected row are then connected to their respective bit line columns. Meanwhile, the column address signals (A6 through A11) are decoded and used to select one of 64 columns for the sense amplifier. Thus a single cell is connected into the output path.

During read operations, the sensed data is latched into the output register and is available for the balance of the operating cycle. During write operations, the write amplifier is turned on and drives the input data onto the sense lines, up the column

bit lines and into the selected cell. Read and write data are the same polarity.

The data buffer is three-state and unselected chips have their outputs turned off so that several may be wire-ored together. The Output Enable and Output Disable signals provide asynchronous controls for turning off the output buffers.

Within the storage matrix there is an extra row of simulated cells. This reference row is selected on every operating cycle in addition to the addressed row and provides internal timing signals that control the data flow through the memory. The Memory Status output signal is derived from the reference row and uses the same designs for its sense and buffer circuits as used by the data bits.

### Chip Enable

The Chip Enable input is a control clock that coordinates all internal activities. The rising edge of CE begins each cycle and strobes the Address and Chip Select signals into the on-chip register. Internal timing signals are derived from CE and from transitions of the address latches and the reference cells.

When the actual access time of the part has been reached (or a write operation is complete), CE may be switched low if desired. The worst-case time as specified in the data sheet may be used to determine the access. Alternatively, the access or write-complete time indicated by the rising edge of the Memory Status output signal may be used.

When CE goes low, the internal preset operation begins. The memory is ready for a new cycle only after the preset is complete. The worst-case CE low time specified in the data sheet may be used to determine the preset interval. Alternatively, the actual preset time is indicated as complete when Memory Status goes low.

There are no restrictions on the maximum times that CE may remain in either state so the clock may be extended or stopped whenever convenient. After power-on and before beginning a valid operation, the clock should be brought low to initially preset the memory.

### Address and Chip Select

The Address inputs are latched into the on-chip address register by the rising edge of CE. Addresses must be held stable for the specified minimum time following the rising edge of CE in order to be properly loaded into the register. Following the address hold time, the address inputs are ignored by the memory until the next cycle is initiated.

The Chip Select input acts as a high order address for use when the system word capacity is larger than that of an individual chip. It allows the Address lines to be wired in parallel to all chips with the CS lines then used to select one active row of chips at a time. Unselected chips have their output buffers off so that selected chips wired to the same data lines can dominate the output bus. Only selected chips can perform write operations.

CS is latched in the same way that Addresses are. Once a memory is selected or deselected, it will remain that way until a new cycle with new select information begins.

### Write Enable

The Write Enable line controls the read or write condition of the devices. When the CE clock is low, the WE signal may be in any state without affecting the memory. WE does not affect the status of the output buffer.

To execute a read cycle, WE is held high while CE is high. To perform a write operation, the WE line is switched low while CE is high. Only a narrow write pulse width is required to successfully write into a cell. In many cases, however, it will be convenient to leave the WE line low during the whole cycle.

A write cycle can take place only when three conditions are met: The chip is selected, CE is high, and WE is low. This means that if either CE goes low or WE goes high, the writing is terminated.

### Data In and Data Out

The requirements for incoming data during a write operation show a minimum set-up time with respect to the termination of the write. Termination occurs when either WE goes high or CE goes low. If incoming data changes during a write operation, the information finally written in the cell will be that stable data preceeding the termination by the set-up time. Since the data being written during a write cycle is impressed on the sense amplifier inputs, the output data will be the same as the input once the write is established.

During a read cycle, once all of the addressing is complete and the cell information has propagated through the sense amplifier, it enters the output data register. The read information can also flow through to the output if the buffer is enabled. As long as CE is high, the addressing remains valid and the output data will be stable. When CE goes low to begin the internal preset operation, the output information is latched into the data register. It will remain latched and stable as long as CE is low. If the output is disabled when CE is low, the output data register is cleared. At the start of every cycle when CE goes high, the output data latch is cleared in preparation for new information to come from the sense amplifier, and the output buffer is turned off.

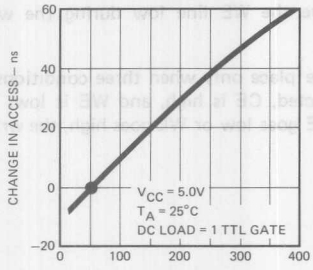
OE and OD are designed to provide asynchronous control of the output buffer independent of the synchronous Chip Select control. The OE and OD control lines perform the same internal function except that one is inverted from the other. If either OE is low or OD is high, the output buffer will turn off. If the CS input is latched low and OE is high and OD is low, then the output buffer can turn on when data is available.

### Memory Status

The Memory Status output is derived from the actual performance of the reference row of cells. Since the reference row is always doing a read operation, the MS output will appear in every operating cycle, whether a read or write is being performed. MS uses the same output circuitry as used in the data path. The result is that Memory Status tracks very closely the true operating performance of the memory.

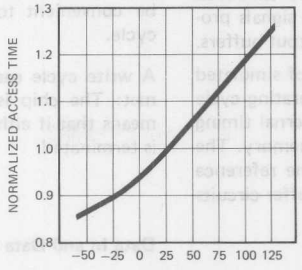
The rising edge of MS indicates when output data is valid and tracks changes in access time with changing operating conditions. The rising edge also specifies the end of the time that CE must be held high for a read. CE may be high as long as desired, but may safely go low any time after MS goes high. The falling edge of MS occurs after CE goes low and the internal preset period is complete. It indicates that CE may go high to begin a new cycle. See the Am9130/40 Application Note for details.

### Versus Capacitive Load



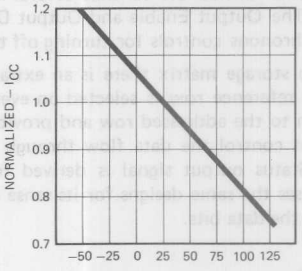

CAPACITIVE LOAD – pF MPR-397

### Versus Ambient Temperature



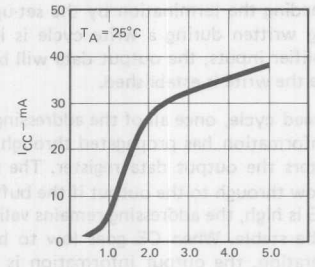

AMBIENT TEMPERATURE – °C MPR-398

### Versus Ambient Temperature



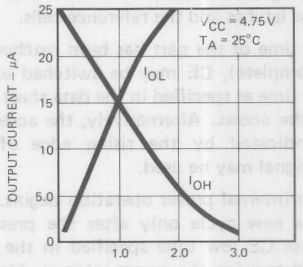

AMBIENT TEMPERATURE – °C MPR-399

### Typical $I_{CC}$ Versus $V_{CC}$



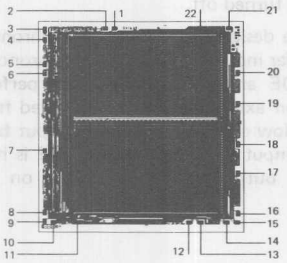

MPR-400

### Typical Output Currents Versus Output Voltage



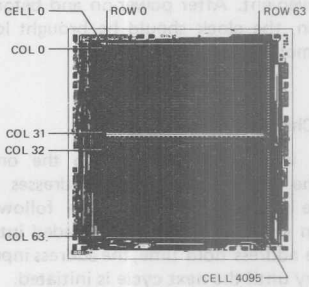

MPR-401

### Metallization and Pad Layout




DIE SIZE 0.192" X 0.197"

### Bit Map




For bit mapping purposes:
Row address LSB = A5, MSB = A0
Column address LSB = A6, MSB = A11

# Am9141 • Am91L41

## 4096 x 1 Static R/W Random Access Memories

2

### DISTINCTIVE CHARACTERISTICS

- 4k X 1 organization
- Fully static data storage — no refreshing
- Single +5V power supply
- High-speed — access times down to 200ns max.
- Low operating power
  - 578mW max., 9141
  - 368mW max., 91L41
- Interface logic levels identical to TTL
- High noise immunity — 400mV worst-case
- High output drive — two standard TTL loads
- DC power-down mode — reduces power by >80%
- Single phase, low voltage, low capacitance clock
- Static clock may be stopped in either state
- Data register on-chip
- Address register on-chip
- Steady power drain — no large surges
- Full MIL temperature range available
- 100% reliability assurance testing in compliance with MIL-STD-883

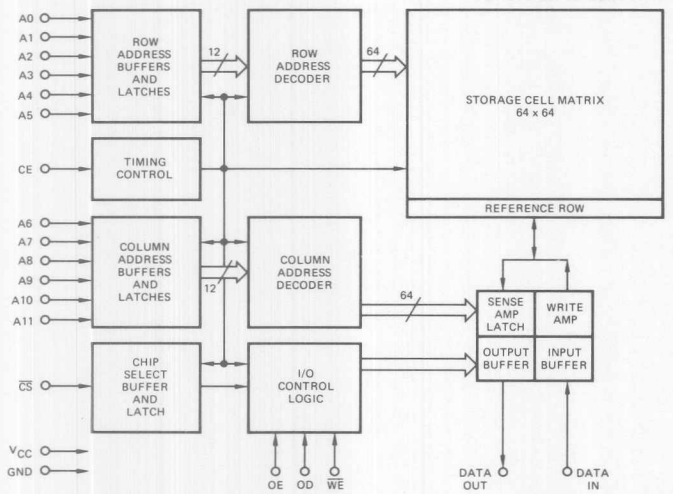
### GENERAL DESCRIPTION

The Am9141 and Am91L41 products are high performance, low-power, 4k-bit, static, read/write random access memories. They are implemented as 4096 words by 1 bit per word. Only a single +5V power supply is required for normal operation. A DC power-down mode reduces power while retaining data with a supply voltage as low as 1.5V.

All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive two full TTL loads or more than eight low-power Schottky loads.

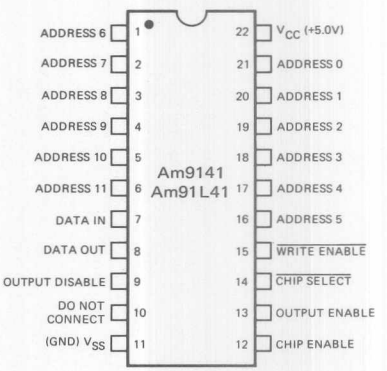
Operational cycles are initiated when the Chip Enable clock goes HIGH. When the read or write is complete, Chip Enable goes LOW to preset the memory for the next cycle. Address and Chip Select signals are latched on-chip to simplify system timing. Output data is also latched and is available until the next operating cycle. The $\overline{WE}$ signal is HIGH for all read operations and is LOW during the Chip Enable time to perform a write.

### BLOCK DIAGRAM




MOS-364

### CONNECTION DIAGRAM




**Top View**

Pin 1 is marked for orientation.

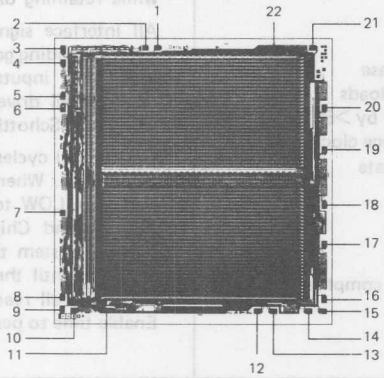
MOS-365

### ORDERING INFORMATION

| Package Type | Ambient Temperature | Power Type | Access Time | | | | |
|---|---|---|---|---|---|---|---|
| | | | 500ns | 400ns | 300ns | 250ns | 200ns |
| Hermetic DIP | $0°C \leq T_A \leq +70°C$ | STD | Am9141ADC | Am9141BDC | Am9141CDC | Am9141DDC | Am9141EDC |
| | | LOW | Am91L41ADC | Am91L41BDC | Am91L41CDC | Am91L41DDC | |
| | $-55°C \leq T_A \leq +125°C$ | STD | Am9141ADM | Am9141BDM | Am9141CDM | | |
| | | LOW | Am91L41ADM | Am91L41BDM | Am91L41CDM | | |

The Am9141 and Am91L41 memories are identical in every respect to their counterparts in the Am9140 and Am91L40 family, with the single exception that the Memory Status output is not functional. Pin 10 on the Am9141/L41 products should not be used and should not be connected to any external circuit. Please refer to the Am9140/L40 data sheet for the electrical and switching characteristics of the Am9141/L41.

**Metallization and Pad Layout**




DIE SIZE 0.192 x 0.197"

# Am9147

## 4096 x 1 Static R/W Random Access Memory

**PRELIMINARY**

2

### DISTINCTIVE CHARACTERISTICS

- High speed – access times down to 55ns maximum
- 4K x 1 organization
- Single +5 volt power supply
- Fully static storage and interface circuitry
- No clocks or timing signals required
- Equal access and cycle times
- Automatic power-down when deselected
- Low power dissipation
  - Am9147: 880mW active, 110mW power down
- Standard 18-pin, .300 inch dual in-line package
- High output drive
  - Up to seven standard TTL loads or six Schottky TTL loads
- TTL compatible interface levels
- 100% MIL-STD-883 reliability assurance testing
- No power-on current surge
- Polyplanar™ technology

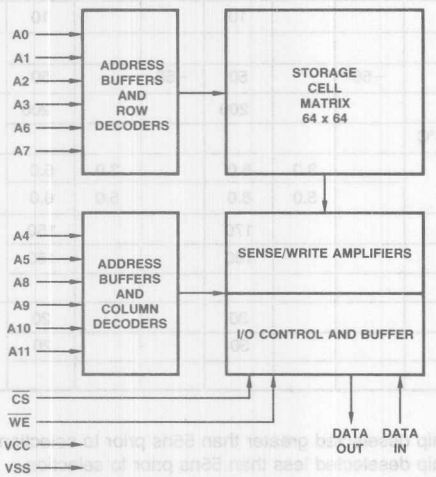
### GENERAL DESCRIPTION

The Am9147 is a high performance, 4096-bit, static, read/write, random access memory. It is organized as 4096 words by one bit per word. All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive up to seven standard Schottky TTL loads or up to six standard TTL loads.

Only a single +5 volt power supply is required. When deselected (CS ≥ VIH), the Am9147 automatically enters a power-down mode which reduces power dissipation by more than 85%. When selected, the chip powers up again with no access time penalty.

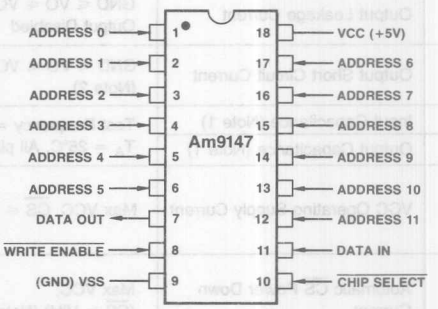
Data In and Data Out use separate pins on the standard 18-pin package. Data Out is the Same polarity as Data In. Data Out is a 3-state signal allowing wired-or operation of several chips. Data In and Data Out may be connected together for operation in a common data bus environment.

### BLOCK DIAGRAM




MOS-267

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

MOS-268

### ORDERING INFORMATION

| | Am9147-55 | Am9147-70 |
|---|---|---|
| Maximum Access Time (ns) | 55 | 70 |
| Maximum Active Current (mA) | 180 | 160 |
| Maximum Standby Current (mA) | 30 | 20 |

## MAXIMUM RATINGS beyond which useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65 to +150°C |
| Ambient Temperature Under Bias | −55 to +125°C |
| VCC with Respect to VSS | −0.5 to +7.0V |
| All Signal Voltages with Respect to VSS | −1.5 to +7.0V |
| Power Dissipation (Package Limitation) | 1.2W |
| DC Output Current | 20mA |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGE

| Part Number | Ambient Temperature | VSS | VCC | Part Number | Ambient Temperature | VSS | VCC |
|---|---|---|---|---|---|---|---|
| Am9147-55 PC/DC<br>Am9147-70 PC/DC | 0°C ≤ $T_A$ ≤ +70°C | 0V | +5.0V ± 10% | Am9147DM | −55°C ≤ $T_A$ ≤ +125°C | 0V | +5.0V ± 10% |

## ELECTRICAL CHARACTERISTICS over operating range (Note 6)

| Parameter | Description | Test Conditions | | Am9147-55 Min | Am9147-55 Typ (Note 1) | Am9147-55 Max | Am9147-70 Min | Am9147-70 Typ (Note 1) | Am9147-70 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| IOH | Output High Current | VOH = 2.4V | VCC = 4.5V | −4 | | | −4 | | | mA |
| IOL | Output Low Current | VOL = 0.4V | $T_A$ = 70°C | 12 | | | 12 | | | mA |
| | | | $T_A$ = 125°C | | | | | | | |
| VIH | Input High Voltage | | | 2.0 | | 6.0 | 2.0 | | 6.0 | Volts |
| VIL | Input Low Voltage | | | −1.0 | | 0.8 | −1.0 | | 0.8 | Volts |
| IIX | Input Load Current | VSS ≤ VI ≤ VCC | | | | 10 | | | 10 | μA |
| IOZ | Output Leakage Current | GND ≤ VO ≤ VCC<br>Output Disabled | $T_A$ = 125°C | | | | | | | μA |
| | | | $T_A$ = 70°C | −50 | | 50 | −50 | | 50 | |
| IOS | Output Short Circuit Current | GND ≤ VO ≤ VCC<br>(Note 2) | 0 to + 70°C | | | 200 | | | 200 | mA |
| | | | −55 to +125°C | | | | | | | |
| CI | Input Capacitance (Note 1) | Test Frequency = 1.0MHz<br>$T_A$ = 25°C, All pins at 0V | | | 3.0 | 5.0 | | 3.0 | 5.0 | pF |
| CO | Output Capacitance (Note 1) | | | | 5.0 | 6.0 | | 5.0 | 6.0 | |
| ICC | VCC Operating Supply Current | Max VCC, $\overline{CS}$ ≤ VIL | $T_A$ = 25°C | | | 170 | | | 150 | mA |
| | | | $T_A$ = 0°C | | | 180 | | | 160 | |
| | | | $T_A$ = −55°C | | | | | | | |
| ISB | Automatic $\overline{CS}$ Power Down Current | Max VCC,<br>($\overline{CS}$ ≥ VIH) (Note 5) | $T_A$ = 0°C | | | 30 | | | 20 | mA |
| | | | $T_A$ = 70°C | | | 30 | | | 20 | |
| | | | $T_A$ = 125°C | | | | | | | |

Notes:

1. Typical values are for $T_A$ = 25°C, nominal supply voltage and nominal processing parameters.
2. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
3. Test conditions assume signal transition times of 10ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.5V and output loading of the specified IOL/IOH and 30pF load capacitance.
4. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
5. A pull up resistor to VCC on the $\overline{CS}$ input is required to keep the device deselected, otherwise ISB will exceed values given.
6. The operating ambient temperature range is guaranteed with transverse air flow of 400 linear feet per minute.
7. Chip deselected greater than 55ns prior to selection.
8. Chip deselected less than 55ns prior to selection.
9. At any given temperature and voltage condition, tHZ is less than tLZ for all devices.
10. $\overline{WE}$ is high for read cycle.
11. Device is continuously selected, $\overline{CS}$ = VIL.
12. Address valid prior to or coincident with $\overline{CS}$ transition low.

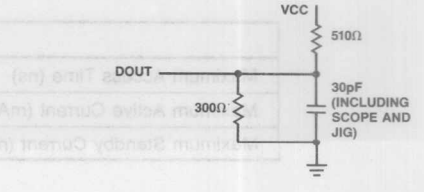


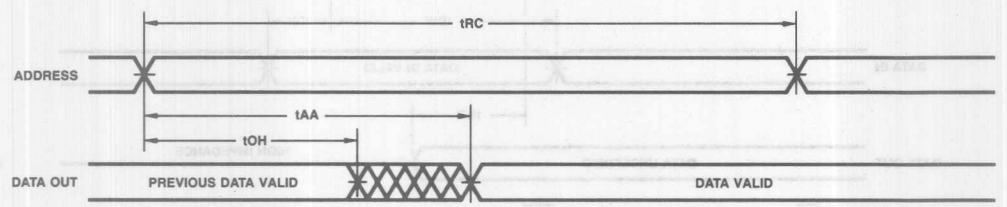

**Figure 1. Output Load.**

## SWITCHING CHARACTERISTICS over operating range (Note 3)

| Parameter | Description | | Am9147-55 Min | Am9147-55 Max | Am9147-70 Min | Am9147-70 Max | Units |
|---|---|---|---|---|---|---|---|
| **Read Cycle** | | | | | | | |
| tRC | Address Valid to Address Do Not Care Time (Read Cycle Time) | | 55 | | 70 | | ns |
| tAA | Address Valid to Data Out Valid Delay (Address Access Time) | | | 55 | | 70 | ns |
| tACS1 | Chip Select Low to Data Out Valid (Note 5) | Note 7 | | 55 | | 70 | ns |
| tACS2 | | Note 8 | | 65 | | 80 | |
| tLZ | Chip Select Low to Data Out On | Note 9 | 10 | | 10 | | ns |
| tHZ | Chip Select High to Data Out Off | Note 9 | 0 | 40 | 0 | 40 | ns |
| tOH | Address Unknown to Data Out Unknown Time | | 5 | | 5 | | ns |
| **Write Cycle** | | | | | | | |
| tWC | Address Valid to Address Do Not Care Time (Write Cycle Time) | | 55 | | 70 | | ns |
| tWP | Write Enable Low to Write Enable High Time (Note 4) | | 35 | | 40 | | ns |
| tWR | Write Enable High to Address Do Not Care Time | | 10 | | 15 | | ns |
| tWZ | Write Enable Low to Data Out Off Delay | | 0 | 30 | 0 | 35 | ns |
| tDW | Data In Valid to Write Enable High Time | | 25 | | 30 | | ns |
| tDH | Write Enable Low to Data In Do Not Care Time | | 10 | | 10 | | ns |
| tAS | Address Valid to Write Enable Low Time | | 0 | | 0 | | ns |
| tPD | Chip Select High to Power Low Delay | | | 30 | | 30 | ns |
| tPU | Chip Select Low to Power High Delay | | 0 | | 0 | | ns |
| tCW | Chip Select Low to Write Enable High Time (Note 4) | | 45 | | 55 | | ns |
| tOW | Write Enable High to Output Turn On | | 0 | | 0 | | ns |
| tAW | Address Valid to End of Write | | 45 | | 55 | | ns |

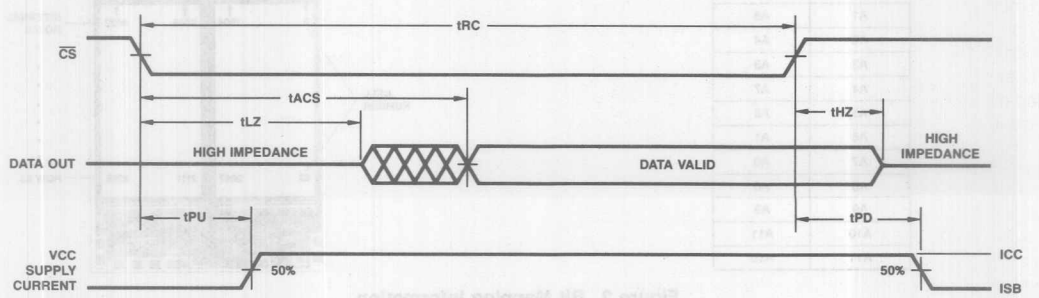
## SWITCHING WAVEFORMS

### READ CYCLE NO. 1 (Notes 10, 11)




MOS-328

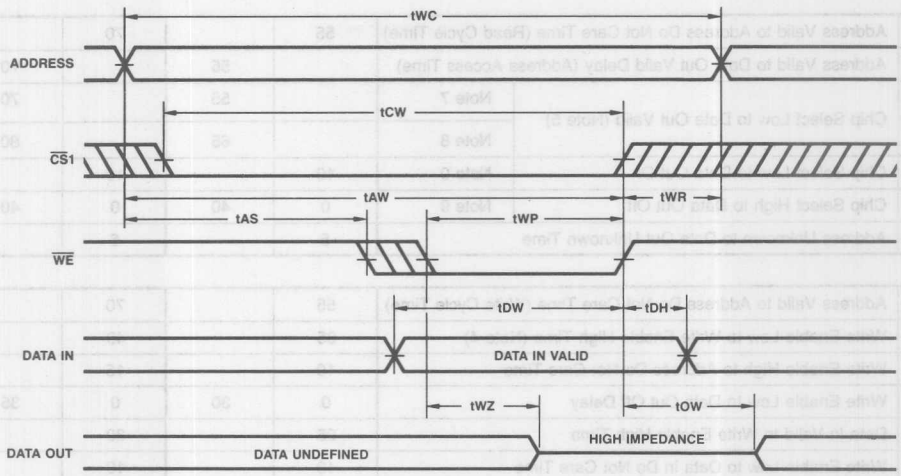
### READ CYCLE NO. 2 (Notes 10, 12)



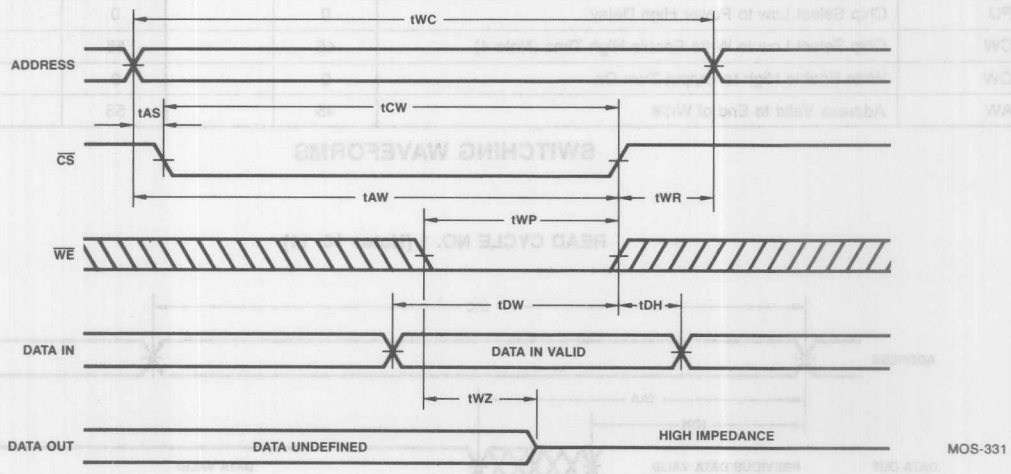

MOS-329

## SWITCHING WAVEFORMS (Cont.)

### WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)




### WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)




Note: If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

### BIT MAP

| Address Designators | |
|---|---|
| External | Internal |
| A0 | A2 |
| A1 | A5 |
| A2 | A4 |
| A3 | A3 |
| A4 | A7 |
| A5 | A8 |
| A6 | A1 |
| A7 | A0 |
| A8 | A6 |
| A9 | A9 |
| A10 | A11 |
| A11 | A10 |

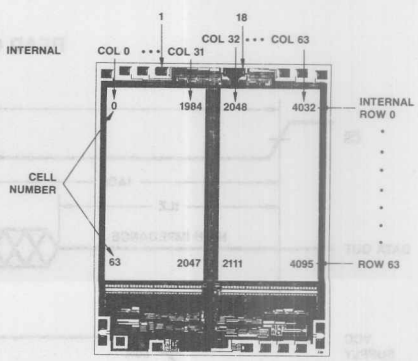
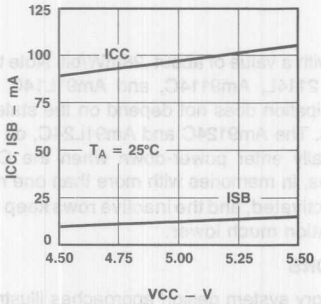


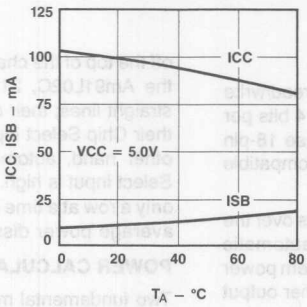

**Figure 2. Bit Mapping Information.**

## TYPICAL DC AND AC CHARACTERISTICS

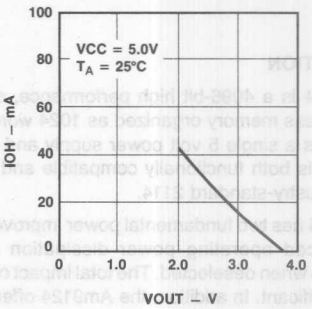
**Supply Current Versus Supply Voltage**



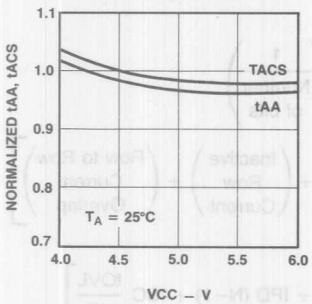

**Supply Current Versus Ambient Temperature**



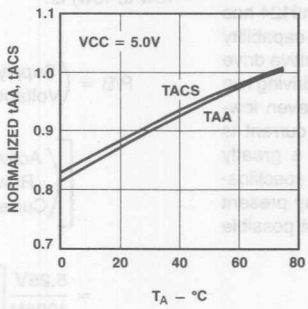

**Output Source Current Versus Output Voltage**



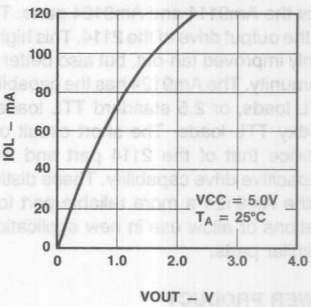

**Normalized Access Time Versus Supply Voltage**



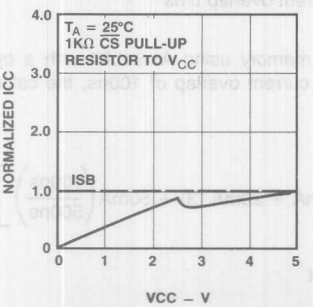

**Normalized Access Time Versus Ambient Temperature**



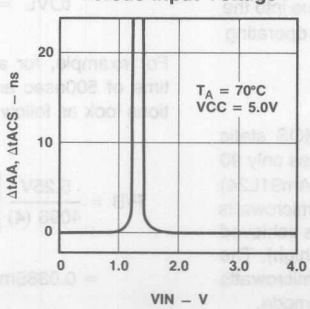

**Output Sink Current Versus Output Voltage**



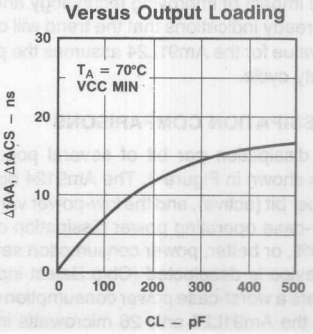

**Typical Power-On Current Versus Power Supply**




**Access Time Change Versus Input Voltage**




**Access Time Change Versus Output Loading**




Note: 1. The supply current shown in Graphs 1 and 2 are for the 9147-70. The supply current curves for the 9147-55 can be calculated by scaling proportionately.

MOS-332

# IMPROVED PERFORMANCE WITH THE Am9124

By Alex Shevekov, Paul Liu and Joe Kroeger

## INTRODUCTION

The Am9124 is a 4096-bit high performance, static read/write random access memory organized as 1024 words by 4 bits per word. It uses a single 5 volt power supply and a dense 18-pin package. It is both functionally compatible and pin compatible with the industry-standard 2114.

The Am9124 has two fundamental power improvements over the 2114: reduced operating power dissipation and automatic power-down when deselected. The total impact on system power is quite significant. In addition, the Am9124 offers higher output fan-out capability.

## IMPROVED D.C. PARAMETERS

Figure 1 compares the D.C. parameters of the 2114, Am9114, Am9124 and their low-power equivalents. The Am9114 is similar to the Am9124, except that it does not feature power-down on deselection. In addition to supply current, significant differences in IOL (output low current) and IOS (output short-circuit current) are shown for the Am9114 and Am9124 parts. The Am9124 has nearly twice the output drive of the 2114. This high drive capability allows not only improved fan-out, but also better capacitive drive and noise immunity. The Am9124 has the capability of driving two Schottky TTL loads, or 2.5 standard TTL loads or eleven low-power Schottky TTL loads. The short circuit output current is more than twice that of the 2114 part and reflects a greatly improved capacitive drive capability. These distinctive specifications make the Am9124 a more reliable part for many present 2114 applications or allow use in new applications not possible with other similar parts.

## SPEED/POWER PRODUCT

Figure 2 demonstrates the speed-power product per bit achieved by AMD for several static random access memories. The speed-power product is a figure of merit obtained by multiplying the fastest worst-case access time for a particular RAM family by the worst-case power consumption and dividing the product by the bit capacity of the chip. The trend is clear from the graph and shows the dramatic impact of improving technology and circuit design. There are already indications that the trend will continue into the future. The value for the Am91L24 assumes the part is operating at a 25% duty cycle.

## POWER DISSIPATION COMPARISONS

The power dissipation per bit of several popular MOS static memories is shown in Figure 3. The Am9124 dissipates only 90 microwatts per bit (active), and the low-power version (Am91L24) has a worst-case operating power dissipation of 64 microwatts per bit. A 50%, or better, power consumption saving is achieved when the device is deselected (Chip Select input is high). The Am9124 offers a worst-case power consumption of 39 microwatts per bit, and the Am91L24 only 26 microwatts in this mode.

Figure 4 shows the worst-case power dissipation per bit for various part types in various operating configurations. The 1k-bit Am91L02C is shown for comparison purposes. The Am9102C is off the top of the chart with a value of about .28mW/bit. Note that the Am91L02C, 2114, 2114L, Am9114C, and Am91L14C are straight lines; their dissipation does not depend on the state of their Chip Select inputs. The Am9124C and Am91L24C, on the other hand, automatically enter power-down when the Chip Select input is high.Thus, in memories with more than one row, only a row at a time is activated, and the inactive rows keep the average power dissipation much lower.

## POWER CALCULATIONS

Two fundamental memory system design approaches illustrate the advantage of the Am9124 power-down characteristic. The first approach simply statically decodes addresses to generate Chip Selects.This means that one row of the memory is always active whether or not it is being accessed, and the only change with system cycle time (rate of address generation) is the supply current overlap time when selecting a new row. The equation for this "no deselect" mode for worst-case operation (access from row to row) is:

$$P/B = \left(\begin{matrix}\text{Supply}\\ \text{Voltage}\end{matrix}\right)\left(\frac{1}{\begin{matrix}\text{Number}\\ \text{of bits}\end{matrix}}\right) \cdot \left[\left(\begin{matrix}\text{Active}\\ \text{Row}\\ \text{Current}\end{matrix}\right) + \left(\begin{matrix}\text{Inactive}\\ \text{Row}\\ \text{Current}\end{matrix}\right) + \left(\begin{matrix}\text{Row to Row}\\ \text{Current}\\ \text{Overlap}\end{matrix}\right)\right]$$

$$= \frac{5.25V}{4096N}\left[ICC + IPD\,(N-1) + ICC\,\frac{tOVL}{tC}\right]$$

where P/B = Maximum average power per bit
N = Number of 1k rows in system memory
ICC = Operating current
IPD = Power-down current
tC = Address cycle time
tOVL = Current overlap time

For example, for a 4k memory using Am91L24 with a cycle time of 500nsec and a current overlap of 100ns, the calculations look as follows:

$$P/B = \frac{5.25V}{4096\,(4)}\left[50mA + 20mA\,(3) + 50mA\left(\frac{100ns}{500ns}\right)\right]$$

$$= 0.0385mW/bit$$

Note that successive accesses within the same row will exhibit a smaller result since the overlap component disappears.

| Parameter | Temperature | 2114 | 2114L | Am9114 | Am91L14 | Am9124 | Am91L24 |
|---|---|---|---|---|---|---|---|
| ICC ($\overline{CS}$ < VIL) | 0°C | 100mA | 70mA | 70mA | 50mA | 70mA | 50mA |
| ICC ($\overline{CS}$ > VIH) | 0°C | 100mA | 70mA | 70mA | 50mA | 30mA | 20mA |
| IOL | +70°C | 2.1mA | 2.1mA | 3.2mA | 3.2mA | 4.0mA | 4.0mA |
| IOL | +125°C | – | – | 2.4mA | 2.4mA | 3.2mA | 3.2mA |
| IOH | +70°C | 1.0mA | 1.0mA | 1.0mA | 1.0mA | 1.4mA | 1.4mA |
| IOH | +125°C | – | – | 1.0mA | 1.0mA | 1.0mA | 1.0mA |
| IOS | 0°C | 40mA | 40mA | 75mA | 75mA | 95mA | 95mA |
| IOS | −55°C | – | – | 75mA | 75mA | 115mA | 115mA |

**Figure 1. DC Parameter Comparison.**

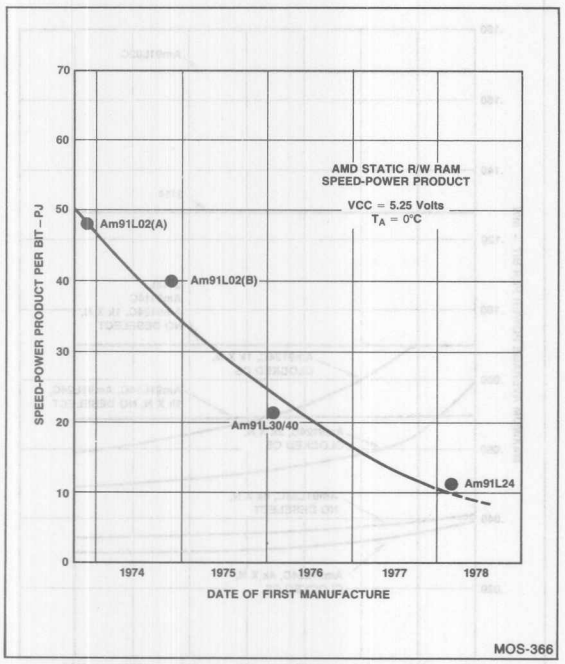



**Figure 2. Speed-Power Product.**

The second approach dynamically decodes addresses to generate Chip Select: $\overline{CS}$ is deselected (high) when no memory addressing is required. This means that the entire memory is in a power-down mode when it is not being accessed, and one row is powered-up only during active operations. This approach requires an extra timing signal to deactivate all $\overline{CS}$ signals when memory access is not under way. The power dissipation equation for this "clocked" mode is the same as in the "no deselect" mode above, except that a duty cycle factor is also included.

$$P/B = \left(\begin{matrix}\text{Supply}\\ \text{Voltage}\end{matrix}\right)\left(\frac{1}{\begin{matrix}\text{Number}\\ \text{of bits}\end{matrix}}\right)\left[\left(\begin{matrix}\text{Active}\\ \text{Row}\\ \text{Current}\end{matrix}\right)+\left(\begin{matrix}\text{Current}\\ \text{Overlap after}\\ \text{Deselect}\end{matrix}\right)+\left(\begin{matrix}\text{Deselected}\\ \text{Current for}\\ \text{Addressed Row}\end{matrix}\right)+\left(\begin{matrix}\text{Current for}\\ \text{Inactive}\\ \text{Rows}\end{matrix}\right)\right]$$

$$P/B = \frac{5.25V}{4096N}\left[\left(\frac{tCS}{tC}\,ICC\right)+\left(\frac{tOVL}{tC}\,ICC\right)+\left(\frac{tC-tCS-tOVL}{tC}\,IPD\right)+(N-1)\,IPD\right]$$

Where P/B = Maximum average power per bit
tCS = Chip select active time
tC = Address cycle time
tOVL = Current overlap time
ICC = Operating current
IPD = Power-down current
N = Number of 1k rows in system memory

For example, a 4k memory using Am91L24 with a Chip Select time of 300ns and an address cycle time of 800ns would show:

$$P/B = \frac{5.25V}{4096\,(4)}\left[\frac{300}{800}\,(50mA)+\frac{100}{800}\,(50mA)+\frac{800-300-100}{800}\,(20mA)+20mA\,(3)\right]$$

$$= 0.0304mW/bit$$

## MEMORY CAPACITY EFFECTS

The advantage of the "clocked" and the "no deselect" modes with the Am9124 series is illustrated in Figure 4 for various memory sizes using calculations based on the above equations. Figure 4 makes the conservative assumption that the supply current (ICC) rises immediately to its maximum value when $\overline{CS}$ goes low; that it does not change for 50nsec following the rising edge of $\overline{CS}$, and subsequently decreases linearly to the power-down current (IPD) over a 100nsec period.

From Figure 4, it can be observed that the Am9124 offers power advantages that increase as system size increases. The "clocked" mode reduces power consumption even further. In addition, "clocked" mode may be helpful in systems where bus contention may be a problem for any 1k x 4 part with common data I/O.

Table 1 illustrates total worst-case memory supply current requirement as a function of chip count. It is assumed that the system memory designer will take advantage of the best access times so that the width of Chip Select will equal the width of the read or write cycle. Typically, system memory configurations are

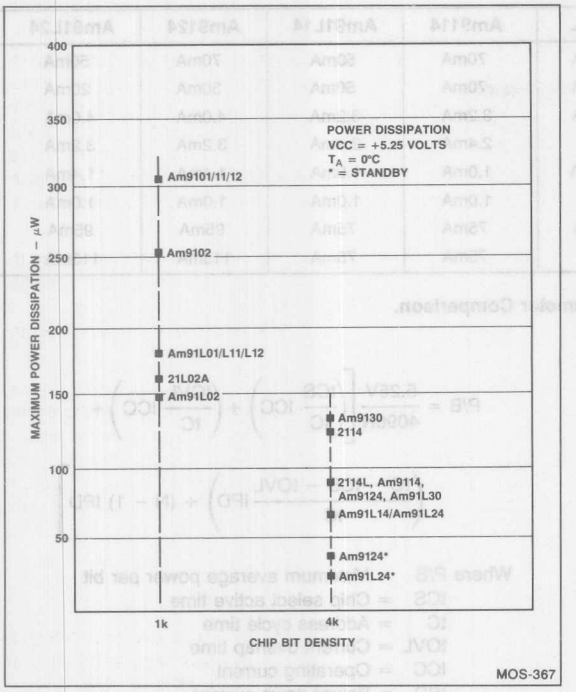



**Figure 3. Power Dissipation Improvements.**

such that one row (1k words in this case) is addressed all the time whether or not memory read/write is required; or a particular row is addressed only when an actual read/write operation will be performed. The worst-case memory operating currents for the two modes of memory operation are illustrated in the table. The "clocked" mode of operation is shown for a memory access duty cycle of 25%; otherwise the current consumption would be the same as if a row was active at all times. A close approximation of the current consumption for most such memory systems can be calculated with the following equation:

$$\Sigma ICC = K\left(\frac{M}{4} ICC\right) + (1 - K)\frac{M}{4} IPD + (N - 1)\frac{M}{4} IPD$$

Where K = duty cycle fraction
M = number of bits in a word
N = number of 1k words

Example: for an 8k x 16 memory at 25% duty cycle using Am91L24,

$$ICC = .25\ (4)\ (50) + .75\ (4)\ (20) + (8 - 1)\ (4)\ (20)$$
$$= 670mA$$

It is evident from the table that the Am9124/L24 average worst-case current improves memory system power consumption, relative to the 2114 and 2114L, by quite significant factors, with the exact difference depending on memory size and configuration.

The power-down feature advantage of the Am9124 is further demonstrated by plotting the average supply current per chip versus memory size as shown in Figure 5. The average supply current per chip converges towards the power-down value as memory size increases and the memory system power becomes less dependent on duty cycle. Even for small systems, the Am9124 offers significant power savings.

## TIMING SPECIFICATIONS

The timing patterns for the 2114, the Am9114 and the Am9124 are all the same. The timing parameter differences between the Am9124 and the 2114 involve tCO (Chip Select access time) in the read operation, tW (Write Enable pulse width) and tCW (Write Overlap). Table 2 summarizes the timing differences. In most systems, the tCO differences will not be a problem. Usually, Chip Select is decoded directly from an address. Thus, as long as tCO plus the decode time is less than the access time, the system will

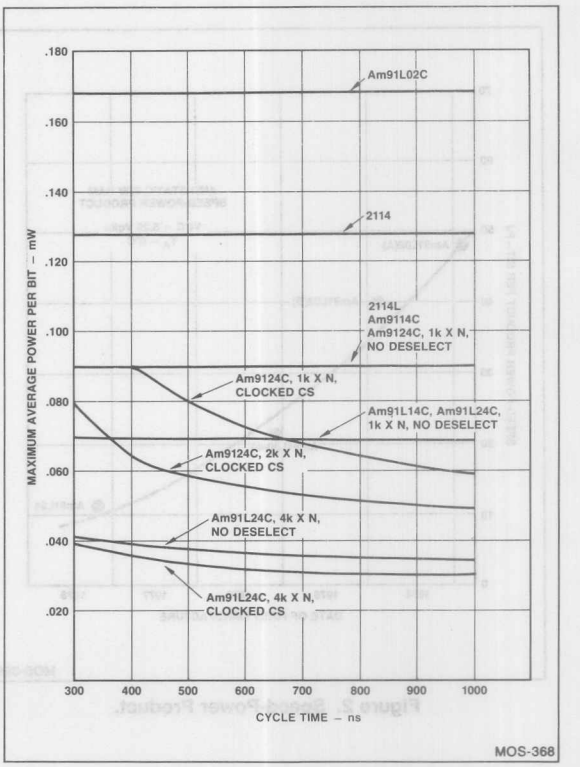



**Figure 4. Cycle Time Effects on Power.**

not know, from a timing point of view, which chip is installed. Similarly, most systems maintain very wide write pulse widths so that in the write operation, the slightly wider tW pulse widths should not be a problem.

## BUS CONTENTION

The Am9124 4k static RAMs, along with the 2114, because of their common Data I/O pins, may have problems with bus contention when used improperly. A similar situation is true for the earlier Am9112 and 2112 memories. If the chip is selected and the memory is in the Read state, then the output buffers will be driving Data Out onto the Data I/O lines. If the external system tries to drive the same lines with information there may be contention for control of the I/O bus and large surge currents can result. Even when $\overline{WE}$ is switched low, at the start of a Write cycle for example, there will be some delay before the internal buffers turn off and

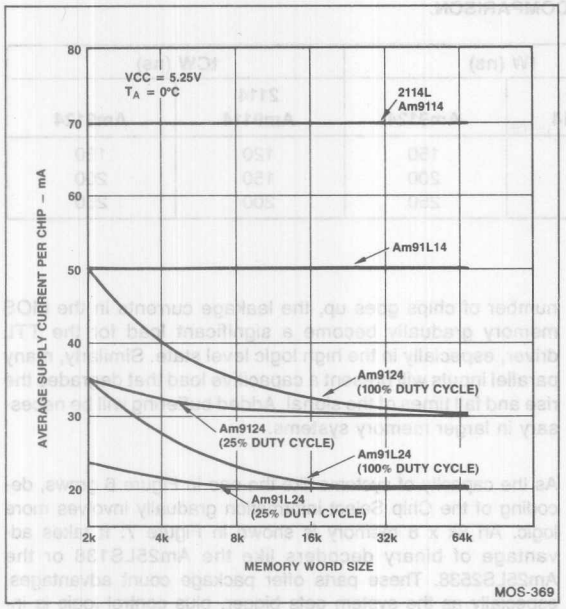



**Figure 5. Capacity Effects on Power.**

contention can therefore still be a problem. Such contention can cause several problems and should not be ignored.

The proper system design procedure is to assure that incoming Data to be written not be entered until the output buffers have been turned off. Several methods are available to accomplish this.

In many systems $\overline{CS}$ is derived directly from addresses and is low for the whole memory cycle. For writing, the designer should make sure that tW is at least tDW plus tOTW and the input data should be delayed until tOTW following the falling edge of $\overline{WE}$. With address setup and hold specifications of zero, it will often be convenient to make $\overline{WE}$ a cycle-width level (tW ≈ tWC) so that the only subcycle timing required will be the delay before the assertion of input data.

For systems where $\overline{CS}$ is high for at least tOTD preceding the falling edge of $\overline{WE}$, tW may be used at its minimum specified value. When $\overline{CS}$ is high for at least tOTD before the start of the write cycle, then no other subcycle timing is necessary; $\overline{WE}$ and Data In may occur together.

Because both $\overline{CS}$ and $\overline{WE}$ must be low to cause a Write to take place, either signal may be used to determine the effective write pulse timing. Thus $\overline{WE}$ could be a level that goes active early in the cycle while $\overline{CS}$ is inactive. $\overline{CS}$ then becomes the Write timing signal, going active sometime later after tOTW has expired. In some systems this approach will simplify the timing for driving the Data In lines.

## MEMORY SYSTEM DESIGN

Figure 6 shows a typical way to connect four Am9124 chips to make a 2k X 8 memory. The ten Address lines and the Write Enable control line are tied in parallel to all four chips.

Address 10 and its inversion are used to select one of the two rows of chips for each operating cycle. As long as A10 is low, the upper row will be active and will communicate on the data bus

**TABLE 1. MEMORY SUPPLY CURRENT REQUIREMENT.**

| | | Average Worst Case Current (mA at 0°C) | |
|---|---|---|---|
| **Memory Configuration** | **Part Number** | **One 1k row active at all times** | **One 1k row active only when accessed at 25% duty cycle** |
| 2k x 8 | 2114 | 400 | 400 |
| | 2114L | 280 | 280 |
| | Am9114 | 280 | 280 |
| | Am91L14 | 200 | 200 |
| | Am9124 | 200 | 140 |
| | Am91L24 | 140 | 95 |
| 4k X 12 | 2114 | 1200 | 1200 |
| | 2114L | 840 | 840 |
| | Am9114 | 840 | 840 |
| | Am91L14 | 600 | 600 |
| | Am9124 | 480 | 390 |
| | Am91L24 | 330 | 262.5 |
| 8k X 16 | 2114 | 3200 | 3200 |
| | 2114L | 2240 | 2240 |
| | Am9114 | 2240 | 2240 |
| | Am91L14 | 1600 | 1600 |
| | Am9124 | 1120 | 1000 |
| | Am91L24 | 760 | 670 |

TABLE 2. TIMING COMPARISON.

| Cycle Time (ns) | tCO (ns) | | tW (ns) | | tCW (ns) | |
|---|---|---|---|---|---|---|
| | 2114 Am9114 | Am9124 | 2114 Am9114 | Am9124 | 2114 Am9114 | Am9124 |
| 200 | 70 | 185 | 120 | 150 | 120 | 150 |
| 300 | 100 | 280 | 150 | 200 | 150 | 200 |
| 450 | 120 | 420 | 200 | 250 | 200 | 250 |

while the lower row is deselected and can neither read nor write. When A10 is high, the row roles are reversed.

The Data I/O lines have corresponding bits tied together in vertical columns. The control logic is arranged such that only one of the output buffers at a time will drive an I/O line, and only one chip at a time will write from an I/O line.

The type of memory illustrated is easily expanded to many different capacities. A 4k X 16, for example, could be implemented with 16 Am9124 chips (4 in each row), using the same control line configuration, plus an additional address line decoded to enable the correct row.

Driving and buffering limitations for both the inputs and outputs will be dictated by a) accumulated leakage currents and b) accumulated capacitance. On an address line, for example, many chips may be driven in parallel from a standard TTL output. As the number of chips goes up, the leakage currents in the MOS memory gradually become a significant load for the TTL driver, especially in the high logic level state. Similarly, many parallel inputs will present a capacitive load that degrades the rise and fall times of the signal. Added buffering will be necessary in larger memory systems.

As the capacity of systems like the one in Figure 6 grows, decoding of the Chip Select information gradually involves more logic. An 8k x 8 memory is shown in Figure 7. It takes advantage of binary decoders like the Am25LS138 or the Am25LS2538. These parts offer package count advantages, especially as the system gets bigger, plus control logic is included that permits deselection. A Memory Request signal is used to deselect all the memory rows when access is not required. This approach takes advantage of the automatic power-down feature of the Am9124.

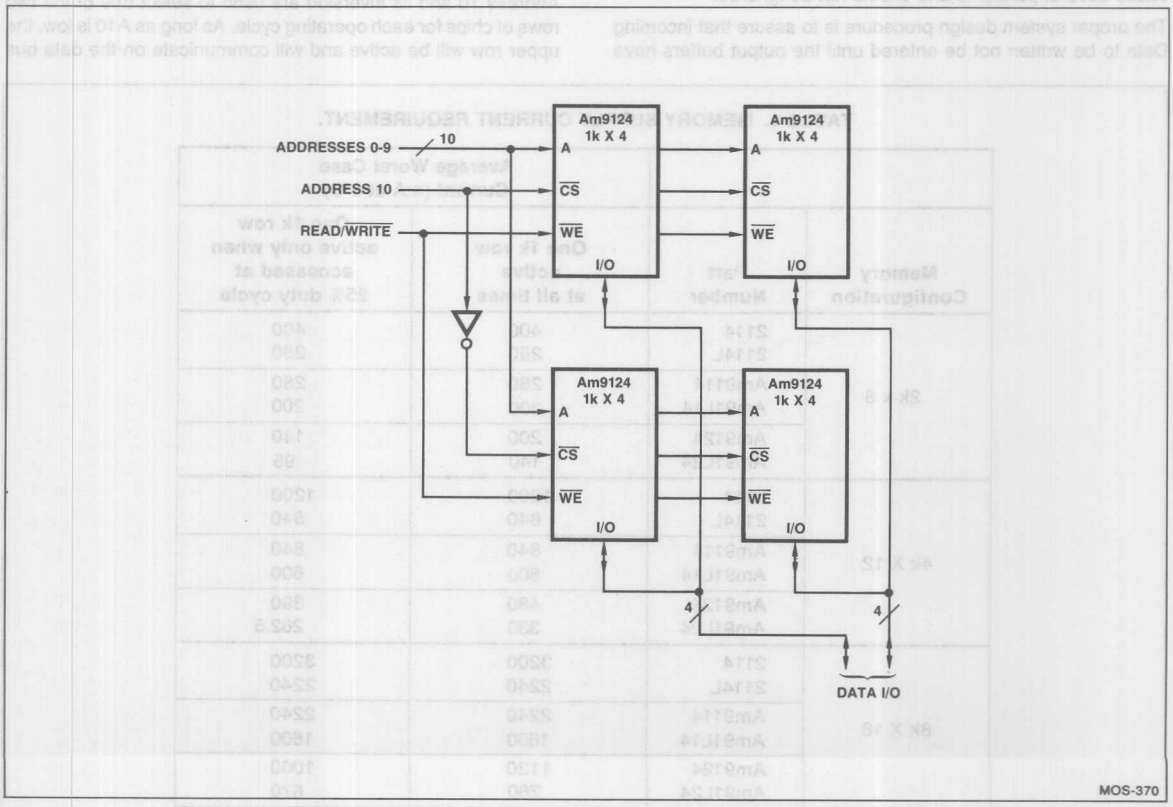



Figure 6. 2k x 8 Memory System.

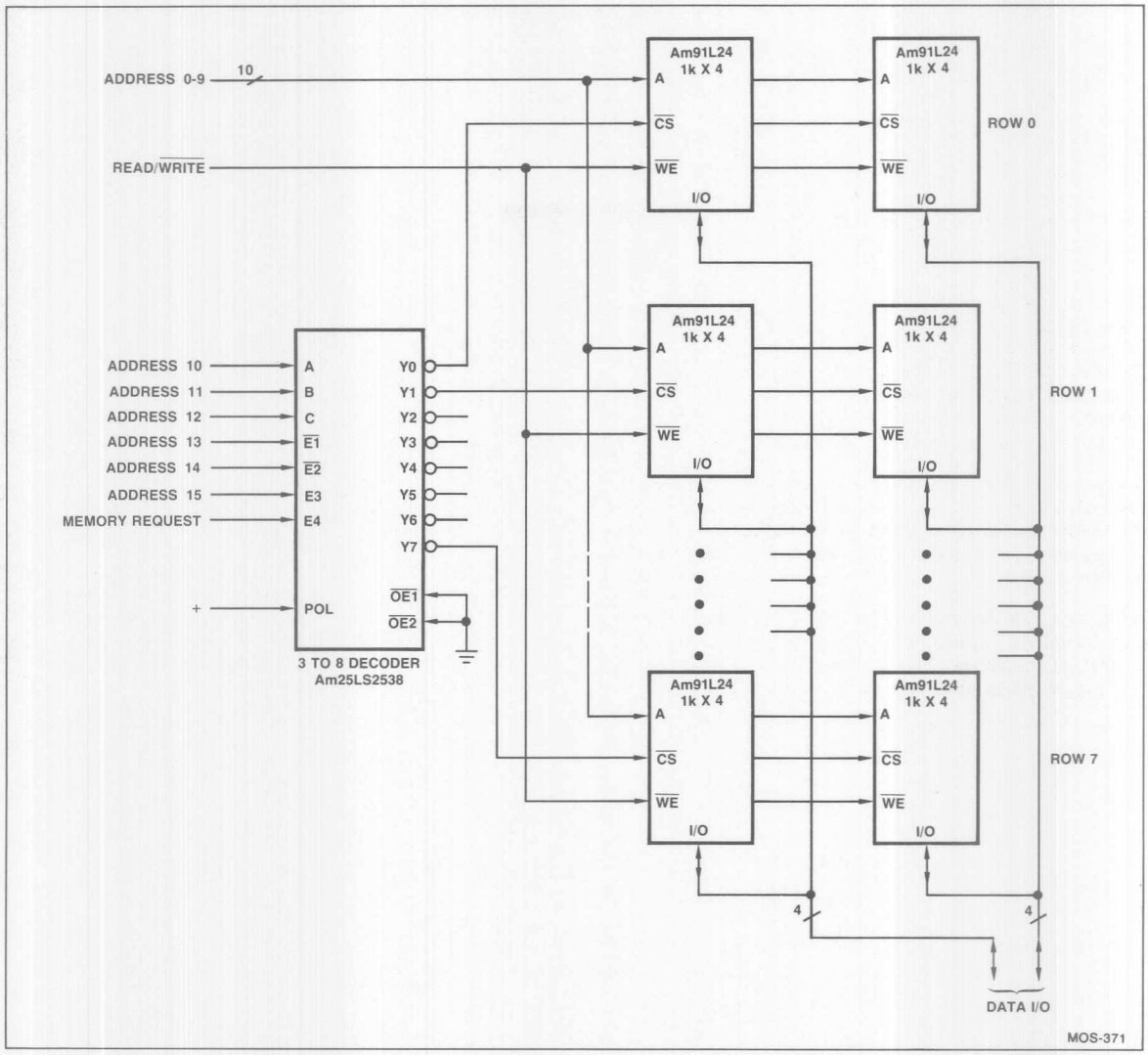



**Figure 7. 8k x 8 Memory System "Clocked" Mode.**

Figure 7 uses the Am25LS2538 to decode more address lines than necessary for a capacity of 8k words. This allows considerable flexibility in where the memory is mapped within a much larger address space. Reassignment of addresses 13, 14 and 15 allows mapping into other locations without additional logic. If Memory Request is not needed, the E4 input may be tied high. In that case the memory will operate with one row active at all times in the same way as Figure 6.

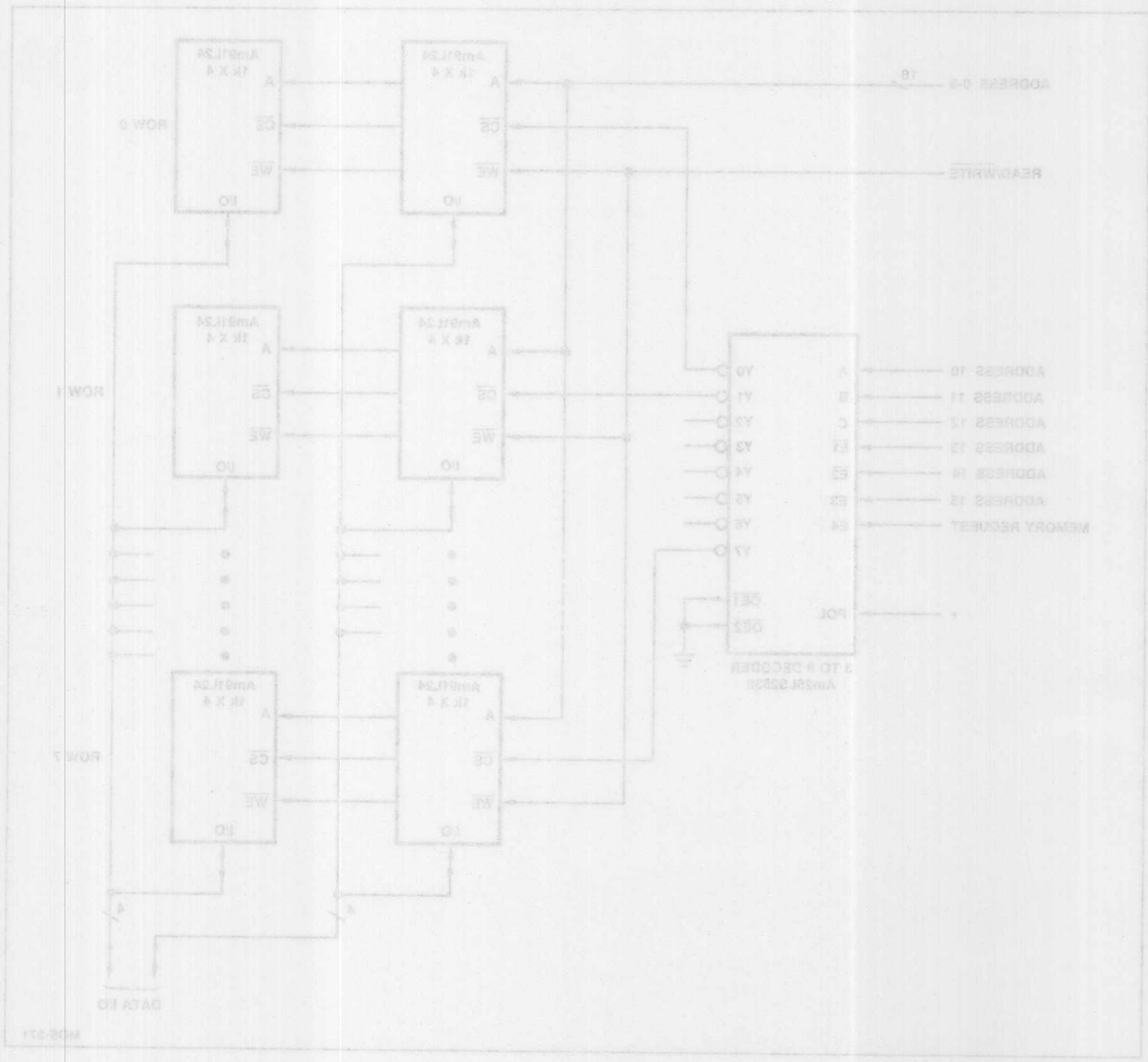



Figure 7. 8k x 8 Memory System "Clocked" Mode.

# UV Erasable-Programmable ROM

3

## NUMERICAL INDEX


| Erasable | | Page |
|---|---|---|
| Am1702A | 256 x 8 | 3-1 |
| Am2708 | 1024 x 8 | 3-7 |
| Am2716 | 2048 x 8 | 3-11 |
| Am2732 | 4096 x 8 | 3-16 |
| Am9708 | 1024 x 8 | 3-7 |
| Am9732 | 4096 x 8 | 3-16 |

# UV Erasable-Programmable ROM

3

## NUMERICAL INDEX


| Erasable | | Page |
|---|---|---|
| Am1702A | 256 x 8 | 3-1 |
| Am2708 | 1024 x 8 | 3-7 |
| Am2716 | 2048 x 8 | 3-11 |
| Am2732 | 4096 x 8 | 3-16 |
| Am9708 | 1024 x 8 | 3-7 |
| Am9732 | 4096 x 8 | 3-16 |

# Am1702A

## 256-Word by 8-Bit Programmable Read Only Memory



### DISTINCTIVE CHARACTERISTICS

- Field programmable 2048 bit ROM
- Access times down to 550 nanoseconds
- 100% tested for programmability
- Inputs and outputs TTL compatible
- Three-state output – wired-OR capability
- Typical programming time of less than 2 minutes/device
- Clocked VGG mode for lower power dissipation
- 100% MIL-STD-883 reliability assurance testing

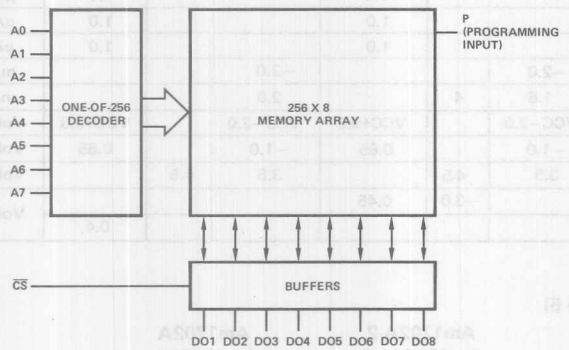
### GENERAL DESCRIPTION

The Am1702A is a 2048-bit electrically programmable ultraviolet light erasable Read Only Memory. It is organized as 256 by 8 bits. It is packaged in a 24 pin dual in-line hermetic cerdip package with a foggy lid.

The transparent lid allows the user to erase any previously stored bit pattern by exposing the die to an ultraviolet (UV) light source. Initially, and after each erasure, all 2048 bits are in the zero state (output low). The data is selectively written into specified address locations by writing in ones.

A low power version, the Am1702AL, is available which permits the VGG input to be clocked for lower average power dissipation.

### BLOCK DIAGRAM




MOS-372

### CONNECTION DIAGRAM




Top View

Pin 1 is marked for orientation

MOS-373

### ORDERING INFORMATION

| Ambient Temperature Specification | Package Type | Clocked VGG | Access Time (ns) | | |
|---|---|---|---|---|---|
| | | | 1000 | 650 | 550 |
| 0°C to +70°C | Hermetic DIP Transparent Window | No | AM1702A | AM1702A-2 | AM1702A-1 |
| | | Yes | AM1702AL | AM1702AL-2 | AM1702AL-1 |
| −55°C to +85°C | Hermetic DIP Transparent Window | No | AM9702AHDL | AM9702A-2HDL | AM9702A-1HDL |
| | | Yes | AM9702ALHDL | AM9702AL-2HDL | AM9702AL-1DHL |

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +85°C |
| Power Dissipation | 1 W |
| Input and Supply Voltages (Operating) | VCC −20 V to VCC +0.5 V |
| Input and Supply Voltages (Programming) | −50 V |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGE, Read Mode (Notes 1, 2)

| Ambient Temperature | VCC | VDD | VGG | VBB |
|---|---|---|---|---|
| 0°C to +70°C | +5.0V ±5% | −9.0V ±5% | −9.0V ±5% | +5.0V ±5% |
| −55°C to +85°C | +5.0V ±5% | −9.0V ±5% | −9.0V ±5% | +5.0V ±5% |

## ELECTRICAL CHARACTERISTICS over operating range (Note 3)

| Parameter | Description | Test Conditions | | Am1702A Am9702A Min. | Typ. | Max. | Am1702AL Am9702AL Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| ICF1 | Output Clamp Current | $T_A$ = 0°C, VO = −1.0V | | | 8 | 14 | | 5.5 | 8 | mA |
| ICF2 | Output Clamp Current | $T_A$ = 25°C, VO = −1.0V | | | | 13 | | 5 | 7 | mA |
| IDD0 | VDD Current (Note 4) | VGG = VCC, IOL = 0mA, $\overline{CS}$ = VCC −2.0, $T_A$ = 25°C | | | | | | 7 | 10 | mA |
| IDD1 | | IOL = 0mA, $\overline{CS}$ = VCC −2.0, $T_A$ = 25°C | | | 35 | 50 | | 35 | 50 | mA |
| IDD2 | | IOL = 0mA, $\overline{CS}$ = 0, $T_A$ = 25°C | | | 32 | 46 | | 32 | 46 | mA |
| IDD3 | | IOL = 0mA, $\overline{CS}$ = VCC −2.0, $T_A$ = 0°C | | | 38 | 60 | | 38 | 60 | mA |
| IGG | VGG Current | | | | | 1.0 | | | 1.0 | μA |
| IL1 | Input Leakage Current | VI = 0V | | | | 1.0 | | | 1.0 | μA |
| IL0 | Output Leakage Current | $\overline{CS}$ = VCC −2.0, VO = 0V | | | | 1.0 | | | 1.0 | μA |
| IOH | Output Source Current | VO = 0V | | −2.0 | | | −2.0 | | | mA |
| IOL | Output Sink Current | VO = 0.45V | | 1.6 | 4 | | 2.0 | | | mA |
| VIH | Input HIGH Level | | | VCC−2.0 | | VCC+0.3 | VCC−2.0 | | VCC+0.3 | Volts |
| VIL | Input LOW Level | | | −1.0 | | 0.65 | −1.0 | | 0.65 | Volts |
| VOH | Output HIGH Level | IOH = −200μA | | 3.5 | 4.5 | | 3.5 | 4.5 | | Volts |
| VOL | Output LOW Level | IOL | 1.6mA | | −3.0 | 0.45 | | | | Volts |
| | | | 2.0mA | | | | | | 0.4 | |

## SWITCHING CHARACTERISTICS over operating range (Note 5)

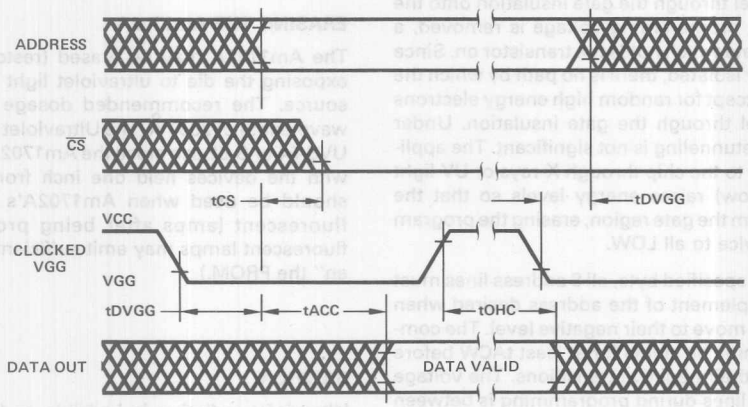
| Parameter | Description | Am1702A-1 Am1702AL-1 Am9702A-1 Am9702AL-1 Min. | Max. | Am1702A-2 Am1702AL-2 Am9702A-2 Am9702AL-2 Min. | Max. | Am1702A Am1702AL Am9702A Am9702AL Min. | Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| tACC | Address to Output Access Time | | 550 | | 650 | | 1000 | ns |
| tCO | Output Delay from $\overline{CS}$ | | 450 | | 350 | | 900 | ns |
| tCS | Chip Select Delay | | 100 | | 300 | | 100 | ns |
| tDVGG | Set-up Time, VGG | 0.3 | | 0.3 | | 0.4 | | μs |
| tOD | Output Deselect | | 300 | | 300 | | 300 | ns |
| tDH | Previous Read Data Valid | | 100 | | 100 | | 100 | ns |
| tOHC | Data Out Valid from VGG (Note 6) | | 5.0 | | 5.0 | | 5.0 | μs |
| freq. | Repetition Rate | | 1.8 | | 1.6 | | 1.0 | MHz |

## CAPACITANCE (Note 7)

| Parameter | Description | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| CI | Input Capacitance | $T_A$ = 25°C | 8 | 15 | pF |
| CO | Output Capacitance | All unused pins are at VCC | 10 | 15 | pF |
| CVGG | VGG Capacitance | | | 30 | pF |

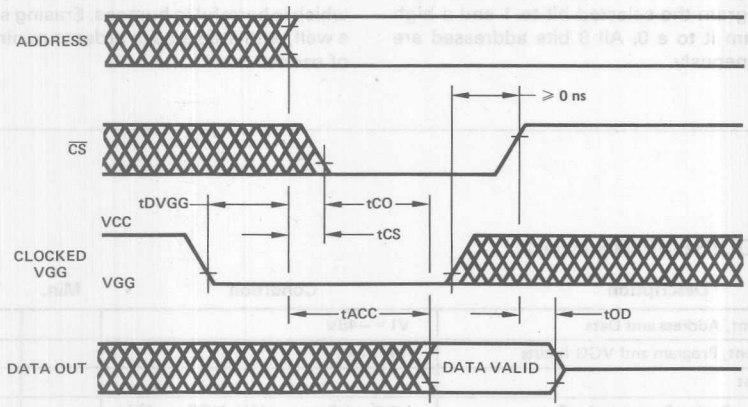
## SWITCHING WAVEFORMS

### READ OPERATION (Note 2)




MOS-374

### DESELECTION




MOS-375

### CLOCKED VGG OPERATION (Note 1)

The VGG input may be clocked between +5V (VCC) and −9V to save power. To read the data, the chip select ($\overline{CS}$) must be low (≤ VIL) and the VGG level must be lowered to −9V at least tDVGG prior to the address selection. Once the data has appeared at the output and the access time has elapsed, VGG may be raised to +5V. The data output will remain stable for tOHC. To deselect the chip, $\overline{CS}$ is raised to ≥ VIH, and the output will go the high impedance state after tOD. The chip will be deselected when $\overline{CS}$ is raised to VIH whether the VGG is at +5V or at −9V.

## PROGRAMMING THE Am1702A

Each storage node in the Am1702A consists of an MOS transistor whose gate is not connected to any circuit element. The transistors are all normally off, making all outputs LOW in an unprogrammed device. A bit is programmed to a HIGH by applying a large negative voltage to the MOS transistor; electrons tunnel through the gate insulation onto the gate itself. When the programming voltage is removed, a charge is left on the gate which holds the transistor on. Since the gate is completely isolated, there is no path by which the charge can escape, except for random high energy electrons which might retunnel through the gate insulation. Under ordinary conditions retunneling is not significant. The application of high energy to the chip through X-rays or UV light (via the quartz window) raises energy levels so that the charge can escape from the gate region, erasing the program and restoring the device to all LOW.

In order to program a specified byte, all 8 address lines must be in the binary complement of the address desired when pulsed VDD and VGG move to their negative level. The complemented address must be stable for at least tACW before VDD and VGG make their negative transitions. The voltage swing of the address lines during programming is between −47V ± 1V and 0V. The addresses must then make a transition to the true state at least tATW before the program pulse is applied. For good data retention, the addresses should be programmed in sequence from 0 to 255, a minimum of 32 times. DO1 through DO8 are used as the data inputs to program the desired pattern. A low level at the data input (−47V ± 1V) will program the selected bit to 1 and a high level (0V) will program it to a 0. All 8 bits addressed are programmed simultaneously.

Programming Boards are available for the Data I/O automatic programmer (part number 1010/1011), for the Spectrum Dynamics programmer (part number 434-549), and for the Pro-Log programmer (part number PM9001).

## ERASING THE Am1702A

The Am1702A may be erased (restored to all LOW's) by exposing the die to ultraviolet light from a high intensity source. The recommended dosage is 6 W-sec/cm$^2$ at a wavelength of 2537 Å. The Ultraviolet Products, Inc., models UVS-54 or S-52 can erase the Am1702A in about 15 minutes, with the devices held one inch from the lamp. (Caution should be used when Am1702A's are inspected under fluorescent lamps after being programmed, as some fluorescent lamps may emit sufficient UV to erase or "soften" the PROM.)

## CAUTION

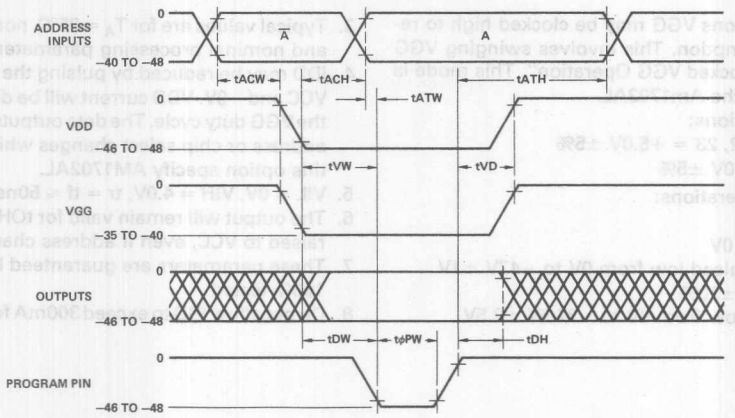
Ultraviolet radiation is invisible and can damage human eyes. Precautions should be taken to avoid exposure to direct or reflected ultraviolet radiation. It will often be convenient to fully enclose the ultraviolet source and the EROMs being erased to prevent accidental exposure.

Ultraviolet lamps can also ionize oxygen and create ozone which is harmful to humans. Erasing should be carried out in a well ventilated area in order to minimize the concentration of ozone.

## PROGRAMMING REQUIREMENTS (Note 2)

| Parameter | Description | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| ILI1P | Input Current, Address and Data | VI = −48V | | | 10 | mA |
| ILI2P | Input Current, Program and VGG Inputs | VI = −48V | | | 10 | mA |
| IBB | VBB Current | | | 0.05 | | mA |
| IDDP | IDD Current During Programming Pulse | VDD = VProg = −48V, VGG = −35V | | 200 | Note 8 | mA |
| VIHP | Input HIGH Voltage | | | | 0.3 | Volts |
| VIL1P | Voltage Applied to Output to Program a HIGH | | −46 | | −48 | Volts |
| VIL2P | Input LOW Level on Address Inputs | | −40 | | −48 | Volts |
| VIL3P | Voltage Applied to VDD and Program Inputs | | −46 | | −48 | Volts |
| VIL4P | Voltage Applied to VGG Input | | −35 | | −40 | Volts |
| tφPW | Programming Pulse Width | VGG = −35V, VDD = VProg = −48V | | | 3.0 | ms |
| tDW | Data Set-up Time | | 25 | | | μs |
| tDH | Data Hold Time | | 10 | | | μs |
| tVW | VGG and VDD Set-up Time | | 100 | | | μs |
| tVD | VGG and VDD Hold Time | | 10 | | 100 | μs |
| tACW | Address Set-up Time (Complement) | | 25 | | | μs |
| tACH | Address Hold Time (Complement) | | 25 | | | μs |
| tATW | Address Set-up Time (True) | | 10 | | | μs |
| tATH | Address Hold Time (True) | | 10 | | | μs |
| | Duty Cycle | | | | 20 | % |

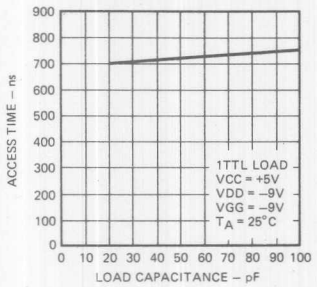
## PROGRAMMING WAVEFORMS



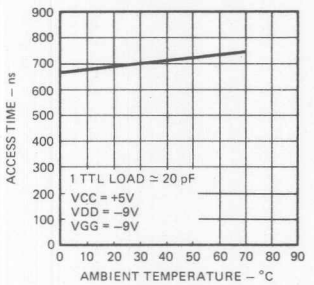

MOS-376

## TYPICAL PERFORMANCE CURVES

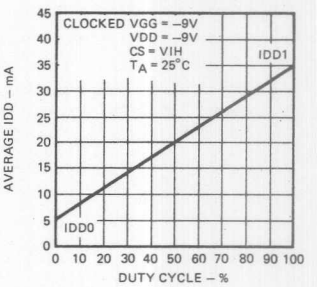
### Access Time Versus Load Capacitance



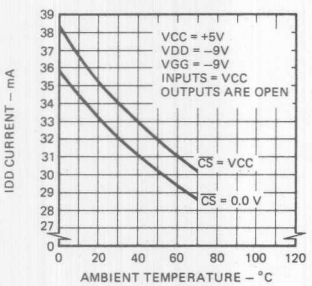

### Access Time Versus Temperature



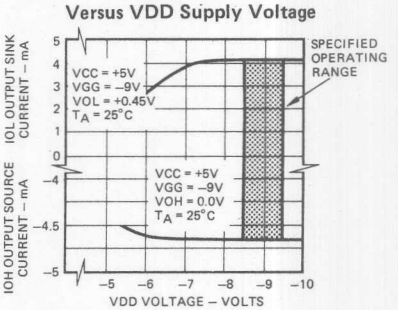

### Average Current Versus Duty Cycle for Clocked VGG



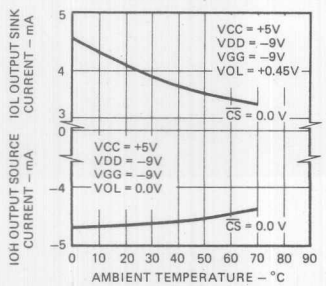

### IDD Current Versus Temperature



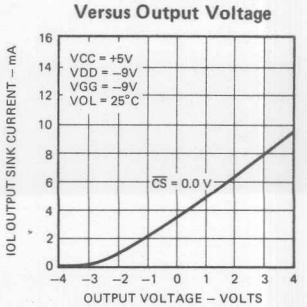

### Output Current Versus VDD Supply Voltage




### Output Current Versus Temperature




### Output Sink Current Versus Output Voltage




MOS-377

1. During read operations VGG may be clocked high to reduce power consumption. This involves swinging VGG up to VCC. See "Clocked VGG Operation". This mode is possible only with the Am1702AL.
2. During Read operations:
   Pins 12, 13, 15, 22, 23 = +5.0V ±5%
   Pins 16, 24 = −9.0V ±5%
   During Program operations:
   $T_A$ = 25°C
   Pins 12, 22, 23 = 0V
   Pins 13, 24 are pulsed low from 0V to −47V ±1V
   Pin 15 = +12.0V ±10%
   Pin 16 is pulsed low from 0V to −37.5V ±2.5V
3. Typical values are for $T_A$ = 25°C, nominal supply voltages and nominal processing parameters.
4. IDD may be reduced by pulsing the VGG supply between VCC and −9V. VDD current will be directly proportional to the VGG duty cycle. The data outputs will be unaffected by address or chip select changes while VGG is at VCC. For this option specify AM1702AL.
5. VIL = 0V, VIH = 4.0V, tr = tf ≤ 50ns, Load = 1 TTL gate.
6. The output will remain valid for tOHC after the VGG pin is raised to VCC, even if address change occurs.
7. These parameters are guaranteed by design and are not 100% tested.
8. Do not allow IDD to exceed 300mA for more than 100μsec.

# Am9708/Am2708

## 1024 x 8 Erasable Read Only Memory



### DISTINCTIVE CHARACTERISTICS

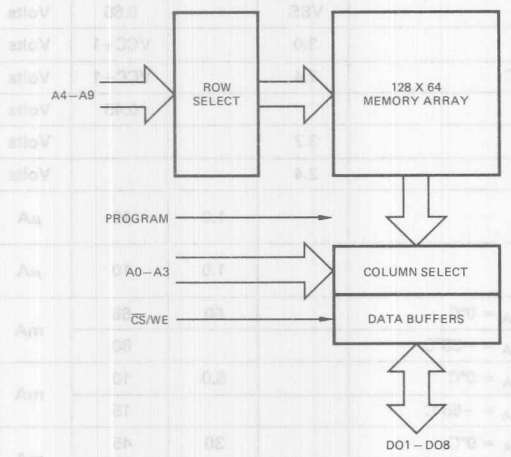
- Direct replacement for Intel 2708/8708
- Interchangeable with Am9208, Am9216 masked ROMs
- Full military temperature operation
- Fast programming time – typically 50 sec.
- TTL compatible interface signals
- Fully static operation – no clocks
- Fast access time – 350ns
- Three-state outputs
- Tested for 100% programmability
- 100% MIL-STD-883 reliability assurance testing

### GENERAL DESCRIPTION

The Am2708 is an 8,192-bit erasable and programmable MOS read-only memory. It is organized as 1024 words by 8 bits per word. Erasing the data in the EROM is accomplished by projecting ultraviolet light through a transparent window for a predetermined time period.

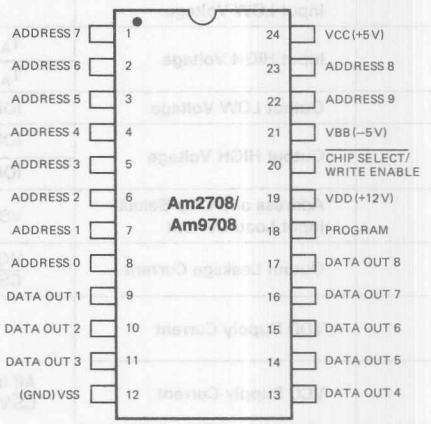
When the Chip Select/Write Enable input is at the high logic level, the device is unselected and the data lines are in their high impedance state. The device is selected when $\overline{CS}$/WE is at the low logic level. The contents of a particular memory location, specified by the 10 address lines, will be available on the data lines after the access time has elapsed. For programming, $\overline{CS}$/WE is connected to +12V and is used in conjunction with the Program input. The Address and Data lines are TTL compatible for all operating and programming modes.

### BLOCK DIAGRAM




MOS-052

### CONNECTION DIAGRAM




Top View

Pin 1 is marked for orientation.

MOS-053

### ORDERING INFORMATION

| Package Type | Ambient Temperature Specification | Order Number |
|---|---|---|
| Hermetic DIP Transparent Window | $0°C \leq T_A \leq +70°C$ | AM2708DC (450ns)<br>AM2708-1DC (350ns) |
| Hermetic DIP Transparent Window | $-55°C \leq T_A \leq +125°C$ | AM9708DM (480ns) |

## MAXIMUM RATINGS above which the useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| All Signal Voltages, except Program and $\overline{CS}$/WE, with Respect to VBB | −0.3V to +15V |
| Program Input Voltage with Respect to VBB | −0.3V to +35V |
| $\overline{CS}$/WE Input with Respect to VBB | −0.3V to +20V |
| VCC and VSS with Respect to VBB | −0.3V to +15V |
| VDD with Respect to VBB | −0.3V to +20V |
| Power Dissipation | 1.5W |

The product described by this specification includes internal circuitry designed to protect input devices from excessive accumulation of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to any voltages that exceed the maximum ratings.

## OPERATING RANGE

| Ambient Temperature | VDD | VCC | VBB | VSS |
|---|---|---|---|---|
| 0°C to +70°C | +12V ±5% | +5V ±5% | −5V ±5% | 0V |
| −55°C to +125°C | +12V ±10% | +5V ±10% | −5V ±10% | 0V |

## PROGRAMMING CONDITIONS

| Ambient Temperature | VDD | VCC | VBB | VSS | $\overline{CS}$/WE | VIHP |
|---|---|---|---|---|---|---|
| +25°C | +12V ± 5% | +5V ± 5% | −5V ± 5% | 0V | +12V ± 5% | 26V ± 1V |

## READ OPERATION
## ELECTRICAL CHARACTERISTICS over operating range (Notes 1, 7)

| Parameters | Description | Test Conditions | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| VIL | Input LOW Voltage | | | VSS | | 0.65 | Volts |
| VIH | Input HIGH Voltage | $T_A$ = 0°C to +70°C | | 3.0 | | VCC+1 | Volts |
| | | $T_A$ = −55°C to +125°C | | 2.4 | | VCC+1 | Volts |
| VOL | Output LOW Voltage | IOL = 1.6mA | | | | 0.45 | Volts |
| VOH | Output HIGH Voltage | IOH = − 100μA | | 3.7 | | | Volts |
| | | IOH = −1.0mA | | 2.4 | | | Volts |
| ILI | Address and Chip Select Input Load Current | VSS ≤ VIN ≤ VCC | | | 1.0 | 10 | μA |
| ILO | Output Leakage Current | VOUT = Worst Case $\overline{CS}$/WE = + 5.0V | | | 1.0 | 10 | μA |
| IDD | VDD Supply Current | All inputs HIGH. $\overline{CS}$/WE = +5.0V | $T_A$ = 0°C | | 50 | 65 | mA |
| | | | $T_A$ = −55°C | | | 80 | |
| ICC | VCC Supply Current | | $T_A$ = 0°C | | 6.0 | 10 | mA |
| | | | $T_A$ = −55°C | | | 15 | |
| IBB | VBB Supply Current | | $T_A$ = 0°C | | 30 | 45 | mA |
| | | | $T_A$ = −55°C | | | 60 | |
| PD | Power Dissipation | $T_A$ = 70°C | | | | 800 | mW |
| CIN | Input Capacitance | $T_A$ = 25°C f = 1MHz All pins at 0V | | | 4.0 | 6.0 | pF |
| COUT | Output Capacitance | | | | 8.0 | 12.0 | pF |

## READ OPERATION
## SWITCHING CHARACTERISTICS over operating range (Notes 2, 7)

| Parameters | Description | Test Conditions | 0°C ≤ $T_A$ ≤ 70°C | | | −55°C ≤ $T_A$ ≤ +125°C | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | | Min. | Max. | |
| | | | | 2708 | 2708-1 | | | |
| tACC | Address to Output Access Time (Note 3) | tr = tf ≤ 20ns Output Load: One Standard TTL Gate Plus 100pF | | 450 | 350 | | 480 | ns |
| tCO | Chip Select to Output on Delay (Note 4) | | | 120 | | | 150 | ns |
| tDF | Chip Select to Output OFF Delay | | 0 | 120 | | 0 | 150 | |
| tOH | Previous Read Data Valid with Respect to Address Change | | 0 | | | 0 | | |

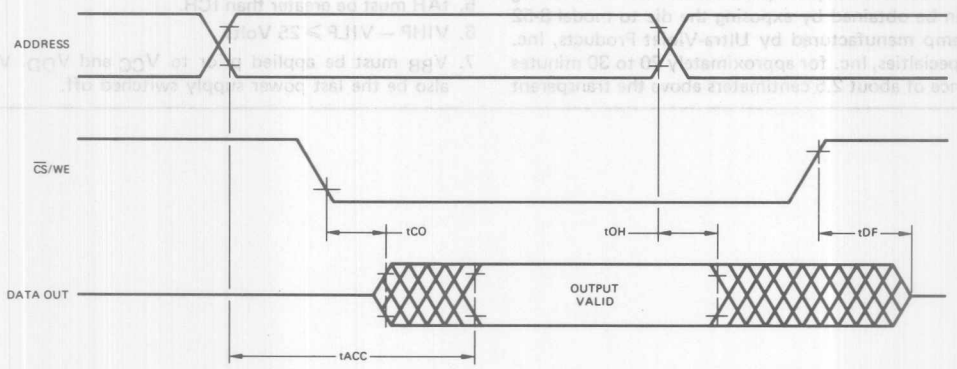
## PROGRAMMING CHARACTERISTICS under programming conditions

| Parameter | Description | Min. | Max. | Units |
|---|---|---|---|---|
| tAS | Address Set Up Time | 10 | | μs |
| tCSS | $\overline{CS}$/WE Set Up Time | 10 | | μs |
| tDS | Data Set Up Time | 10 | | μs |
| tAH | Address Hold Time (Note 5) | 1.0 | | μs |
| tCH | $\overline{CS}$/WE Hold Time (Note 5) | 0.5 | | μs |
| tDH | Data Hold Time | 1.0 | | μs |
| tDF | Chip Select to Output Off Delay | 0 | 120 | ns |
| tDPR | Program to Read Delay | | 10 | μs |
| tPW | Program Pulse Width | 0.1 | 1.0 | ms |
| tPR, tPF | Program Pulse Transition Times | 0.5 | 2.0 | μs |
| VIHW | $\overline{CS}$/WE Input High Level | 11.4 | 12.6 | Volts |
| VIHP | Program Pulse High Level (Note 6) | 25 | 27 | Volts |
| VILP | Program Pulse Low Level (Note 6) | VSS | 1.0 | Volts |

3

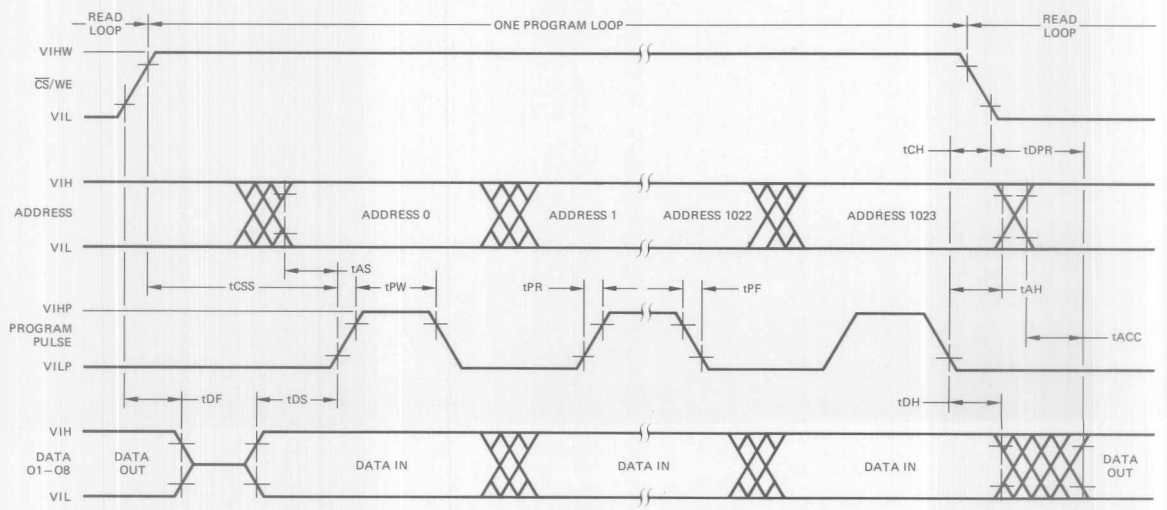
## SWITCHING WAVEFORMS

### READ CYCLE




MOS-054

### PROGRAM MODE (Note 5)




MOS-055

put state will change from HIGH to LOW. Programming of the device is initiated by raising the $\overline{CS}$/WE input to +12V. A memory location is programmed by addressing the device and supplying 8 data bits in parallel to the data out lines. When address and data bits are set up, a programming pulse is applied to the program input. All addresses are programmed sequentially in a similar manner. One pass through all 1024 addresses is considered one program loop. The number of program loops (N) required to complete the programming cycle is a function of the program pulse width (tPW) such that N $\geqslant$ 100ms/tPW requirement is met. Do not apply more than one program pulse per address without sequentially programming all other addresses. There should be N successive loops through all locations. The Program pin will source the IIPL current when it is low (VILP) and $\overline{CS}$/WE is high (VIHW). The Program pin should be actively pulled down to maintain its low level.

## ERASING THE Am2708

The Am2708 can be erased by exposing the die to high-intensity, short-wave, ultra-violet light at a wavelength of 2537 angstroms through the transparent lid. The recommended dosage is ten watt-seconds per square centimeter. This erasing condition can be obtained by exposing the die to model S-52 ultraviolet lamp manufactured by Ultra-Violet Products, Inc. or Product Specialties, Inc. for approximately 20 to 30 minutes from a distance of about 2.5 centimeters above the transparent

## CAUTION

Ultraviolet radiation is invisible and can damage human eyes. Precautions should be taken to avoid exposure to direct or reflected ultraviolet radiation. It will often be convenient to fully enclose the ultraviolet source and the EROMs being erased to prevent accidental exposure.

Ultraviolet lamps can also ionize oxygen and create ozone which can be harmful to humans. Erasing should be carried out in a well ventilated area in order to minimize the concentration of ozone.

## NOTES:

1. Typical values are for $T_A = 25°C$, nominal supply voltages and nominal processing parameters.
2. Timing reference levels (Read) —
   Inputs: High = 2.8V (DC), 2.2V (DM); Low = 0.8V
   Outputs: High = 2.4V, Low = 0.8V
3. Typical access time is 280ns.
4. Typical chip select to output on delay is 60ns.
5. tAH must be greater than tCH.
6. VIHP – VILP $\geqslant$ 25 Volts.
7. $V_{BB}$ must be applied prior to $V_{CC}$ and $V_{DD}$. $V_{BB}$ must also be the last power supply switched off.

# Am2716/Am4716

## 2048 x 8-Bit UV Erasable PROM

3

### DISTINCTIVE CHARACTERISTICS

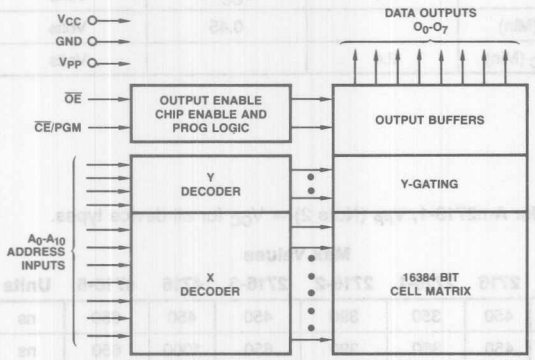
- Direct replacement for Intel 2716
- Interchangeable with Am9218 – 16K ROM
- Single +5V power supply
- Fast access time – 450ns standard with 350ns and 390ns options
- Low power dissipation
  - 525mW active
  - 132mW standby
- Fully static operation – no clocks
- Three-state outputs
- TTL compatible inputs/outputs
- 100% MIL-STD-883 reliability assurance testing

### GENERAL DESCRIPTION

The Am2716/Am4716 is a 16384-bit ultraviolet erasable and programmable read-only memory. It is organized as 2048 words by 8 bits per word, operates from a single +5V supply, has a static standby mode and features fast single address location programming.

Because the Am2716/Am4716 operates from a single +5V supply, it is ideal for use in microprocessor systems. All programming signals are TTL levels, requiring a single pulse. For programming outside of the system, existing EPROM programmers may be used. Locations may be programmed singly, in blocks, or at random. Total programming time for all bits is 100 seconds.

### BLOCK DIAGRAM

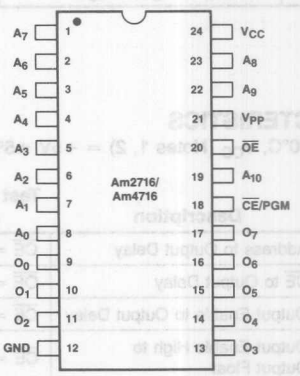



MOS-199

### MODE SELECTION

| Mode \ Pins | $\overline{CE}$/PGM (18) | $\overline{OE}$ (20) | $V_{PP}$ (21) | $V_{CC}$ (24) | Outputs (9-11, 13-17) |
|---|---|---|---|---|---|
| Read | $V_{IL}$ | $V_{IL}$ | +5 | +5 | $D_{OUT}$ |
| Standby | $V_{IH}$ | Don't Care | +5 | +5 | High Z |
| Program | Pulsed $V_{IL}$ to $V_{IH}$ | $V_{IH}$ | +25 | +5 | $D_{IN}$ |
| Program Verify | $V_{IL}$ | $V_{IL}$ | +25 | +5 | $D_{OUT}$ |
| Program Inhibit | $V_{IL}$ | $V_{IH}$ | +25 | +5 | High Z |

### CONNECTION DIAGRAM
Top View




MOS-200

$A_0$-$A_{10}$: Addresses
$O_0$-$O_7$: Outputs
$\overline{CE}$/PGM: Chip Enable/Program
$\overline{OE}$: Output Enable

### ORDERING INFORMATION

| Package Type | Ambient Temperature Specification | Order Number | $t_{ACC}$ (ns) | $t_{CE}$(ns) | $t_{OE}$(ns) |
|---|---|---|---|---|---|
| Hermetic DIP Transparent Window | 0°C ≤ $T_A$ ≤ +70°C | AM2716DC | 450 | 450 | 120 |
| | | AM2716-1DC | 350 | 350 | 120 |
| | | AM2716-2DC | 390 | 390 | 120 |
| | | AM2716-6DC | 450 | 650 | 200 |
| | | AM4716DC | 450 | 1000 | 200 |
| | | AM4716-6DC | 650 | 650 | 200 |

**MAXIMUM RATINGS** above which the useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65 to +125°C |
| Ambient Temperature Under Bias | −10 to +80°C |
| Voltage on All Inputs/Outputs (except $V_{PP}$) with Respect to GND | +6 to −0.3V |
| Voltage on $V_{PP}$ During Program with Respect to GND | +26.5 to −0.3V |

## READ OPERATION

## DC CHARACTERISTICS

0°C ≤ $T_A$ ≤ +70°C, $V_{CC}$ (Notes 1, 2) = +5V ±5%, except +5V ±10% for Am2716-1, $V_{PP}$ (Note 2) = $V_{CC}$ for all device types.

| Parameters | Description | Test Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN}$ = 5.25V/0V | | 10 | μA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = 5.25V/0V | | 10 | μA |
| $I_{PP1}$ (Note 2) | $V_{PP}$ Current | $V_{PP}$ = 5.25V | | 5 (Note 3) | mA |
| $I_{CC1}$ (Note 2) | $V_{CC}$ Current (Standby) | $\overline{CE}$ = $V_{IH}$, $\overline{OE}$ = $V_{IL}$ | | 25 | mA |
| $I_{CC2}$ (Note 2) | $V_{CC}$ Current (Active) | $\overline{OE}$ = $\overline{CE}$ = $V_{IL}$ | | 100 | mA |
| $V_{IL}$ | Input Low Voltage | | −0.1 | 0.8 | Volts |
| $V_{IH}$ | Input High Voltage | | 2.0 | $V_{CC}$+1 | Volts |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1mA @ $V_{CC}$ (Min) | | 0.45 | Volts |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = −400μA @ $V_{CC}$ (Min) | 2.4 | | Volts |

## AC CHARACTERISTICS

0°C ≤ $T_A$ ≤ +70°C, $V_{CC}$ (Notes 1, 2) = +5V ±5%, except +5V ±10% for Am2716-1, $V_{PP}$ (Note 2) = $V_{CC}$ for all device types.

| Parameters | Description | Test Conditions (Note 4) | Min Values | Max Values 2716 | 2716-1 | 2716-2 | 2716-6 | 4716 | 4716-6 | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{ACC}$ | Address to Output Delay | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$ | | 450 | 350 | 390 | 450 | 450 | 650 | ns |
| $t_{CE}$ | $\overline{CE}$ to Output Delay | $\overline{OE}$ = $V_{IL}$ | | 450 | 350 | 390 | 650 | 1000 | 650 | ns |
| $t_{OE}$ | Output Enable to Output Delay | $\overline{CE}$ = $V_{IL}$ | | 120 | 120 | 120 | 200 | 200 | 200 | ns |
| $t_{DF}$ | Output Enable High to Output Float | $\overline{CE}$ = $V_{IL}$ | 0 | 100 | 100 | 100 | 100 | 100 | 100 | ns |
| $t_{OH}$ | Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$ | 0 | | | | | | | ns |

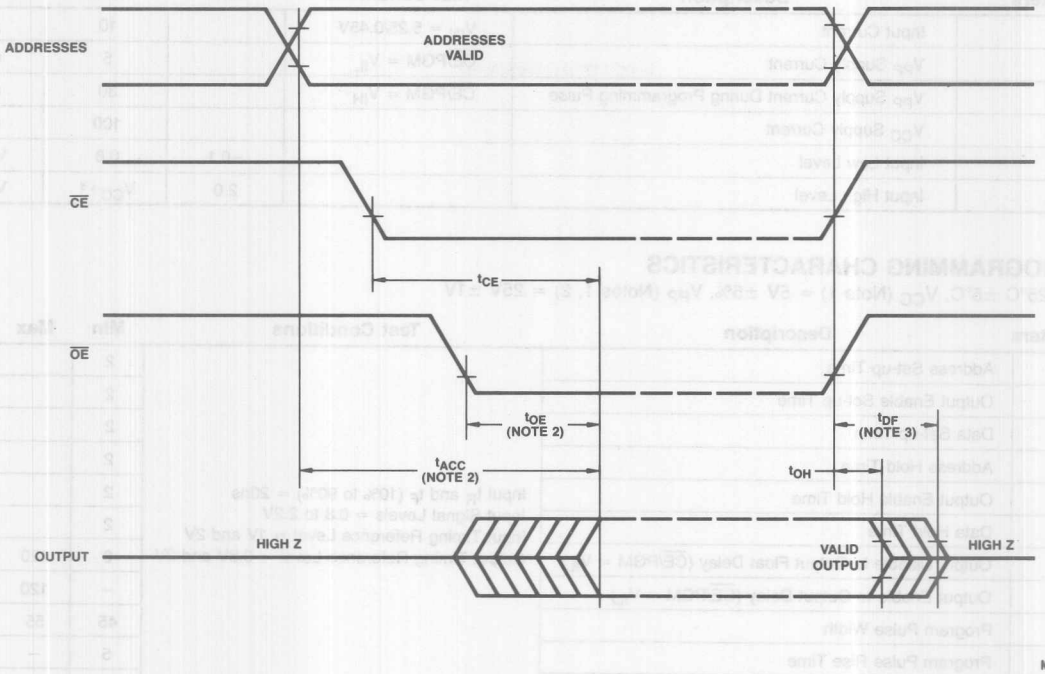
## CAPACITANCE (Note 5)

$T_A$ = +25°C, f = 1MHz

| Parameters | Description | Test Conditions | Typ | Max | Units |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 4 | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 8 | 12 | pF |

Notes: 1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. $V_{PP}$ may be connected directly to $V_{CC}$ except during programming. The supply current would then be the sum of $I_{CC}$ and $I_{PP1}$.
3. 8mA for Am4716 and Am4716-6.
4. Other Test Conditions: a) Output Load: 1 TTL gate and $C_L$ = 100pF
   b) Input Rise and Fall Times: ≤20ns
   c) Input Pulse Levels: 0.8 to 2.2V
   d) Timing Measurement Reference Level:
      Inputs: 1V and 2V
      Outputs: 0.8V and 2V
5. This parameter is only sampled and is not 100% tested.

## AC WAVEFORMS (Note 1)




MOS-201

Notes: 1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{ACC}$.
3. $t_{DF}$ is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

## PROGRAM OPERATION

### DC PROGRAMMING CHARACTERISTICS

$T_A$ = +25°C ±5°C, $V_{CC}$ (Note 1) = 5V ±5%, $V_{PP}$ (Notes 1, 2) = 25V ±1V

| Parameters | Description | Test Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Current | $V_{IN}$ = 5.25/0.45V | | 10 | μA |
| $I_{PP1}$ | $V_{PP}$ Supply Current | $\overline{CE}$/PGM = $V_{IL}$ | | 5 | mA |
| $I_{PP2}$ | $V_{PP}$ Supply Current During Programming Pulse | $\overline{CE}$/PGM = $V_{IH}$ | | 30 | mA |
| $I_{CC}$ | $V_{CC}$ Supply Current | | | 100 | mA |
| $V_{IL}$ | Input Low Level | | −0.1 | 0.8 | Volts |
| $V_{IH}$ | Input High Level | | 2.0 | $V_{CC}$+1 | Volts |

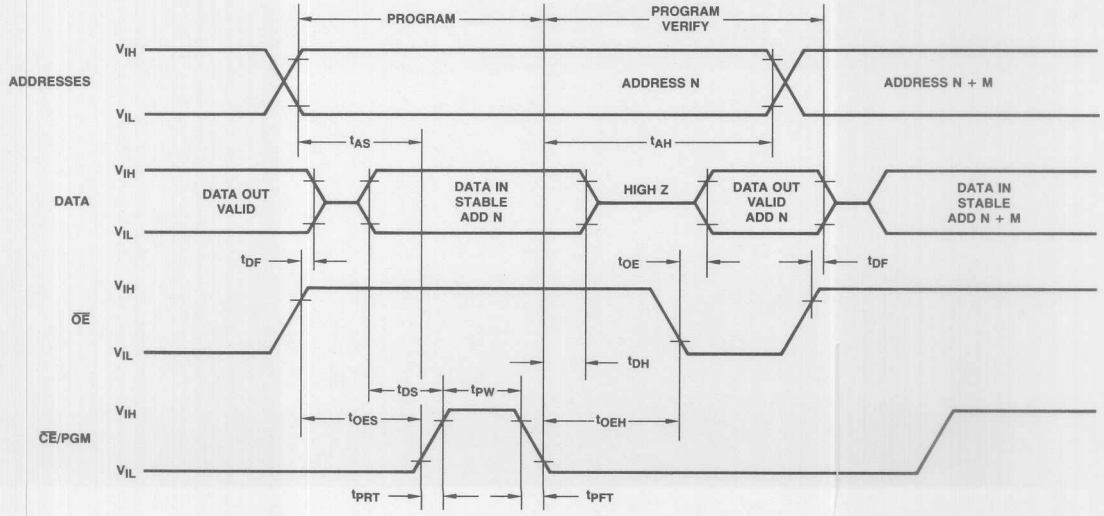
### AC PROGRAMMING CHARACTERISTICS

$T_A$ = +25°C ±5°C, $V_{CC}$ (Note 1) = 5V ±5%, $V_{PP}$ (Notes 1, 2) = 25V ±1V

| Parameters | Description | Test Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $t_{AS}$ | Address Set-up Time | Input $t_R$ and $t_F$ (10% to 90%) = 20ns<br>Input Signal Levels = 0.8 to 2.2V<br>Input Timing Reference Level = 1V and 2V<br>Output Timing Reference Level = 0.8V and 2V | 2 | | μs |
| $t_{OES}$ | Output Enable Set-up Time | | 2 | | μs |
| $t_{DS}$ | Data Set-up Time | | 2 | | μs |
| $t_{AH}$ | Address Hold Time | | 2 | | μs |
| $t_{OEH}$ | Output Enable Hold Time | | 2 | | μs |
| $t_{DH}$ | Data Hold Time | | 2 | | μs |
| $t_{DF}$ | Output Disable to Output Float Delay ($\overline{CE}$/PGM = $V_{IL}$) | | 0 | 120 | ns |
| $t_{OE}$ | Output Enable to Output Delay ($\overline{CE}$/PGM = $V_{IL}$) | | – | 120 | ns |
| $t_{PW}$ | Program Pulse Width | | 45 | 55 | ms |
| $t_{PRT}$ | Program Pulse Rise Time | | 5 | – | ns |
| $t_{PFT}$ | Program Pulse Fall Time | | 5 | – | ns |

Notes: 1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. $V_{PP}$ must not be greater than 26 volts including overshoot. Permanent device damage may occur if the device is taken out of or put into the socket when $V_{PP}$ = 25 volts is applied. Also, during $\overline{OE}$ = $\overline{CE}$/PGM = $V_{IH}$, $V_{PP}$ must not be switched from 5 volts to 25 volts or vice versa.

### PROGRAMMING WAVEFORMS




MOS-202

## ERASING THE Am2716/Am4716

In order to clear all locations of their programmed contents, it is necessary to expose the Am2716/Am4716 to an ultraviolet light source. A dosage of 15 Wseconds/cm$^2$ is required to completely erase an Am2716/Am4716. This dosage can be obtained by exposure to an ultraviolet lamp [wavelength of 2537 Angstroms (Å)] with intensity of 12000$\mu$W/cm$^2$ for 15 to 20 minutes. The Am2716/Am4716 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am2716/Am4716, and similar devices, will erase with light sources having wavelengths shorter than 4000 Angstroms. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to florescent light and sunlight will eventually erase the Am2716/Am4716, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

## PROGRAMMING THE Am2716/Am4716

Upon delivery, or after each erasure the Am2716/Am4716 has all 16384 bits in the "1," or high state. "0s" are loaded into the Am2716/Am4716 through the procedure of programming.

The programming mode is entered when +25V is applied to the $V_{PP}$ pin and when $\overline{OE}$ is at $V_{IH}$. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50msec, TTL high level pulse is applied to the $\overline{CE}$/PGM input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55msec. Therefore, applying a DC level to the $\overline{CE}$/PGM input is prohibited when programming.

## READ MODE

The Am2716/Am4716 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the outputs pins, independent of device selection. Assuming that addresses are stable, address access time ($t_{ACC}$) is equal to the delay from $\overline{CE}$ to output ($t_{CE}$) for all devices except Am2716-6 and Am4716. Data is available at the outputs 120ns or 200ns ($t_{OE}$) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

## STANDBY MODE

The Am2716/Am4716 has a standby mode which reduces the active power dissipation by 75%, from 525mW to 132mW. The Am2716/Am4716 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

## OUTPUT OR-TIEING

To accommodate multiple memory connections, a 2-line control function is provided to allow for:

1. Low memory power dissipation
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

## PROGRAM INHIBIT

Programming of multiple Am2716/Am4716s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel Am2716/Am4716s may be common. A TTL level program pulse applied to an Am2716/Am4716's $\overline{CE}$/PGM input with $V_{PP}$ at 25V will program that Am2716/Am4716. A low level $\overline{CE}$/PGM input inhibits the other Am2716/Am4716s from being programmed.

## PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with $V_{PP}$ at 25V. Except during programming and program verify, $V_{PP}$ must be at $V_{CC}$.

# Am9732/Am2732

## 4096 x 8-Bit UV Erasable PROM

### DISTINCTIVE CHARACTERISTICS

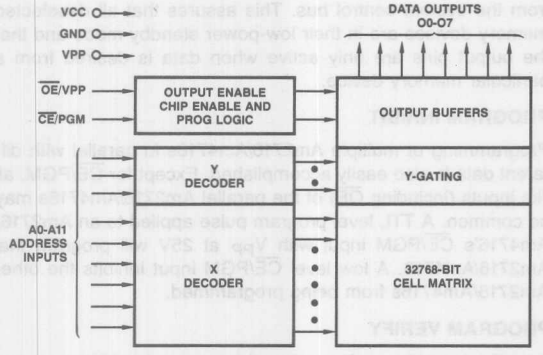
- Direct replacement for Intel 2732
- Pin compatible with Am9233 – 32K ROM
- Single +5V power supply
- Fast access time – 450ns
- Low power dissipation
  - –787mW active
  - –157mW standby
- Fully static operation – no clocks
- Three-state outputs
- TTL compatible inputs/outputs
- 100% MIL-STD-883 reliability assurance testing

### GENERAL DESCRIPTION

The Am2732 is a 32768-bit ultraviolet erasable and programmable read-only memory. It is organized as 4096 words by 8 bits per word, operates from a single +5V supply, has a static standby mode, and features fast single address location programming.

Because the Am2732 operates from a single +5V supply, it is ideal for use in microprocessor systems. All programming signals are TTL levels, requiring a single pulse. For programming outside of the system, existing EPROM programmers may be used. Locations may be programmed singly, in blocks, or at random. Total programming time for all bits is 200 seconds.

### BLOCK DIAGRAM

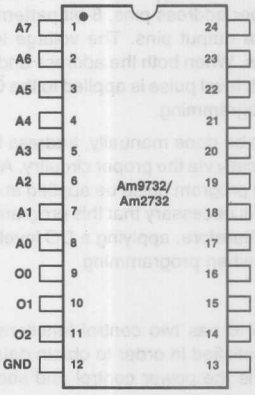



MOS-490

### MODE SELECTION

| Mode \ Pins | CE/PGM (18) | OE/VPP (20) | VCC (24) | Outputs (9-11, 13-17) |
|---|---|---|---|---|
| Read | VIL | VIL | +5 | DOUT |
| Standby | VIH | Don't Care | +5 | High Z |
| Program | VIL | VPP | +5 | DIN |
| Program Verify | VIL | VIL | +5 | DOUT |
| Program Inhibit | VIH | VPP | +5 | High Z |

### CONNECTION DIAGRAM




MOS-491

Top View

Pin 1 is marked for orientation.

A0-A11: Addresses
O0-O7: Outputs
CE/PGM: Chip Enable/Program
OE/VPP: Output Enable

### ORDERING INFORMATION

| Package Type | Ambient Temperature Specification | Order Number | |
|---|---|---|---|
| | | 450ns | 550ns |
| Hermetic DIP Transparent Window | $0°C \leq T_A \leq +70°C$ | AM2732DC | AM2732-6DC |

| **MAXIMUM RATINGS** above which the useful life may be impaired | |
|---|---|
| Storage Temperature | −65 to +125°C |
| Ambient Temperature Under Bias | −10 to +80°C |
| Voltage on All Inputs/Outputs (Except $\overline{OE}$/VPP) with Respect to GND | +6 to −0.3V |
| $\overline{OE}$/VPP with Respect to GND | +26.5 to −0.3V |



## READ OPERATION

### DC CHARACTERISTICS

$0°C \leq T_A \leq +70°C$, VCC = +5V ±5%

| Parameters | Description | Test Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| ILI | Input Load Current | VIN = 5.25V | | 10 | μA |
| ILO | Output Leakage Current | VOUT = 5.25V | | 10 | μA |
| ICC1 | VCC Current (Standby) | $\overline{CE}$ = VIH, $\overline{OE}$ = VIL | | 30 | mA |
| ICC2 | VCC Current (Active) | $\overline{OE}$ = $\overline{CE}$ = VIL | | 150 | mA |
| VIL | Input Low Voltage | | −0.1 | 0.8 | Volts |
| VIH | Input High Voltage | | 2.0 | VCC+1 | Volts |
| VOL | Output Low Voltage | IOL = 2.1mA | | 0.45 | Volts |
| VOH | Output High Voltage | IOH = −400μA | 2.4 | | Volts |

### AC CHARACTERISTICS

$0°C \leq T_A \leq +70°C$, VCC = +5V ±5%

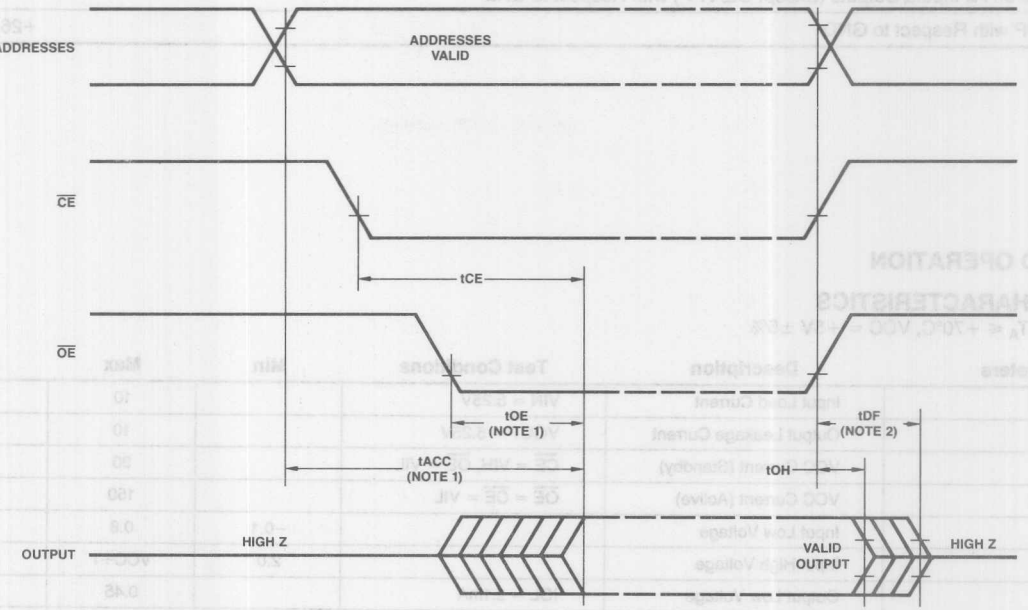
| Parameters | Description | Test Conditions | | Am2732 Min | Am2732 Max | Am2732-6 Min | Am2732-6 Max | Units |
|---|---|---|---|---|---|---|---|---|
| tACC | Address to Output Delay | Output Load: 1 TTL gate and CL = 100pF<br>Input Rise and Fall Times: ≤20ns<br>Input Pulse Levels: 0.8 to 2.2V<br>Timing Measurement Reference Level:<br>Inputs: 1V and 2V<br>Outputs: 0.8V and 2V | $\overline{CE}$ = $\overline{OE}$ = VIL | | 450 | | 550 | ns |
| tCE | $\overline{CE}$ to Output Delay | | $\overline{OE}$ = VIL | | 450 | | 550 | ns |
| tOE | Output Enable to Output Delay | | $\overline{CE}$ = VIL | | 120 | | 120 | ns |
| tDF | Output Enable High to Output Float | | $\overline{CE}$ = VIL | 0 | 100 | 0 | 100 | ns |
| tOH | Address to Output Hold | | $\overline{CE}$ = $\overline{OE}$ = VIL | 0 | | 0 | | ns |

### CAPACITANCE (Note 1)

$T_A$ = +25C, f = 1MHz

| Parameters | Description | Test Conditions | Typ | Max | Units |
|---|---|---|---|---|---|
| CIN1 | Input Capacitance (Except $\overline{OE}$/VPP) | VIN = 0V | 4 | 6 | pF |
| CIN2 | $\overline{OE}$/VPP Input Capacitance | VIN = 0V | | 20 | pF |
| COUT | Output Capacitance | VOUT = 0V | | 12 | pF |

Note: 1. This parameter is only sampled and is not 100% tested.




MOS-492

Notes: 1. $\overline{OE}$ may be delayed up to 330ns after the falling edge of $\overline{CE}$ without impact on tACC.
2. tDF is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

## PROGRAM OPERATION

### DC PROGRAMMING CHARACTERISTICS

$T_A$ = +25°C ±5°C, VCC = 5V ±5%, VPP = 25V ±1V

| Parameters | Description | Test Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| ILI | Input Current (All Inputs) | VIN = VIL or VIH | | 10 | μA |
| VOL | Output Low Voltage During Verify | IOL = 2.1mA | | 0.45 | Volts |
| VOH | Output High Voltage During Verify | IOH = −400μA | 2.4 | | Volts |
| ICC | VCC Supply Current | | | 150 | mA |
| VIL | Input Low Level (All Inputs) | | −0.1 | 0.8 | Volts |
| VIH | Input High Level (All Inputs Except $\overline{OE}$/VPP) | | 2.0 | VCC+1 | Volts |
| IPP | VPP Supply Current | $\overline{CE}$ = VIL, $\overline{OE}$ = VPP | | 30 | mA |

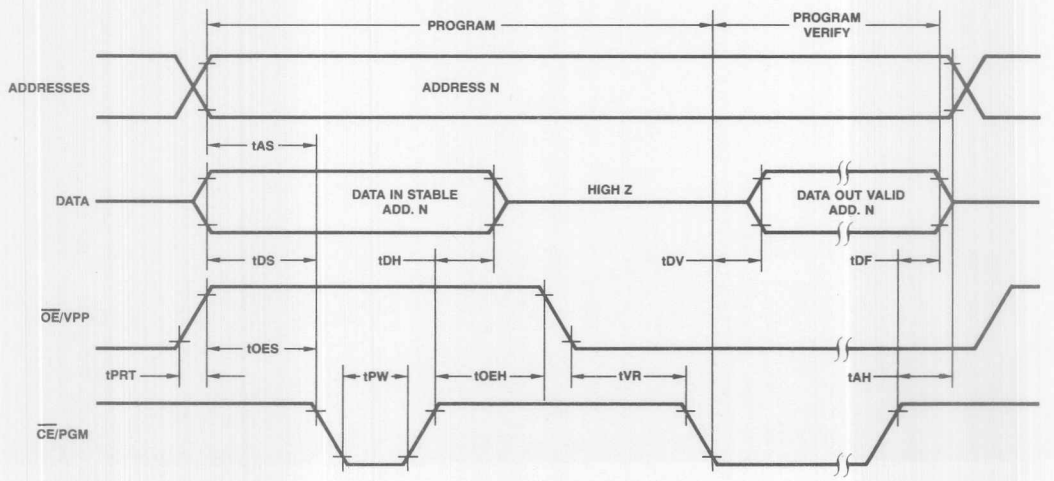
### AC PROGRAMMING CHARACTERISTICS (Note 1)

$T_A$ = +25°C ±5°C, VCC = 5V ±5%, VPP = 25V ±1V

| Parameters | Description | Test Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| tAS | Address Set-up Time | Input tR and tF (10% to 90%) = 20ns<br>Input Signal Levels = 0.8 to 2.2V<br>Timing Measurement Reference Level:<br>Inputs: 1V and 2V<br>Outputs: 0.8V and 2V | 2 | | μs |
| tOES | Output Enable Set-up Time | | 2 | | μs |
| tDS | Data Set-up Time | | 2 | | μs |
| tAH | Address Hold Time | | 0 | | μs |
| tOEH | Output Enable Hold Time | | 2 | | μs |
| tDH | Data Hold Time | | 2 | | μs |
| tDF | Chip Enable to Output Float Delay | | 0 | 120 | ns |
| tDV | Data Valid From $\overline{CE}$ ($\overline{CE}$ = VIL, $\overline{OE}$ = VIL) | | – | 1 | μs |
| tPW | Program Pulse Width | | 45 | 55 | ms |
| tPRT | Program Pulse Rise Time | | 50 | – | ns |
| tVR | VPP Recovery Time | | 2 | – | μs |

Note: 1. When programming the Am2732, a 0.1μF capacitor is required across $\overline{OE}$/VPP and ground to suppress spurious voltage transients which may damage the device.

### PROGRAMMING WAVEFORMS




MOS-493

### ERASING THE Am2732

In order to clear all locations of their programmed contents, it is necessary to expose the Am2732 to an ultraviolet light source. A dosage of 15 Wseconds/cm$^2$ is required to completely erase an Am2732. This dosage can be obtained by exposure to an ultraviolet lamp [(wavelength of 2537 Angstroms (Å)] with intensity of 12000$\mu$W/cm$^2$ for 15 to 20 minutes. The Am2732 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am2732, and similar devices, will erase with light sources having wavelengths shorter than 4000 Angstroms. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am2732, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

### PROGRAMMING THE Am2732

Upon delivery, or after each erasure the Am2732 has all 32768 bits in the "1", or high state. "0"s are loaded into the Am2732 through the procedure of programming.

The programming mode is entered when +25V is applied to the $\overline{OE}$/VPP pin. A 0.1$\mu$F capacitor must be placed across $\overline{OE}$/VPP and ground to suppress spurious voltage transients which may damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50msec, TTL low level pulse is applied to the $\overline{CE}$/PGM input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55msec. Therefore, applying a DC low level to the $\overline{CE}$/PGM input is prohibited when programming.

### READ MODE

The Am2732 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$/VPP) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the outputs 120ns (tOE) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least tACC – tOE.

### STANDBY MODE

The Am2732 has a standby mode which reduces the active power dissipation by 80%, from 787mW to 157mW. The Am2732 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

### OUTPUT OR-TIEING

To accommodate multiple memory connections, a 2 line control function is provided to allow for:

1. Low memory power dissipation
2. Assurance that output bus contention will not occur.

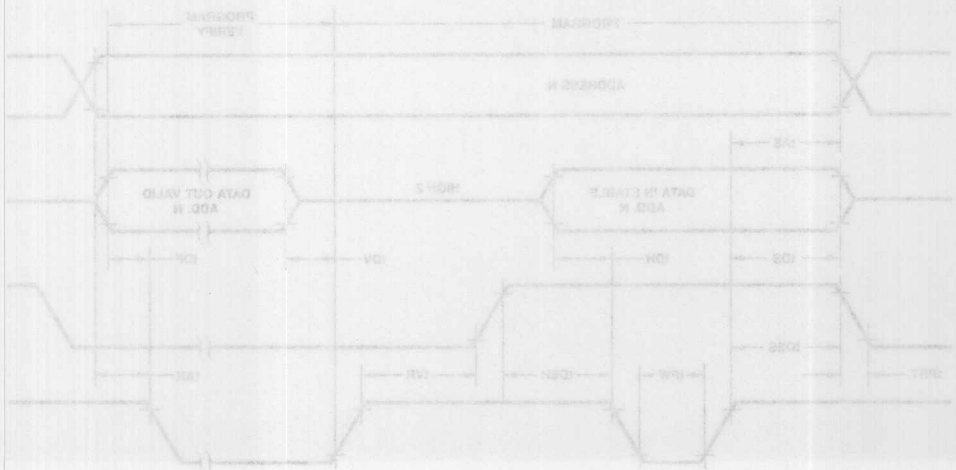
It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

### PROGRAM INHIBIT

Programming of multiple Am2732s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel Am2732s may be common. A TTL level program pulse applied to an Am2732's $\overline{CE}$/PGM input with VPP at 25V will program that Am2732. A high level $\overline{CE}$/PGM input inhibits the other Am2732 from being programmed.

### PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify must be performed with $\overline{OE}$/VPP and $\overline{CE}$ at VIL. Data should be verified tDV after the falling edge of $\overline{CE}$.



# Read-Only Memories

4

## NUMERICAL INDEX


| Mask Programmed | | Page |
|---|---|---|
| Am3514 | 512 x 8 | 4-5 |
| Am9208 | 1024 x 8 | 4-1 |
| Am9214 | 512 x 8 | 4-5 |
| Am9216 | 2048 x 8 | 4-11 |
| Am9217/8316A | 2048 x 8 | 4-15 |
| Am9218/8316E | 2048 x 8 | 4-18 |
| Am9232 | 4096 x 8 | 4-21 |
| Am9233 | 4096 x 8 | 4-21 |

# NUMERICAL INDEX


| Mask Programmed | | Page |
|---|---|---|
| Am3514 | 512 x 8 | 4-5 |
| Am9208 | 1024 x 8 | 4-1 |
| Am9214 | 512 x 8 | 4-5 |
| Am9216 | 2048 x 8 | 4-11 |
| Am9217/83190A | 2048 x 8 | 4-15 |
| Am9218/83160 | 2048 x 8 | 4-18 |
| Am9232 | 4096 x 8 | 4-27 |
| Am9233 | 4096 x 8 | 4-21 |

# Am9208

## 1024 x 8 Read Only Memory

### DISTINCTIVE CHARACTERISTICS

- 1024 x 8 organization
- High speed — 400ns access time
- Fully capacitive inputs — simplified driving
- 2 fully programmable chip selects — increased flexibility
- Logic voltage levels compatible to TTL
- Three-state output buffers — simplified expansion
- Standard supply voltages — +12V, +5.0V
- No $V_{BB}$ supply required
- N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing
- Direct plug-in replacement for Intel 8308/2308 and T.I. 4700

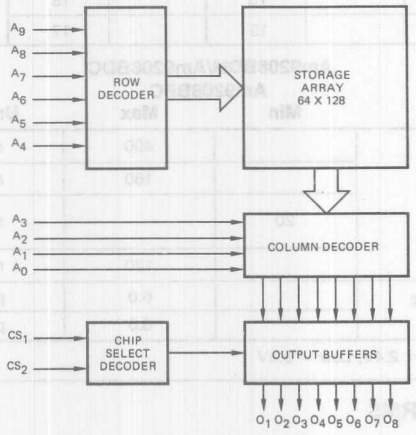
### FUNCTIONAL DESCRIPTION

The Am9208 devices are high performance, 8192 bit, static, mask programmed, read only memories. Each memory is implemented as 1024 words by 8 bits per word. This organization simplifies the design of small memory systems and permits incremental memory sizes as small as 1024 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

Two Chip Select input signals are logically ANDed together to provide control of the output buffers. Each Chip Select polarity may be specified by the customer thus allowing the addressing of 4 memory chips without external gating. The outputs of unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9208 devices and other three-state components.

These memories are fully static and require no clock signals of any kind. A selected chip will output data from a location specified by whatever address is present on the address input lines. The Am9208 is pin compatible with the Am9216 which is a 16k-bit mask programmed ROM. Input and output voltage levels are compatible to TTL specifications, providing simplified interfacing.

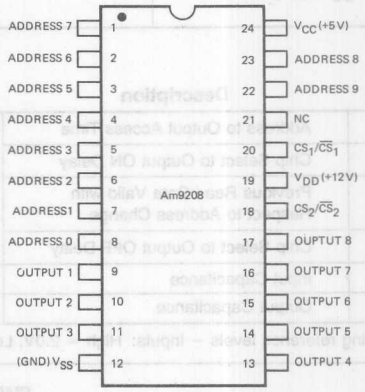
### BLOCK DIAGRAM




MOS-378

### CONNECTION DIAGRAM

Top View




Note: Pin 1 is marked for orientation.

MOS-379

### ORDERING INFORMATION

| Package Type | Ambient Temperature Specification | Access Time 400ns |
|---|---|---|
| Hermetic DIP | 0°C ≤ $T_A$ ≤ 70°C | AM9208BDC |
| | −55°C ≤ $T_A$ ≤ +125°C | AM9208BDM |
| Plastic DIP | 0°C ≤ $T_A$ ≤ 70°C | AM9208BPC |

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| $V_{DD}$ with Respect to $V_{SS}$ | 15V |
| $V_{CC}$ with Respect to $V_{SS}$ | +7.0V |
| DC Voltage Applied to Outputs | −0.5V to +7.0V |
| DC Input Voltage | −0.5V to +7.0V |
| Power Dissipation | 1.0W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGE

| Part Number | Ambient Temperature | $V_{DD}$ | $V_{CC}$ | $V_{SS}$ |
|---|---|---|---|---|
| Am9208DC | $0°C \leq T_A \leq +70°C$ | +12V ± 5% | +5.0V ± 5% | 0V |
| Am9208DM | $-55°C \leq T_A \leq +125°C$ | +12V ± 10% | +5.0V ± 10% | 0V |

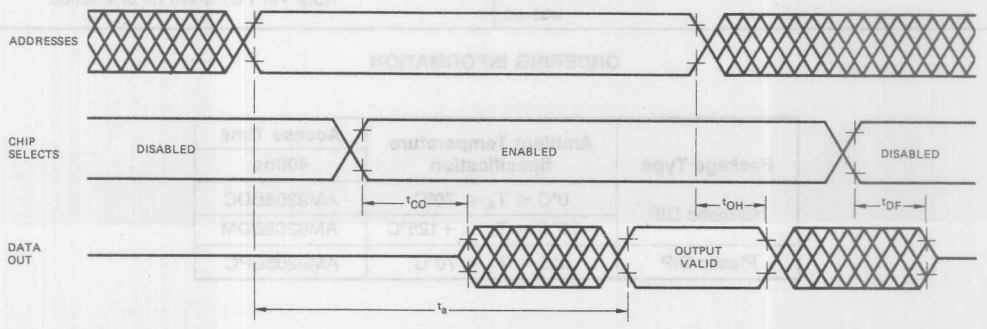
## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions | | Am9208DC/PC Min. | Am9208DC/PC Max. | Am9208DM Min. | Am9208DM Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -1.0mA$ | | 3.7 | | 3.7 | | Volts |
| | | $I_{OH} = -4.0mA$ | | 2.4 | | 2.4 | | |
| $V_{OL}$ | Output LOW Voltage | $I_{OL} = 3.2mA$ | | | 0.4 | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | | 2.4 | $V_{CC}+1.0$ | 2.6 | $V_{CC}+1.0$ | Volts |
| $V_{IL}$ | Input LOW Voltage | | | −0.5 | 0.8 | −0.5 | 0.8 | Volts |
| $I_{LO}$ | Output Leakage Current | Chip disable | | | 10 | | 10 | μA |
| $I_{LI}$ | Input Leakage Current | | | | 10 | | 10 | μA |
| $I_{DD}$ | $V_{DD}$ Supply Current | Selected | Am9208B/C | | 35 | | 43 | mA |
| | | | Am9208D | | 44 | | 50 | |
| | | Deselected | Am9208B/C | | 48 | | 53 | |
| | | | Am9208D | | 55 | | 61 | |
| $I_{CC}$ | $V_{CC}$ Supply Current | | Am9208B/C | | 13 | | 15 | mA |
| | | | Am9208D | | 15 | | 17 | |

| Parameters | Description | Test Conditions | Am9208BDM/Am9208BDC/Am9208BPC Min | Max | Units |
|---|---|---|---|---|---|
| $t_a$ | Address to Output Access Time | $t_r = t_f = 20ns$ Output load: one standard TTL gate plus 100pF (Note 1) | | 400 | ns |
| $t_{CO}$ | Chip Select to Output ON Delay | | | 160 | ns |
| $t_{OH}$ | Previous Read Data Valid with Respect to Address Change | | 20 | | ns |
| $t_{DF}$ | Chip Select to Output OFF Delay | | | 120 | ns |
| $C_I$ | Input Capacitance | $T_A = 25°C$, f = 1MHz All pins at 0V | | 6.0 | pF |
| $C_O$ | Output Capacitance | | | 6.0 | pF |

Notes: 1. Timing reference levels – Inputs: High = 2.0V, Low = 1.0V. Outputs: High = 2.4V, Low = 0.8V

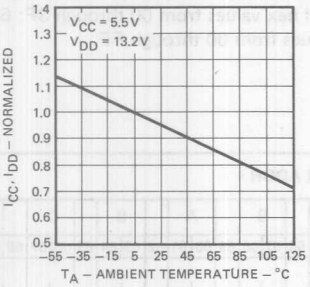
## SWITCHING WAVEFORMS



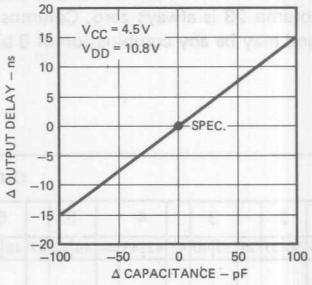

MOS-380

## TYPICAL CHARACTERISTICS

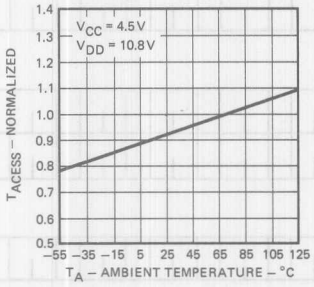
$I_{DD}$, $I_{CC}$ Versus Temperature (Normalized)



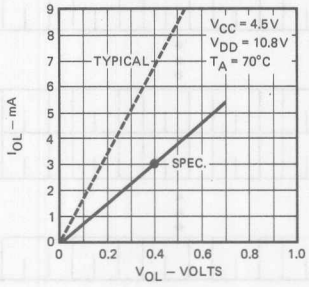

Δ Output Capacitance Versus Δ Output Delay



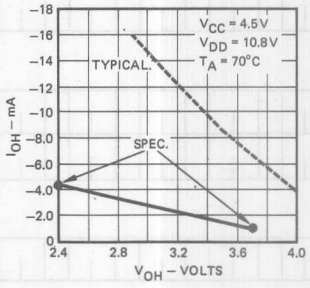

$T_{Access}$ Versus Temperature (Normalized)




$I_{OL}$ Versus $V_{OL}$




$I_{OH}$ Versus $V_{OH}$




MOS-381

4

## PROGRAMMING INSTRUCTIONS

### CUSTOM PATTERN ORDERING INFORMATION

The Am9208 is programmed from punched cards, card coding forms or from paper tape in card image form in the format as shown below.

Logic "1" = a more positive voltage (normally +5.0 V)
Logic "0" = a more negative voltage (normally 0V)

### FIRST CARD

| Column Number | Description |
|---|---|
| 10 thru 29 | Customer Name |
| 32 thru 37 | Total number of "1's" contained in the data. This is optional and should be left blank if not used. |
| 50 thru 62 | 9208B |
| 65 thru 72 | Data |

### SECOND CARD

| Column Number | Description |
|---|---|
| 31 | $CS_2$ input required to select chip (0 or 1) |
| 33 | $CS_1$ input required to select chip (0 or 1) |

Two options are provided for entering the data pattern with the remaining cards.

**OPTION 1** is the Binary Option where the address and data are presented in binary form on the basis of one word per card. With this option 1024 data cards are required.

| Column Number | |
|---|---|
| 10, 12, 14, 16, 18 20, 22, 24, 26, 28 | Address input pattern with the most significant bit ($A_9$) in column 10 and the least significant bit ($A_0$) in column 28. |
| 40, 42, 44, 46, 48, 50, 52, 54 | Output pattern with the most significant bit ($O_8$) in column 40 and the least significant bit ($O_1$) in column 54. |
| 73 thru 80 | Coding these columns is not essential and may be used for card identification purposes. |

**OPTION 2** is the Hexadecimal Option and is a much more compact way of presenting the data. This format requires only 64 data cards. Each data card contains the 8-bit output information for 16 storage locations in the memory. The address indicated in columns 21, 22 and 23 is the address of the data presented in columns 30 and 31. Addresses for successive data are assumed to be in incremental ascending order from the initial address. Since the address in columns 21, 22 and 23 always points only to the first data on the card, column 23 is always zero. Columns 21 and 22 take all hex values from 00 through 3F: 64 cards in all. Data is entered in hex values and may be any combination of 8 bits, that is, hex values from 00 through FF.

| ADDR | OUTPUT VALUES FOR ADDR + | | |

# Am9214/Am3514

## 512 x 8 Read Only Memory

### DISTINCTIVE CHARACTERISTICS

- Single 5-volt power supply
  Tolerances: ±5% commercial, ±10% military
- 512 x 8 organization
- Fully static operation — no clocks
- 4 programmable chip selects
- High-speed — 500ns access
- Three-state output buffers
- Low power dissipation — 263mW max.
- Logic voltage levels identical to TTL
- High noise immunity — full 400mV
- N-Channel silicon gate MOS technology
- Military and commercial temperature ranges available
- 100% MIL-STD-883 reliability assurance testing
- Directly plug-in compatible with FSC 3514, MOSTEK 2600

### FUNCTIONAL DESCRIPTION

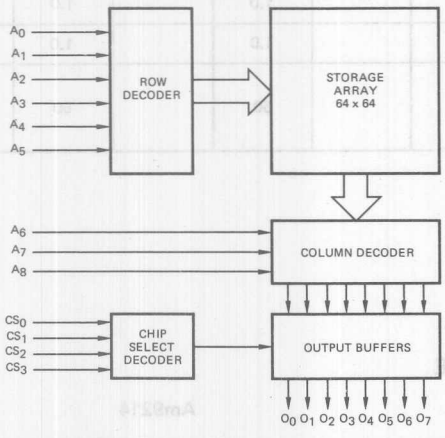
The Am9214/Am3514 devices are high performance, 4096-bit, static, read only memories. Each memory is implemented as 512 words by 8 bits per word. This organization simplifies the design of small memory systems and permits incremental memory sizes as small as 512 words.

Four Chip Select input signals are logically ANDed together to provide control of the output buffers. Each Chip Select polarity may be specified by the customer thus allowing the addressing of up to 16 memories without external gating. The outputs of unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9214 devices and other three-state components.

These memories are fully static and require no clock signals of any kind. A selected chip will output data from a location specified by whatever address is present on the address input lines. Input and output voltage levels are identical to TTL specifications, providing simplified interfacing and standard worst-case noise immunity of 400mV. Only a single supply of +5 volts is required for power.

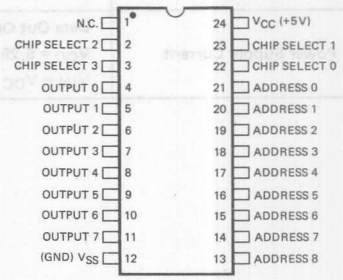
4

### BLOCK DIAGRAM




MOS-382

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

MOS-383

### ORDERING INFORMATION

| Package Type | Ambient Temperature Specification | Access Time | | |
|---|---|---|---|---|
| | | 1000ns | 700ns | 500ns |
| Hermetic DIP | 0°C ≤ $T_A$ ≤ +70°C | AM35142CC | AM35141CC | AM9214CC |
| | | AM35142DC | AM35141DC | AM9214DC |
| | −55°C ≤ $T_A$ ≤ +125°C | | | AM9214CM |
| | | | | AM9214DM |

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential (Pin 10 to Pin 9) Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs | −0.5V to +7.0V |
| DC Input Voltage | −0.5V to +7.0V |
| Power Dissipation | 1.0W |

The products described by this specification include internal circuitry designed to protect input devices from excessive accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to any voltages that exceed the maximum ratings.

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Am9214DC
Am35141DC
Am35142DC

$T_A = 0°C$ to $+70°C$
$V_{CC} = +5V \pm 5\%$

| Parameters | Description | Test Conditions | Am9214 Min. | Am9214 Max. | Am3514 Min. | Am3514 Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC} = 4.75V$, $I_{OH} = 500\mu A$ | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC} = 4.75V$, $I_{OL} = 2.4mA$ | | 0.4 | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | $V_{CC}$ | $V_{CC}-2.75$ | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Voltage | (See Note 1) | −0.5 | 0.8 | −0.5 | 0.55 | Volts |
| $I_{LI}$ | Input Load Current | $V_{CC} = 5.25V$, $0V \leq V_{IN} \leq 5.25V$ | | 1.0 | | 1.0 | μA |
| $I_{LO}$ | Output Leakage Current | Output OFF, $V_{OUT} = 0.4$ to $V_{CC}$ | | 1.0 | | 1.0 | μA |
| $I_{CC}$ | Power Supply Current | Data Out Open<br>$V_{CC} = 5.25V$<br>$V_{IN} = V_{CC}$ | | 50 | | 50 | mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Am9214DM $T_A = -55°C$ to $+125°C$ $V_{CC} = +5V \pm 10\%$

| Parameters | Description | Test Conditions | Am9214 Min. | Am9214 Max. | Units |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC} = 4.5V$, $I_{OH} = 500\mu A$ | 2.2 | $V_{CC}$ | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC} = 4.5V$, $I_{OL} = 2.4mA$ | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Voltage | (See Note 1) | −0.5 | 0.8 | Volts |
| $I_{LI}$ | Input Load Current | $V_{CC} = 5.5V$, $0V \leq V_{IN} \leq 5.5V$ | | 10 | μA |
| $I_{LO}$ | Output Leakage Current | Output OFF, $V_{OUT} = 0.4$ to $V_{CC}$ | | 10 | μA |
| $I_{CC}$ | Power Supply Current | Data Out Open<br>$V_{CC} = 5.5V$<br>$V_{IN} = V_{CC}$ | | 70 | mA |

Notes: 1. Input Logic levels that swing more negative than −0.5 volts will be subject to clamping currents attempting to keep the input from falling.

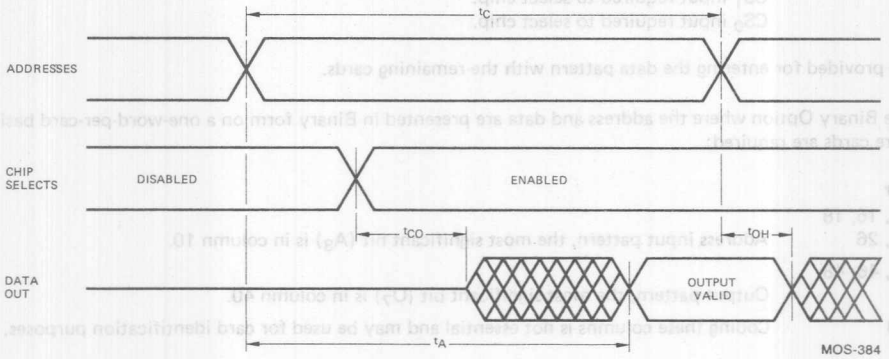
## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Output Load: 1.5 TTL Gate +100pF for Am9214, 1.5 TTL Gate only for Am3514
Transition Times: 10ns
Input Levels: 0.8V and 2.0V
Output Reference: 1.5V

| Parameter | Description | Test Conditions | Am9214 Min. | Am9214 Max. | Am35141 Min. | Am35141 Max. | Am35142 Min. | Am35142 Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_C$ | Cycle Time | | 500 | | | | | | ns |
| $t_A$ | Access Time | | | 500 | | 700 | | 1000 | ns |
| $t_{CO}$ | Chip Select to Output On Delay | | | 200 | | 500 | | 900 | ns |
| $t_{OH}$ | Previous Read Data Valid with Respect to Address Change | | 50 | | | | | | ns |
| $C_I$ | Input Capacitance | | | 6.0 | | 8.0 | | 8.0 | pF |
| $C_O$ | Output Capacitance | | | 10 | | 12 | | 12 | pF |

4

## TIMING DIAGRAM




### GLOSSARY OF TERMS

**Cycle Time** – Specifies the maximum rate at which new read operations may be initiated, and thus the minimum time between successive address changes.

**Access Time** – Maximum delay from the arrival of the last stable address line to valid output data on a selected chip.

**Output Enable Time ($t_{CO}$)** – Maximum delay from the arrival of four active Chip Select signals to enabled output data. Unselected chips will have high impedance outputs. Active level definition for each of the four chip Select inputs may be either high or low and is programmed along with the data pattern.

**Output Hold Time ($t_{OH}$)** – Minimum delay which will elapse between a change of the input address and any consequent change in the output data.

shown below.

Logic "1" = a more positive voltage (normally +5.0V)
Logic "0" = a more negative voltage (normally 0V)

**FIRST CARD**

| Column Number | Description |
|---|---|
| 10 thru 29 | Customer Name |
| 32 thru 37 | Total number of "1's" contained in the data. This is optional and should be left blank if not used. |
| 50 thru 62 | 9214 or 35141 or 35142 |
| 65 thru 72 | Date |

**SECOND CARD**

| Column Number | Description |
|---|---|
| 29 | $CS_3$ input required (0 or 1) to select chip. |
| 31 | $CS_2$ input required to select chip. |
| 33 | $CS_1$ input required to select chip. |
| 35 | $CS_0$ input required to select chip. |

Two options are provided for entering the data pattern with the remaining cards.

**OPTION 1** is the Binary Option where the address and data are presented in Binary form on a one-word-per-card basis. With this option, 512 more cards are required:

| Column Number | |
|---|---|
| 10, 12, 14, 16, 18<br>20, 22, 24, 26 | Address input pattern, the most significant bit ($A_8$) is in column 10. |
| 40, 42, 44, 46, 48,<br>50, 52, 54 | Output pattern, the most significant bit ($O_7$) is in column 40. |
| 73 thru 80 | Coding these columns is not essential and may be used for card identification purposes. |

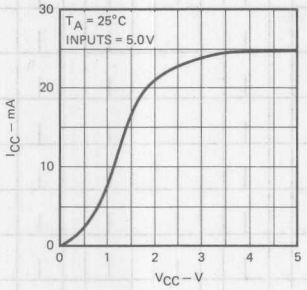
**OPTION 2** is the Hexadecimal Option and is a much more compact way of presenting the data. This format requires only 32 data cards (see chart).

Each data card contains the 8-bit output information for 16 storage locations in the memory. The address indicated in columns 21, 22 and 23 is the address of the data presented in columns 30 and 31. Addresses for successive data are assumed to be in incremental ascending order from the initial address. Since the address in columns 21, 22 and 23 always points only to the first data on the card, column 23 is always zero. Columns 21 and 22 take all hex values from 00 through 1F: 32 cards in all. Data is also entered in hex values and may be any combination of 8 bits, that is, hex value from 00 through FF.

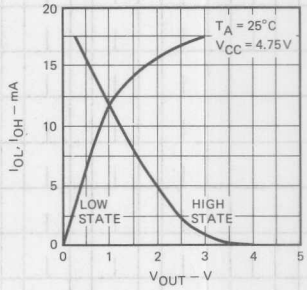
| ADDR | OUTPUT VALUES FOR ADDR + | | |

## Am9214 PERFORMANCE CURVES

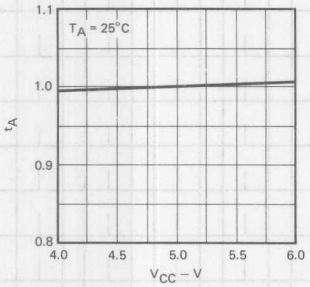
### Typical Power Supply Current Versus Voltage



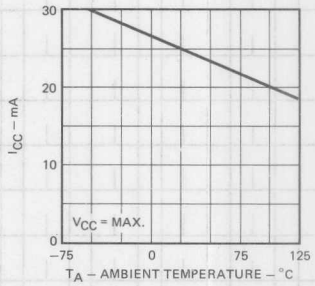

### Typical Output Current Versus Voltage




### Access Time Versus $V_{CC}$ Normalized to $V_{CC}$ at 5.0 V




### Typical Power Supply Current Versus Ambient Temperature




MOS-385

# Am9216

## 2048 x 8 Read Only Memory



### DISTINCTIVE CHARACTERISTICS

- 2048 x 8 organization
- High speed — 300ns access time
- Fully capacitive inputs — simplified driving
- 2 fully programmable chip selects — increased flexibility
- Logic voltage levels compatible with TTL
- Three-state output buffers — simplified expansion
- Standard supply voltages — +12V, +5.0V
- No $V_{BB}$ supply required
- N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

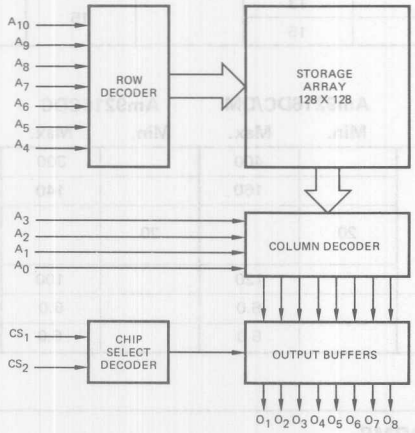
### FUNCTIONAL DESCRIPTION

The Am9216 devices are high performance, 16384-bit, static, mask programmed, read only memories. Each memory is implemented as 2048 words by 8 bits per word. This organization simplifies the design of small memory systems and permits incremental memory sizes as small as 2048 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

Two Chip Select input signals are logically ANDed together to provide control of the output buffers. Each Chip Select polarity may be specified by the customer thus allowing the addressing of 4 memory chips without external gating. The outputs of unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9216 devices and other three-state components.

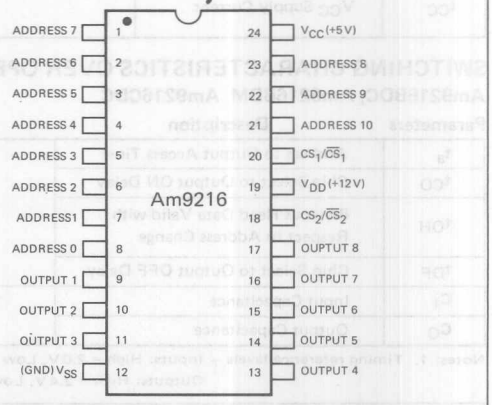
These memories are fully static and require no clock signals of any kind. A selected chip will output data from a location specified by whatever address is present on the address input lines. The Am9216 is pin compatible with the Am9208 which is an 8k-bit mask programmed ROM. Input and output voltage levels are compatible with TTL specifications.

### BLOCK DIAGRAM




### CONNECTION DIAGRAM

Top View




Note: Pin 1 is marked for orientation.

### ORDERING INFORMATION

| Package Type | Ambient Temperature Specifications | Access Time | |
|---|---|---|---|
| | | 400ns | 300ns |
| Hermetic DIP | $0°C \leq T_A \leq 70°C$ | AM9216BDC | AM9216CDC |
| | $-55°C \leq T_A \leq +125°C$ | AM9216BDM | |

| | |
|---|---|
| $V_{DD}$ with Respect to $V_{SS}$ | 15V |
| $V_{CC}$ with Respect to $V_{SS}$ | +7.0V |
| DC Voltage Applied to Outputs | −0.5V to +7.0V |
| DC Input Voltage | −0.5V to +7.0V |
| Power Dissipation | 1.0W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGE

| Part Number | Ambient Temperature | $V_{DD}$ | $V_{CC}$ | $V_{SS}$ |
|---|---|---|---|---|
| Am9216DC | $0°C \leq T_A \leq +70°C$ | +12V ± 5% | +5.0V ± 5% | 0V |
| Am9216DM | $-55°C \leq T_A \leq +125°C$ | +12V ± 10% | +5.0V ± 10% | 0V |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

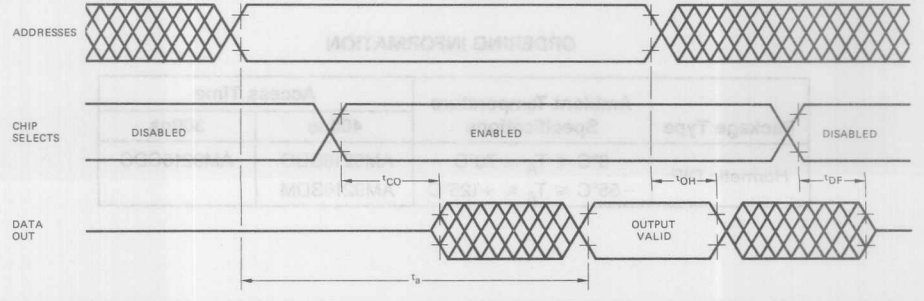
| Parameters | Description | Test Conditions | | Am9216DC Min. | Am9216DC Max. | Am9216DM Min. | Am9216DM Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -1.0mA$ | | 3.7 | | 3.7 | | Volts |
| | | $I_{OH} = -4.0mA$ | | 2.4 | | 2.4 | | |
| $V_{OL}$ | Output LOW Voltage | $I_{OL} = 3.2mA$ | | | 0.4 | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | | 2.4 | $V_{CC}+1.0$ | 2.6 | $V_{CC}+1.0$ | Volts |
| $V_{IL}$ | Input LOW Voltage | | | −0.5 | 0.8 | −0.5 | 0.8 | Volts |
| $I_{LO}$ | Output Leakage Current | Chip disabled | | | 10 | | 10 | μA |
| $I_{LI}$ | Input Leakage Current | | | | 10 | | 10 | μA |
| $I_{DD}$ | $V_{DD}$ Supply Current | Selected | Am9216B | | 42 | | 47 | mA |
| | | | Am9216C | | 49 | | | |
| | | Deselected | Am9216B | | 52 | | 57 | |
| | | | Am9216C | | 60 | | | |
| $I_{CC}$ | $V_{CC}$ Supply Current | | Am9216B | | 13 | | 15 | mA |
| | | | Am9216C | | 15 | | | |

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions | Am9216BDC, Am9216BDM, Am9216CDC Min. | Am9216BDC, Am9216BDM, Am9216CDC Max. | Am9216CDC Min. | Am9216CDC Max. | Units |
|---|---|---|---|---|---|---|---|
| $t_a$ | Address to Output Access Time | $t_r = t_f = 20ns$ Output load: one standard TTL gate plus 100pF (Note 1) | | 400 | | 300 | ns |
| $t_{CO}$ | Chip Select to Output ON Delay | | | 160 | | 140 | ns |
| $t_{OH}$ | Previous Read Data Valid with Respect to Address Change | | 20 | | 20 | | ns |
| $t_{DF}$ | Chip Select to Output OFF Delay | | | 120 | | 100 | ns |
| $C_I$ | Input Capacitance | $T_A = 25°C$, f = 1.0MHz All pins at 0V | | 6.0 | | 6.0 | pF |
| $C_O$ | Output Capacitance | | | 6.0 | | 6.0 | pF |

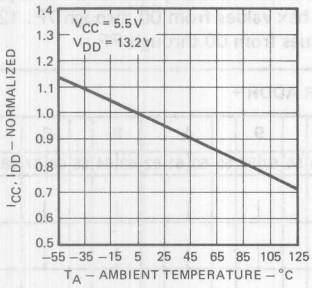
Notes: 1. Timing reference levels — Inputs: High = 2.0V, Low = 1.0V.
Outputs: High = 2.4V, Low = 0.8V.

### SWITCHING WAVEFORMS

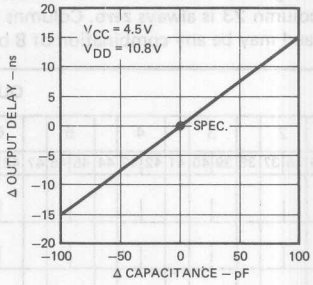


## TYPICAL CHARACTERISTICS

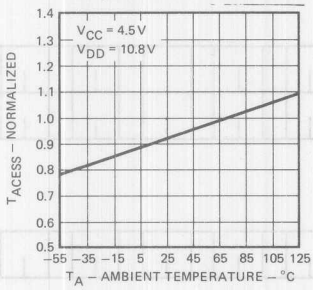
**$I_{DD}$, $I_{CC}$ Versus Temperature (Normalized)**



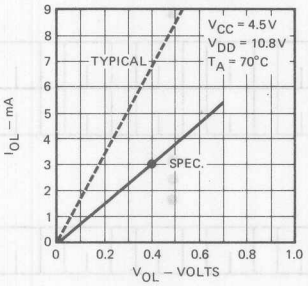

**Δ Output Capacitance Versus Δ Output Delay**



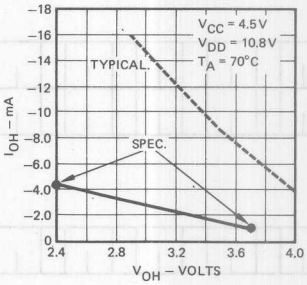

**$T_{Access}$ Versus Temperature (Normalized)**




**$I_{OL}$ Versus $V_{OL}$**




**$I_{OH}$ Versus $V_{OH}$**




4

## PROGRAMMING INSTRUCTIONS

### CUSTOM PATTERN ORDERING INFORMATION

The Am9216 is programmed from punched cards, card coding forms or from paper tape in card image form in the format as shown below.

Logic "1" = a more positive voltage (normally +5.0 V)
Logic "0" = a more negative voltage (normally 0V)

### FIRST CARD

| Column Number | Description |
|---|---|
| 10 thru 29 | Customer Name |
| 32 thru 37 | Total number of "1's" contained in the data. This is optional and should be left blank if not used. |
| 50 thru 62 | 9216B or 9216C |
| 65 thru 72 | Data |

### SECOND CARD

| Column Number | Description |
|---|---|
| 31 | $CS_2$ input required to select chip (0 or 1) |
| 33 | $CS_1$ input required to select chip (0 or 1) |

Two options are provided for entering the data pattern with the remaining cards.

**OPTION 1** is the Binary Option where the address and data are presented in binary form on the basis of one word per card. With this option 2048 data cards are required.

| Column Number | |
|---|---|
| 10, 12, 14, 16, 18<br>20, 22, 24, 26, 28, 30 | Address input pattern with the most significant bit ($A_{10}$) in column 10 and the least significant bit ($A_0$) in column 30. |
| 40, 42, 44, 46, 48,<br>50, 52, 54 | Output pattern with the most significant bit ($O_8$) in column 40 and the least significant bit ($O_1$) in column 54. |
| 73 thru 80 | Coding these columns is not essential and may be used for card identification purposes. |

**OPTION 2** is the Hexadecimal Option and is a much more compact way of presenting the data. This format requires only 128 data cards. Each data card contains the 8-bit output information for 16 storage locations in the memory. The address indicated in columns 21, 22 and 23 is the address of the data presented in columns 30 and 31. Addresses for successive data are assumed to be in incremental ascending order from the initial address. Since the address in columns 21, 22 and 23 always points only to the first data on the card, column 23 is always zero. Columns 21 and 22 take all hex values from 00 through 7F: 128 cards in all. Data is entered in hex values and may be any combination of 8 bits, that is, hex values from 00 through FF.

| ADDR | OUTPUT VALUES FOR ADDR + | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| 21 22 23 | 30 31 32 | 33 34 35 | 36 37 38 | 39 40 41 | 42 43 44 | 45 46 47 | 48 49 50 | 51 52 53 | 54 55 56 | 57 58 59 | 60 61 62 | 63 64 65 | 66 67 68 | 69 70 71 | 72 73 74 | 75 76 |
| 0 0 0 | | | | | | | | | | | | | | | | |
| 0 1 0 | | | | | | | | | | | | | | | | |
| 0 2 0 | | | | | | | | | | | | | | | | |
| ⋮ | | | | | | | | | | | | | | | | |
| 1 F 0 | | | | | | | | | | | | | | | | |
| 2 0 0 | | | | | | | | | | | | | | | | |
| ⋮ | | | | | | | | | | | | | | | | |
| 3 F 0 | | | | | | | | | | | | | | | | |
| ⋮ | | | | | | | | | | | | | | | | |
| 7 F 0 | | | | | | | | | | | | | | | | |

# Am9217/8316A

## 2048 x 8 Read Only Memory



### DISTINCTIVE CHARACTERISTICS

- 2048 x 8 organization
- Plug-in replacement for 8316A
- Access times as fast as 450 ns
- Fully capacitive inputs — simplified driving
- 3 fully programmable Chip Selects — increased flexibility
- Logic voltage levels compatible with TTL
- Three-state output buffers — simplified expansion
- Drives two full TTL loads
- Single supply voltage — +5.0V
- Low power dissipation
- N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

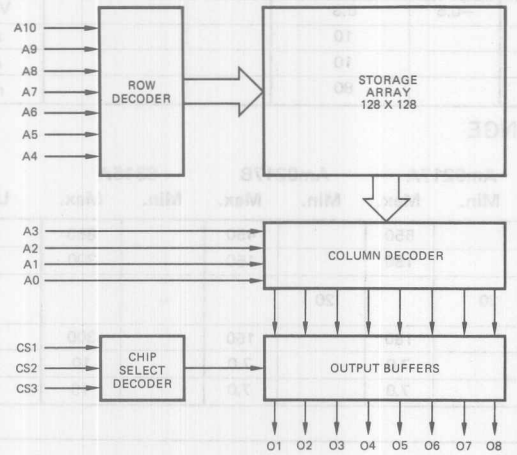
### FUNCTIONAL DESCRIPTION

The Am9217 devices are high performance, 16384-bit, static, mask programmed, read only memories. Each memory is implemented as 2048 words by 8 bits per word. This organization simplifies the design of small memory systems and permits incremental memory sizes as small as 2048 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

Three programmable Chip Select input signals are provided to control the output buffers. Each Chip Select polarity may be specified by the customer thus allowing the addressing of 8 memory chips without external gating. The outputs of unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9217 devices and other three-state components.

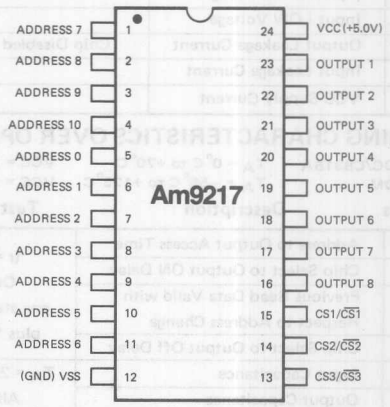
These memories are fully static and require no clock signals of any kind. A selected chip will output data from a location specified by whatever address is present on the address input lines. Input and output voltage levels are compatible with TTL specifications.

### BLOCK DIAGRAM




MOS-386

### CONNECTION DIAGRAM




Top View
Pin 1 is marked for orientation.

MOS-387

### ORDERING INFORMATION

| Package Type | Ambient Temperature Specifications | Access Time | |
|---|---|---|---|
| | | 550ns | 450ns |
| Hermetic DIP | $0°C \leq T_A \leq +70°C$ | AM9217ADC/C8316A | AM9217BDC |
| | | AM9217ACC | AM9217BCC |
| | $-55°C \leq T_A \leq +125°C$ | AM9217ADM | AM9217BDM |
| Plastic DIP | $0°C \leq T_A \leq +70°C$ | AM9217APC/P8316A | AM9217BPC |

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| VCC with Respect to VSS | +7.0V |
| DC Voltage Applied to Outputs | −0.5V to +7.0V |
| DC Input Voltage | −0.5V to +7.0V |
| Power Dissipation | 1.0W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## ELECTRICAL CHARACTERISTICS

Am9217ADC, Am9217BDC, C8316A: $T_A$ = 0°C to +70°C, VCC = 5.0V ± 5%

| Parameters | Description | Test Conditions | | Am9217XDC Min. | Am9217XDC Max. | C8316A Min. | C8316A Max. | Units |
|---|---|---|---|---|---|---|---|---|
| VOH | Output HIGH Voltage | 9217 | IOH = −200μA | 2.4 | | | | Volts |
| | | 8316A | IOH = −100μA | | | 2.2 | | |
| VOL | Output LOW Voltage | 9217 | $I_{OL}$ = 3.2mA | | 0.4 | | | Volts |
| | | 8316A | IOL = 2.0mA | | | | 0.45 | |
| VIH | Input HIGH Voltage | | | 2.0 | VCC + 1.0 | 2.0 | VCC + 1.0 | Volts |
| VIL | Input LOW Voltage | | | −0.5 | 0.8 | −0.5 | 0.8 | Volts |
| ILO | Output Leakage Current | Chip Disabled | | | 10 | | 10 | μA |
| ILI | Input Leakage Current | | | | 10 | | 10 | μA |
| ICC | VCC Supply Current | | | | 70 | | 98 | mA |

## ELECTRICAL CHARACTERISTICS

Am9217ADM, Am9217BDM: $T_A$ = −55°C to +125°C, VCC = 5.0V ± 10%

| Parameters | Description | Test Conditions | | Am9217XDM Min. | Am9217XDM Max. | Min. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| VOH | Output HIGH Voltage | 9217 | IOH = −200μA | 2.2 | | | | Volts |
| VOL | Output LOW Voltage | 9217 | IOL = 3.2mA | | 0.45 | | | Volts |
| VIH | Input HIGH Voltage | | | 2.0 | VCC + 1.0 | | | Volts |
| VIL | Input LOW Voltage | | | −0.5 | 0.8 | | | Volts |
| ILO | Output Leakage Current | Chip Disabled | | | 10 | | | μA |
| ILI | Input Leakage Current | | | | 10 | | | μA |
| ICC | VCC Supply Current | | | | 80 | | | mA |

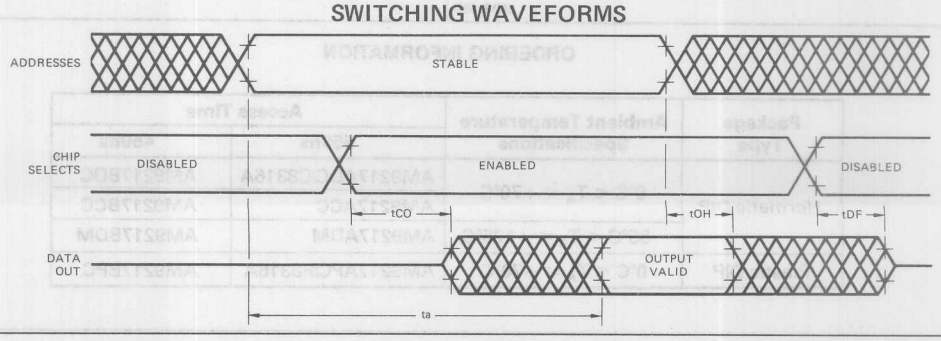
## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Am9217XDC/C8316A: $T_A$ = 0°C to +70°C, VCC = 5.0V ± 5%
Am9217XDM: $T_A$ = −55°C to +125°C, VCC = 5.0V ± 10%

| Parameters | Description | Test Conditions | Am9217A Min. | Am9217A Max. | Am9217B Min. | Am9217B Max. | 8316A Min. | 8316A Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| ta | Address to Output Access Time | tr = tf = 20ns; Output load: one standard TTL gate plus 100pF (Note 1) | | 550 | | 450 | | 850 | ns |
| tCO | Chip Select to Output ON Delay | | | 180 | | 150 | | 300 | ns |
| tOH | Previous Read Data Valid with Respect to Address Change | | 20 | | 20 | | – | | ns |
| tDF | Chip Select to Output Off Delay | | | 180 | | 150 | | 300 | ns |
| CI | Input Capacitance | $T_A$ = 25°C, f = 1.0MHz; All pins at 0V | | 7.0 | | 7.0 | | 10 | pF |
| CO | Output Capacitance | | | 7.0 | | 7.0 | | 15 | pF |

Notes: 1. Timing reference levels: High = 2.0V, Low = 0.8V.

### SWITCHING WAVEFORMS




MOS-388

## PROGRAMMING INSTRUCTIONS

### CUSTOM PATTERN ORDERING INFORMATION

The Am9217 is programmed from punched cards, card coding forms or paper tape in card image format as shown below.

Logic "1" = a more positive voltage (normally +5.0 V)
Logic "0" = a more negative voltage (normally 0 V)

### FIRST CARD

| Column Number | Description |
|---|---|
| 10 thru 29 | Customer Name |
| 32 thru 37 | Total number of "1's" contained in the data. This is optional and should be left blank if not used. |
| 50 thru 62 | 8316A or 9217 |
| 65 thru 72 | Optional information |

### SECOND CARD

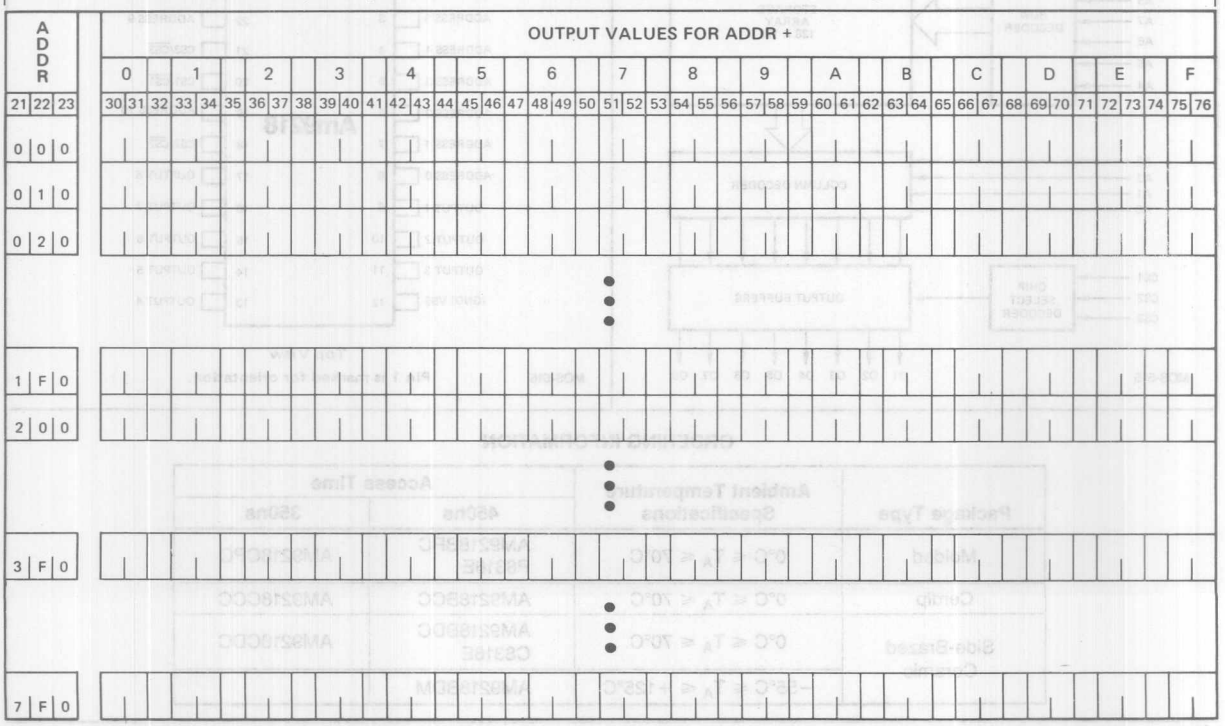
| Column Number | Description |
|---|---|
| 29 | CS3 input required to select chip (0 or 1) |
| 31 | CS2 input required to select chip (0 or 1) |
| 33 | CS1 input required to select chip (0 or 1) |

Two options are provided for entering the data pattern with the remaining cards.

**OPTION 1** is the Binary Option where the address and data are presented in binary form on the basis of one word per card. With this option 2048 data cards are required.

| Column Number | |
|---|---|
| 10, 12, 14, 16, 18 20, 22, 24, 26, 28, 30 | Address input pattern with the most significant bit (A10) in column 10 and the least significant bit (A0) in column 30. |
| 40, 42, 44, 46, 48, 50, 52, 54 | Output pattern with the most significant bit (O8) in column 40 and the least significant bit (O1) in column 54. |
| 73 thru 80 | Coding these columns is not essential and may be used for card identification purposes. |

**OPTION 2** is the Hexadecimal Option and is a much more compact way of presenting the data. This format requires only 128 data cards. Each data card contains the 8-bit output information for 16 storage locations in the memory. The address indicated in columns 21, 22 and 23 is the address of the data presented in columns 30 and 31. Addresses for successive data are assumed to be in incremental ascending order from the initial address. Since the address in columns 21, 22 and 23 always points only to the first data on the card, column 23 is always zero. Columns 21 and 22 take all hex values from 00 through 7F: 128 cards in all. Data is entered in hex values and may be any combination of 8 bits, that is, hex values from 00 through FF.



# Am9218/8316E

## 2048 x 8 Read Only Memory

### DISTINCTIVE CHARACTERISTICS

- 2048 x 8 organization
- Plug-in replacement for 8316E
- Access times as fast as 350 ns
- Fully capacitive inputs — simplified driving
- 3 fully programmable Chip Selects — increased flexibility
- Logic voltage levels compatible with TTL
- Three-state output buffers — simplified expansion
- Drives two full TTL loads
- Single supply voltage — +5.0V
- Low power dissipation
- N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

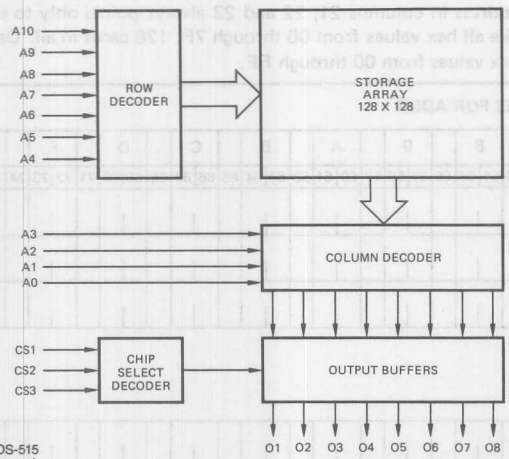
### FUNCTIONAL DESCRIPTION

The Am9218 devices are high performance, 16384-bit, static, mask programmed, read only memories. Each memory is implemented as 2048 words by 8 bits per word. This organization simplifies the design of small memory systems and permits incremental memory sizes as small as 2048 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

Three programmable Chip Select input signals are provided to control the output buffers. Each Chip Select polarity may be specified by the customer thus allowing the addressing of 8 memory chips without external gating. The outputs of unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9218 devices and other three-state components.

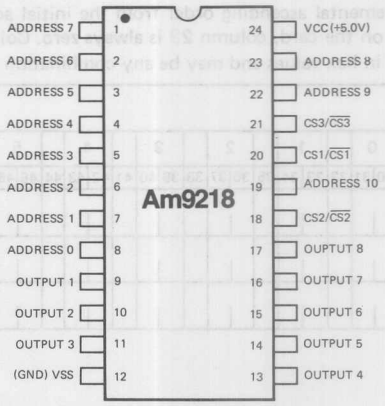
These memories are fully static and require no clock signals of any kind. A selected chip will output data from a location specified by whatever address is present on the address input lines. Input and output voltage levels are compatible with TTL specifications.

### BLOCK DIAGRAM




MOS-515

### CONNECTION DIAGRAM




Top View

MOS-516

Pin 1 is marked for orientation.

### ORDERING INFORMATION

| Package Type | Ambient Temperature Specifications | Access Time | |
|---|---|---|---|
| | | 450ns | 350ns |
| Molded | $0°C \leq T_A \leq 70°C$ | AM9218BPC<br>P8316E | AM9218CPC |
| Cerdip | $0°C \leq T_A \leq 70°C$ | AM9218BCC | AM9218CCC |
| Side-Brazed Ceramic | $0°C \leq T_A \leq 70°C$ | AM9218BDC<br>C8316E | AM9218CDC |
| | $-55°C \leq T_A \leq +125°C$ | AM9218BDM | |

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| VCC with Respect to VSS | +7.0V |
| DC Voltage Applied to Outputs | −0.5V to +7.0V |
| DC Input Voltage | −0.5V to +7.0V |
| Power Dissipation | 1.0W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## ELECTRICAL CHARACTERISTICS

Am9218BDC, Am9218CDC, C8316A: $T_A = 0°C$ to $+70°C$, VCC = 5.0V ±5%

| Parameters | Description | Test Conditions | | Am9218XDC Min. | Am9218XDC Max. | C8316E Min. | C8316E Max. | Units |
|---|---|---|---|---|---|---|---|---|
| VOH | Output HIGH Voltage | 9218 | IOH = −200μA | 2.4 | | | | Volts |
| | | 8316E | IOH = −100μA | | | 2.4 | | |
| VOL | Output LOW Voltage | 9218 | IOL = 3.2mA | | 0.4 | | | Volts |
| | | 8316E | IOL = 2.1mA | | | | 0.4 | |
| VIH | Input HIGH Voltage | | | 2.0 | VCC + 1.0 | 2.0 | VCC + 1.0 | Volts |
| VIL | Input LOW Voltage | | | −0.5 | 0.8 | −0.5 | 0.8 | Volts |
| ILO | Output Leakage Current | Chip Disabled | | | 10 | | 10 | μA |
| ILI | Input Leakage Current | | | | 10 | | 10 | μA |
| ICC | VCC Supply Current | | | | 70 | | 95 | mA |

## ELECTRICAL CHARACTERISTICS

Am9218BDM: $T_A = -55°C$ to $+125°C$, VCC = 5.0V ±10%

| Parameters | Description | Test Conditions | Am9218B Min. | Am9218B Max. | Units |
|---|---|---|---|---|---|
| VOH | Output HIGH Voltage | IOH = −200μA | 2.2 | | Volts |
| VOL | Output LOW Voltage | IOL = 3.2mA | | 0.45 | Volts |
| VIH | Input HIGH Voltage | | 2.0 | VCC + 1.0 | Volts |
| VIL | Input LOW Voltage | | −0.5 | 0.8 | Volts |
| ILO | Output Leakage Current | Chip Disabled | | 10 | μA |
| ILI | Input Leakage Current | | | 10 | μA |
| ICC | VCC Supply Current | | | 80 | mA |

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

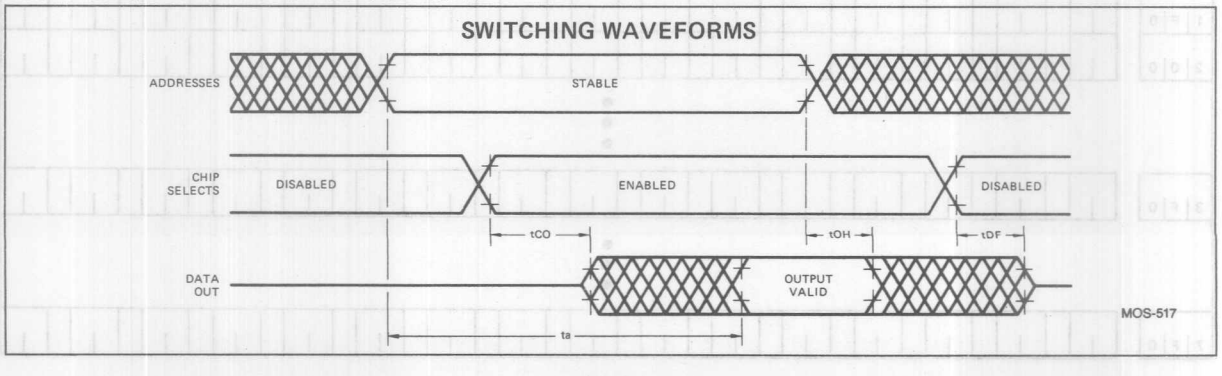
Am9218XDC/C8316E: $T_A = 0°C$ to $+70°C$, VCC = 5.0V ± 5%

Am9218BDM: $T_A = -55°C$ to $+125°C$, VCC = 5.0V ± 10%

| Parameters | Description | Test Conditions | Am9218B Min. | Am9218B Max. | Am9218C Min. | Am9218C Max. | 8316E Min. | 8316E Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| ta | Address to Output Access Time | tr = tf = 20ns, Output Load: one standard TTL gate plus 100pF (Note 1) | | 450 | | 350 | | 450 | ns |
| tCO | Chip Select to Output ON Delay | | | 150 | | 130 | | 250 | ns |
| tOH | Previous Read Data Valid with Respect to Address Change | | 20 | | 20 | | – | | ns |
| tDF | Chip Select to Output OFF Delay | | | 150 | | 130 | | 250 | ns |
| CI | Input Capacitance | $T_A = 25°C$, f = 1.0MHz, All pins at 0V | | 7.0 | | 7.0 | | 7.0 | pF |
| CO | Output Capacitance | | | 7.0 | | 7.0 | | 7.0 | pF |

Notes: 1. Timing reference levels: High = 2.0V, Low = 0.8V.

### SWITCHING WAVEFORMS



## PROGRAMMING INSTRUCTIONS

### CUSTOM PATTERN ORDERING INFORMATION

The Am9218 is programmed from punched cards, card coding forms or paper tape in card image format as shown below.

Logic "1" = a more positive voltage (normally +5.0 V)
Logic "0" = a more negative voltage (normally 0 V)

**FIRST CARD**

| Column Number | Description |
|---|---|
| 10 thru 29 | Customer Name |
| 32 thru 37 | Total number of "1's" contained in the data. This is optional and should be left blank if not used. |
| 50 thru 62 | 8316E or 9218 |
| 65 thru 72 | Optional information |

**SECOND CARD**

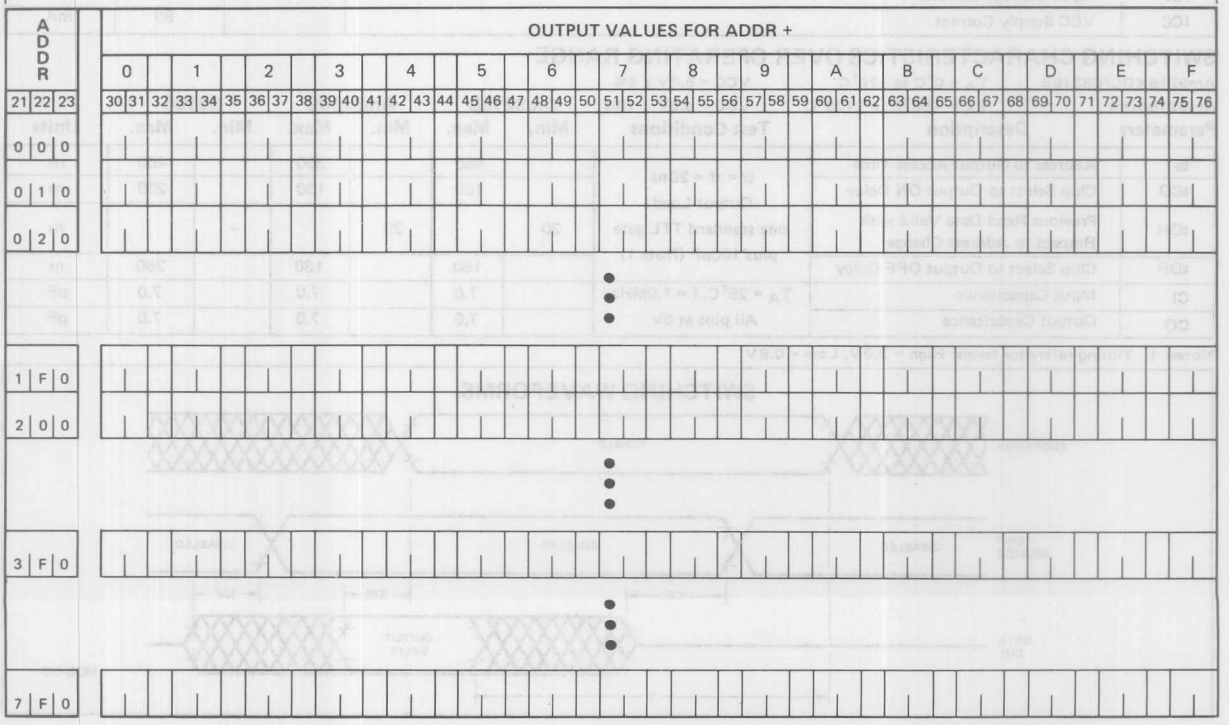
| Column Number | Description |
|---|---|
| 29 | CS3 input required to select chip (0 or 1) |
| 31 | CS2 input required to select chip (0 or 1) |
| 33 | CS1 input required to select chip (0 or 1) |

Two options are provided for entering the data pattern with the remaining cards.

**OPTION 1** is the Binary Option where the address and data are presented in binary form on the basis of one word per card. With this option 2048 data cards are required.

| Column Number | |
|---|---|
| 10, 12, 14, 16, 18<br>20, 22, 24, 26, 28, 30 | Address input pattern with the most significant bit (A10) in column 10 and the least significant bit (A0) in column 30. |
| 40, 42, 44, 46, 48,<br>50, 52, 54 | Output pattern with the most significant bit (O8) in column 40 and the least significant bit (O1) in column 54. |
| 73 thru 80 | Coding these columns is not essential and may be used for card identification purposes. |

**OPTION 2** is the Hexadecimal Option and is a much more compact way of presenting the data. This format requires only 128 data cards. Each data card contains the 8-bit output information for 16 storage locations in the memory. The address indicated in columns 21, 22 and 23 is the address of the data presented in columns 30 and 31. Addresses for successive data are assumed to be in incremental ascending order from the initial address. Since the address in columns 21, 22 and 23 always points only to the first data on the card, column 23 is always zero. Columns 21 and 22 take all hex values from 00 through 7F: 128 cards in all. Data is entered in hex values and may be any combination of 8 bits, that is, hex values from 00 through FF.



# Am9232 • Am9233

## 4096 X 8 Read Only Memory

**PRELIMINARY DATA**

### DISTINCTIVE CHARACTERISTICS

- 4096 X 8 organization
- No clocks or refresh required
- Access time selected to 300ns
- Fully capacitive inputs – simplified driving
- 2 mask programmable chip selects – increased flexibility
- Logic voltage levels compatible with TTL
- Three state output buffers – simplified expansion
- Drives two TTL loads
- Single +5 volt power supply
- Two different pinouts for universal application
- Low power dissipation
- 100% MIL-STD-883 reliability assurance testing
- Non-connect option on chip selects.

### FUNCTIONAL DESCRIPTION

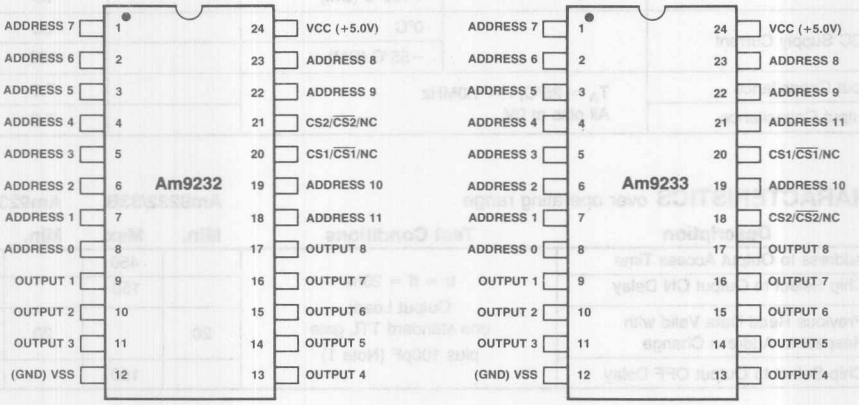
The Am9232/33 devices are high performance, 32,768-bit, static, mask programmed, read only memories. Each memory is implemented as 4096 words by 8 bits per word. This organization simplifies the design of small memory systems and permits incremental memory sizes of 4096 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

Two programmable Chip Select input signals are provided to control the output buffers. Each Chip Select polarity may be specified by the customer thus allowing the addressing of 4 memory chips without external gating. The outputs of unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9232/33 devices and other three-state components.

These memories are fully static and require no clock signals of any kind. A selected chip will output data from a location specified by the address present on the address input lines. Input and output voltage levels are compatible with TTL specifications.

4

### CONNECTION DIAGRAMS
**Top Views**




MOS-103

Note: Pin 1 is marked for orientation.

MOS-104

### ORDERING INFORMATION

| Package Type | Ambient Temperature Specifications | Access Time | |
|---|---|---|---|
| | | 450ns | 300ns |
| Molded | $0°C \leq T_A \leq +70°C$ | AM9232/33BPC | AM9232/33CPC |
| Cerdip | $0°C \leq T_A \leq +70°C$ | AM9232/33BCC | AM9232/33CCC |
| Side-Brazed Ceramic | $-55°C \leq T_A \leq +125°C$ | AM9232/33BDM | |
| | $0°C \leq T_A \leq +70°C$ | AM9232/33BDC | AM9232/33CDC |

## MAXIMUM RATINGS beyond which the useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| VCC with Respect to VSS | +7.0V |
| DC Voltage Applied to Outputs | −0.5V to +7.0V |
| DC Input Voltage | −0.5V to +7.0V |
| Power Dissipation (Package Limitation) | 1.0W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGE

| Part Number | Ambient Temperature | VCC | VSS |
|---|---|---|---|
| Am9232DC/PC/CC | $0°C \leq T_A \leq +70°C$ | +5.0V ±5% | 0V |
| Am9232/33DM | $-55°C \leq T_A \leq +125°C$ | +5.0V ±10% | 0V |

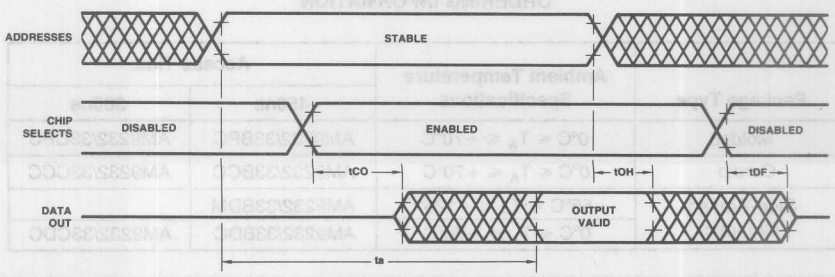
## ELECTRICAL CHARACTERISTICS over operating range

| Parameter | Description | Test Conditions | | Am9232/Am9233 Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| VOH | Output HIGH Voltage | IOH = −200μA | VCC = 4.75 | 2.4 | | Volts |
| | | | VCC = 4.50 | 2.2 | | |
| VOL | Output LOW Voltage | IOL = 3.2mA | | | 0.4 | Volts |
| VIH | Input HIGH Voltage | | | 2.0 | VCC+1.0 | Volts |
| VIL | Input LOW Voltage | | | −0.5 | 0.8 | Volts |
| ILI | Input Load Current | VSS ≤ VI ≤ VCC | | | 10 | μA |
| ILO | Output Leakage Current | VSS ≤ VO ≤ VCC Chip Disabled | +70°C | | 10 | μA |
| | | | +125°C (DM) | | 50 | |
| ICC | VCC Supply Current | | 0°C | | 80 | mA |
| | | | −55°C (DM) | | 100 | |
| CI | Input Capacitance | $T_A$ = 25°C, f = 1.0MHz All pins at 0V | | | 7.0 | pF |
| CO | Output Capacitance | | | | 7.0 | pF |

## SWITCHING CHARACTERISTICS over operating range

| Parameter | Description | Test Conditions | Am9232/33B Min. | Am9232/33B Max. | Am9232/33C Min. | Am9232/33C Max. | Unit |
|---|---|---|---|---|---|---|---|
| ta | Address to Output Access Time | tr = tf = 20ns Output Load: one standard TTL gate plus 100pF (Note 1) | | 450 | | 300 | ns |
| tCO | Chip Select to Output ON Delay | | | 150 | | 120 | ns |
| tOH | Previous Read Data Valid with Respect to Address Change | | 20 | | 20 | | ns |
| tDF | Chip Select to Output OFF Delay | | | 150 | | 120 | ns |

### SWITCHING WAVEFORMS




MOS-105

## PROGRAMMING INTRUCTIONS

### CUSTOM PATTERN ORDERING INFORMATION

The Am9232 is programmed from punched cards, card coding forms or paper tape in card image format as shown below.

Logic "1" = a more positive voltage (normally +5.0V)
Logic "0" = a more negative voltage (normally 0V)

**FIRST CARD**

| Column Number | Description |
|---|---|
| 10 thru 29 | Customer Name |
| 32 thru 37 | Total number of "1's" contained in the data. This is optional and should be left blank if not used. |
| 50 thru 62 | 9232 or 9233 |
| 65 thru 72 | Optional information |

**SECOND CARD**

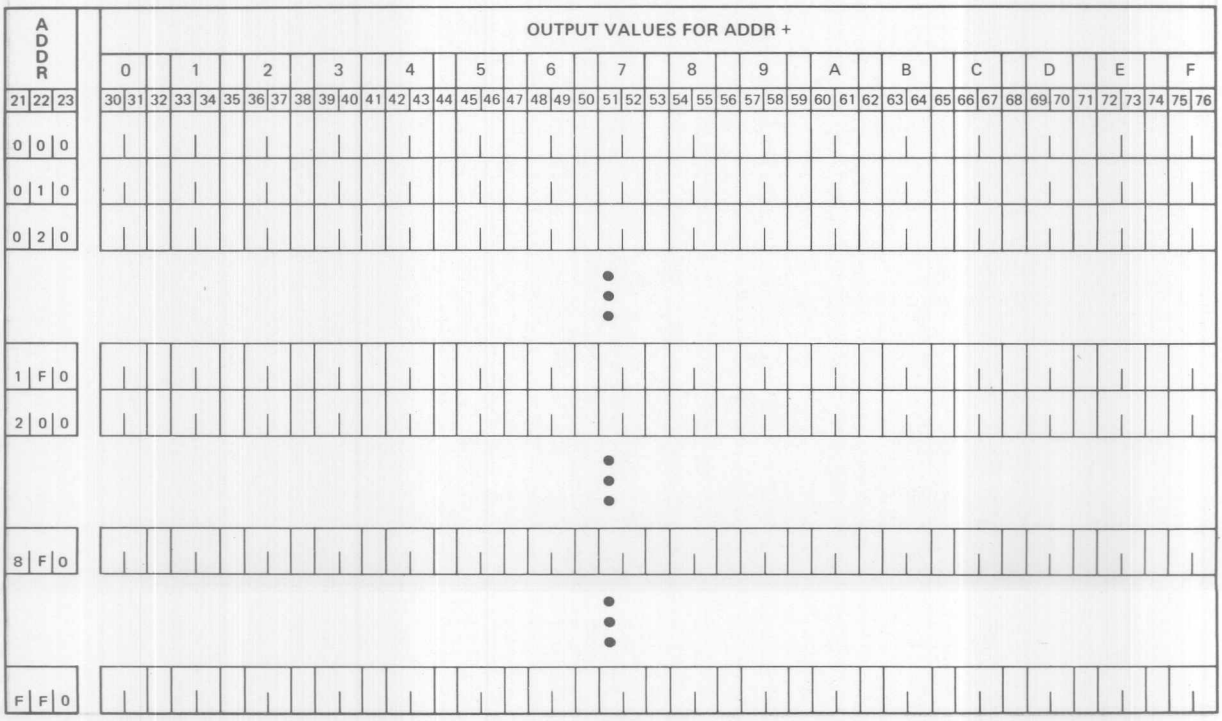
| Column Number | Description |
|---|---|
| 31 | CS2 input required to select chip (0 or 1); If CS2 = NC, column 31 = 2. |
| 33 | CS1 input required to select chip (0 or 1); If CS1 = NC, column 33 = 2. |

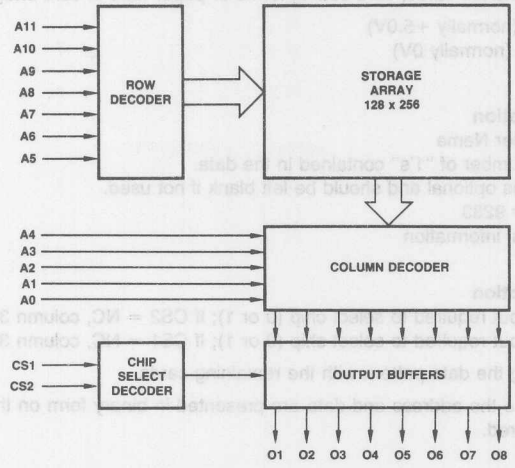
Two options are provided for entering the data pattern with the remaining cards.

**OPTION 1** is the Binary Option where the address and data are presented in binary form on the basis of one word per card. With this option 4096 data cards are required.

| Column Number | |
|---|---|
| 8, 10, 12, 14, 16, 18<br>20, 22, 24, 26, 28, 30 | Address input pattern with the most significant bit (A11) in column 8 and the least significant bit (A0) in column 30. |
| 40, 42, 44, 46, 48<br>50, 52, 54 | Output pattern with the most significant bit (O8) in column 40 and the least significant bit (O1) in column 54. |
| 73 thru 80 | Coding these columns is not essential and may be used for card identification purposes. |

**OPTION 2** is the Hexadecimal Option and is a much more compact way of presenting the data. This format requires only 256 data cards. Each data card contains the 8-bit output information for 16 storage locations in the memory. The address indicated in columns 21, 22 and 23 is the address of the data presented in columns 30 and 31. Addresses for successive data are assumed to be in incremental ascending order from the initial address. Since the address in columns 21, 22 and 23 always points only to the first data on the card, column 23 is always zero. Columns 21 and 22 take all hex values from 00 through FF:256 cards in all. Data is entered in hex values and may be any combination of 8 bits, that is, hex values from 00 through FF.




A11
A10
A9
A8
A7
A6
A5
ROW DECODER
STORAGE ARRAY 128 x 256
A4
A3
A2
A1
A0
COLUMN DECODER
CS1
CS2
CHIP SELECT DECODER
OUTPUT BUFFERS
O1
O2
O3
O4
O5
O6
O7
O8

MOS-106

# SHIFT REGISTERS

## NUMERICAL INDEX


| | | Page |
|---|---|---|
| Am14/1506/Am14/1507 | Dual 100-Bit Dynamic Shift Registers | 5-1 |
| Am1402A/1403A/1404A/ Am2802/2803/2804 | 1024-Bit Dynamic Shift Registers | 5-7 |
| Am2805/2806/2807/2808 | 512- and 1024-Bit Dynamic Shift Registers | 5-13 |
| Am2809 | Dual 128-Bit Static Shift Register | 5-19 |
| Am2810 | Dual 128-Bit Static Shift Register | 5-23 |
| Am2814/3114 | Dual 128-Bit Static Shift Register | 5-27 |
| Am2825/2826/2827 | 2048-Bit Dynamic Shift Registers | 5-31 |
| Am2833/2533 | 1024-Bit Static Shift Registers | 5-36 |
| Am2847/2896 | Quad 80-Bit and Quad 96-Bit Static Shift Registers | 5-40 |
| Am2855/2856/2857 | Quad 128-Bit, Dual 256-Bit and Single 512-Bit Static Shift Registers | 5-44 |
| Am4025/5025/4026/5026/ 4027/5027 | 2048-Bit Dynamic Shift Registers | 5-48 |
| Am4055/5055/4056/5056/ 4057/5057 | Quad 128-Bit, Dual 256-Bit and Single 512-Bit Static Shift Registers | 5-53 |
| Am9401/2401 | Dual 1024-Bit Dynamic Shift Register | 5-57 |

# SHIFT REGISTERS

## NUMERICAL INDEX


| | | Page |
|---|---|---|
| Am14/15S06/Am14/15S07 | Dual 100-Bit Dynamic Shift Registers | 5-1 |
| Am14/402A/1402A/1404A/ | | |
| Am2802/2803/2804 | 1024-Bit Dynamic Shift Registers | 5-7 |
| Am2805/2806/2807/2808 | 512- and 1024-Bit Dynamic Shift Registers | 5-13 |
| Am2809 | Dual 128-Bit Static Shift Register | 5-19 |
| Am2810 | Dual 128-Bit Static Shift Register | 5-23 |
| Am2814/3114 | Dual 128-Bit Static Shift Register | 5-27 |
| Am2825/2826/2827 | 2048-Bit Dynamic Shift Registers | 5-31 |
| Am2833/2933 | 1024-Bit Static Shift Registers | 5-36 |
| Am2847/2896 | Quad 80-Bit and Quad 96-Bit Static Shift Registers | 5-40 |
| Am2855/2856/2857 | Quad 128-Bit, Dual 256-Bit and Single 512-Bit Static Shift Registers | 5-44 |
| Am4025/5025/4029/5029/ | | |
| 4027/5027 | 2048-Bit Dynamic Shift Registers | 5-48 |
| Am4056/5056/4059/5059/ | | |
| 4057/5057 | Quad 128-Bit, Dual 256-Bit and Single 512-Bit Static Shift Registers | 5-53 |
| Am9401/2401 | Dual 1024-Bit Dynamic Shift Register | 5-57 |

# Am14/1506·Am14/1507

## Dual 100-Bit Dynamic Shift Registers

### Distinctive Characteristics

- Dual 100-bit silicon gate MOS shift registers
- DTL and TTL compatible
- Low-power dissipation of 0.4 mW/bit at 1 MHz
- 2 MHz frequency operation guaranteed
- 100% reliability assurance testing in compliance with MIL-STD-883
- Electrically tested and optically inspected die for the assemblers of hybrid products

### FUNCTIONAL DESCRIPTION

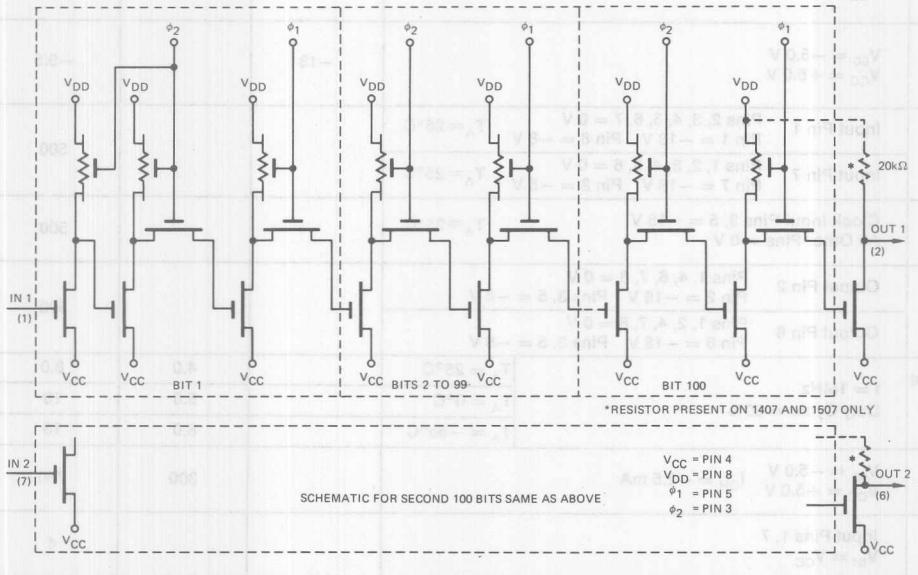
The Advanced Micro Devices dual 100-bit dynamic MOS shift registers are built using enhancement mode P-channel silicon gate MOS devices. The circuits use low-voltage circuitry for low-power dissipation and ease of interfacing into bipolar DTL and TTL circuits.

The shift registers can be driven by either DTL or TTL circuits or by MOS circuits and provide driving capability to MOS or bipolar circuits.

Silicon gate technology gives high-speed operation, low-power dissipation and low clock input capacitance.

The shift registers are ideal for low-cost buffer memories, long serial digital delay lines, etc. The devices are available in the commercial (0°C to +70°C) temperature range and the military (−55°C to +125°C) temperature range and are available with open drain output (Am14/1506), or with a 20kΩ pull-down resistor (Am14/1507) for easier interface to other circuitry.

### CIRCUIT DIAGRAM

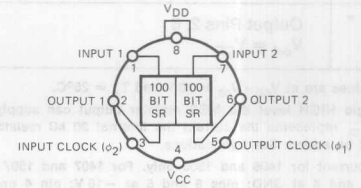



MOS-389

### ORDERING INFORMATION

| Package Type | Ambient Temperature | Output Resistor | Part Number |
|---|---|---|---|
| TO-99 | 0°C ≤ $T_A$ ≤ +70°C | No | AM1506 |
| | | Yes | AM1507 |
| | −55°C ≤ $T_A$ ≤ +125°C | No | AM1406 |
| | | Yes | AM1407 |

### CONNECTION DIAGRAM
Top View




MOS-390

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +160°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Power Dissipation | 500 mW |
| Data and Clock Input Voltages with respect to most Positive Supply Voltage, $V_{CC}$ | +0.5 V to −25 V |
| Power Supply Voltage, $V_{DD}$ with respect to $V_{CC}$ | +0.5 V to −25 V |

## ELECTRICAL CHARACTERISTICS

Am1506/1507 $T_A$ = 0°C to +70°C
Am1406/1407 $T_A$ = −55°C to +125°C
} unless otherwise specified

**DC Characteristics** Over Operating Temperature Range ($V_{DD}$ = −5.0 V ±5%, $V_{CC}$ = +5.0 V ±5% unless otherwise specified)

| Parameters | Test Conditions | Limits Over Specified Temperature Range Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|
| $V_{OH}$ (Note 2) Output HIGH Voltage | $I_{OH}$ = −2.5 mA<br>Load = 20 kΩ | 2.5 | 4.0 | | Volts |
| $V_{OL}$ (Note 2) Output LOW Voltage | $I_{OL}$ = 200 μA<br>1407, 1507 only | | −1.2 | 0.4 | Volts |
| $V_{IH}$ Input HIGH Voltage | $V_{DD}$ = −5.0 V<br>$V_{CC}$ = +5.0 V | 2.5 | 5.0 | 5.3 | Volts |
| $V_{IL}$ Input LOW Voltage | $V_{DD}$ = −5.0 V<br>$V_{CC}$ = +5.0 V | −10 | 0.2 | 0.8 | Volts |
| $V_{IHC}$ Clock Input HIGH Voltage | $V_{DD}$ = −5.0 V<br>$V_{CC}$ = +5.0 V | 3.5 | | 5.3 | Volts |
| $V_{ILC}$ Clock Input LOW Voltage | $V_{DD}$ = −5.0 V<br>$V_{CC}$ = +5.0 V | −13 | | −9.5 | Volts |
| $I_L$ Input Load Current | Input Pin 1: Pins 2, 3, 4, 5, 6, 7 = 0 V; Pin 1 = −18 V; Pin 8 = −8 V; $T_A$ = 25°C | | | 500 | nA |
| | Input Pin 7: Pins 1, 2, 3, 4, 5, 6 = 0 V; Pin 7 = −18 V; Pin 8 = −8 V; $T_A$ = 25°C | | | | |
| $I_{LC}$ Clock Input Current | Clock Input Pins 3, 5 = −18 V<br>All Other Pins = 0 V; $T_A$ = 25°C | | | 500 | nA |
| $I_{LO}$ (Note 3) Output Leakage Current | Output Pin 2: Pins 1, 4, 6, 7, 8 = 0 V; Pin 2 = −18 V; Pins 3, 5 = −8 V | | | 500 | nA |
| | Output Pin 6: Pins 1, 2, 4, 7, 8 = 0 V; Pin 6 = −18 V; Pins 3, 5 = −8 V | | | | |
| $I_{DD}$ (See Graphs) Power Supply Current (Note 4) | f = 1MHz<br>Duty Cycle = 60%<br>$T_A$ = 25°C | | 4.0 | 8.0 | mA |
| | $T_A$ = 0°C | | 5.0 | 10 | |
| | $T_A$ = −55°C | | 8.0 | 13 | |
| $Z_{out}$ Output ON Impedance | $V_{DD}$ = −5.0 V<br>$V_{CC}$ = +5.0 V<br>$I_{OH}$ = −2.5 mA | | 300 | 750 | Ω |
| $C_{IN}$ * Input Capacitance | Input Pins 1, 7<br>$V_{IN}$ = $V_{CC}$ | | | 4 | pF |
| $C_\phi$ * Clock Input Capacitance | Clock Input Pins 3, 5 $V_\phi$ = $V_{CC}$ | | | 40 | pF |
| | Clock Input Pins 3, 5 $V_\phi$ = −20 V Bias | | | 35 | |
| $C_{out}$ (Note 4) * Output Capacitance | Output Pins 2, 6<br>$V_{out}$ = $V_{CC}$ | | | 5 | pF |

**Note 1:** Typical values are at $V_{CC}$ - $V_{DD}$ = 10 V and $T_A$ = 25°C.

**Note 2:** In the logic HIGH level the MOS register output can supply 2.5 mA into the load combination of the internal pull-down resistor and the external load. In the logic LOW level, $I_{OL}$ represents the current the internal 20 kΩ resistor will sink. In order to insure current sinking capability for one standard TTL load, an external pull-down resistor must be added. See applications.

**Note 3:** Leakage current for 1406 and 1506 only. For 1407 and 1507 the output on pins 2 and 6 will exhibit a resistance when measured with the following bias conditions: pins 1, 6, and 8 at GND; pins 3 and 5 at −16 V; pin 4 open; measure pins 2 and 6. 25 kΩ ≥ $R_{OUT}$ ≥ 15 kΩ.

**Note 4:** Power dissipation is directly proportional to clock duty cycle. Duty cycle is defined as: clock frequency ($t\phi_1 pw + t\phi_2 pw + \frac{1}{2}[t_r + t_f]$).

***This paramenter is periodically sampled and is not 100% tested.**

## SWITCHING CHARACTERISTICS ($V_{DD} = -5\ V \pm 5\%$; $V_{CC} = +5\ V \pm 5\%$ unless otherwise specified)

| Parameter | Description | Test Conditions | Limits Over Specified Temperature Range Min. | Max. | Units |
|---|---|---|---|---|---|
| $f_c$ | Clock Frequency | $V_{IH} \geq 3.0\ V$ | (Note 5) | 2 | MHz |
| | | $V_{IH} \geq 2.5\ V$ | | 1 | |
| $t_{\phi PW}$ | Clock Pulse Width | $V_{IH} \geq 3.0\ V$ | 130 | | ns |
| | | $V_{IH} \geq 2.5\ V$ | 200 | | |
| $t\phi_d$ | Clock Pulse Delay | $\phi_{1\ PW} = 0.4\ \mu s$ $\phi_{2\ PW} = 0.2\ \mu s$ $f_c = 1\ MHz$ | 100 | | ns |
| $t_f$, $t_r$ | Clock Pulse Rise/Fall Time | $f_c = 1\ MHz$ | | 50 | ns |
| $t_s$ | Input Data Set Up Time | $f_c = 2\ MHz$ | 100 | | ns |
| | | $f_c = 1\ MHz$ | 200 | | |
| $t_h$ | Input Data Hold Time | | 100 | | ns |
| $t_{pd}$ | Propagation Delay $\phi_1$ to Output | $V_{ILC} - V_{CC} = -16\ V$ | | 100 | ns |

**Note 5:** See "Minimum Operating Frequency" graph for low limits on clock rate.

5

## DESCRIPTION OF TERMS

### OPERATIONAL TERMS

$V_{OH}$ Minimum logic HIGH output voltage with output HIGH current $I_{OH}$ flowing out of output.

$V_{OL}$ Maximum logic LOW output voltage with output LOW current $I_{OL}$ into output.

$V_{IH}$ Logic HIGH input voltage.
$V_{IL}$ Logic LOW input voltage.
$V_{ILC}$ Clock LOW input voltage.
$V_{IHC}$ Clock HIGH input voltage.
$I_L$ Input load current.
$I_{LO}$ Output leakage current.
$I_{DD}$ Power supply current.
$Z_{out}$ Output impedance with output sourcing 2.5 mA.
$C_{IN}$ Input capacitance.
$C_\phi$ Input clock capacitance.
$C_{OUT}$ Output capacitance.

### FUNCTIONAL TERMS

$\phi_1$, $\phi_2$ The two clock phases required by the dynamic shift register.
$f_c$ The clock frequency of the shift register.

### SWITCHING TERMS

$t\phi_d$ The delay between the LOW to HIGH transition of a clock phase to the HIGH to LOW transition of the other clock phase.

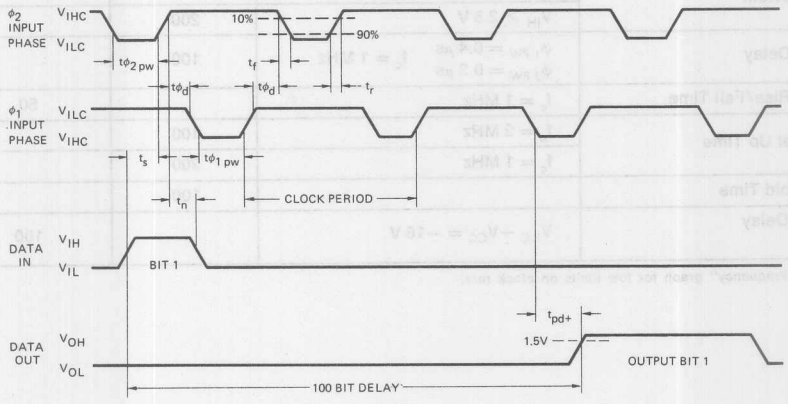
$t_{\phi PW}$ The clock pulse widths necessary for correct operation.

$t_f$, $t_r$ The clock pulse rise and fall times necessary for correct operation.

$t_s$ The time required for the input data to be present prior to the LOW to HIGH transition of the clock phase $\phi_2$ to ensure correct operation.

$t_h$ The time required for the input data to remain present after the LOW to HIGH transition of the clock phase $\phi_2$ to ensure correct operation.

$t_{pd+}$ The propagation delay from the HIGH to LOW clock phase $\phi_1$ transition to the output LOW to HIGH transition.

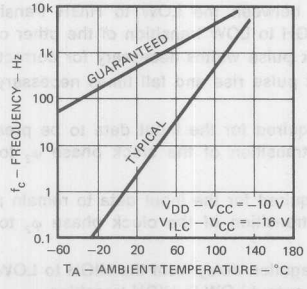



Clock Rise Time 10ns
Clock Fall Time 10ns
Data Amplitude +0.8V to +2.5V
Output Load 1 TTL Unit Load

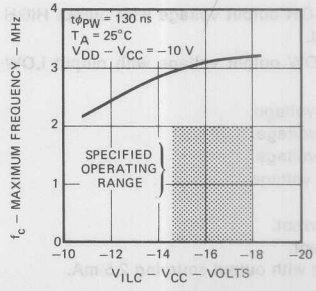
MOS-391

## SWITCHING CHARACTERISTICS

**Minimum Operating Frequency Versus Temperature**



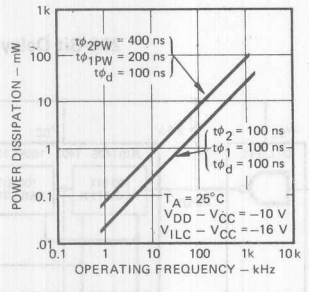

**Maximum Frequency Versus Clock Amplitude**



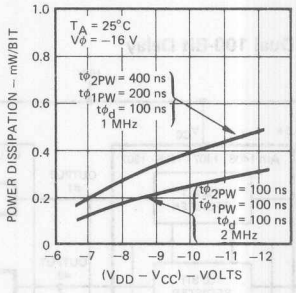

MOS-392

## SWITCHING CHARACTERISTICS

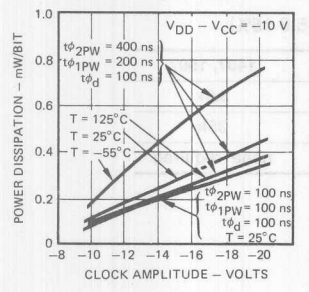
**Power Dissipation Versus Frequency**



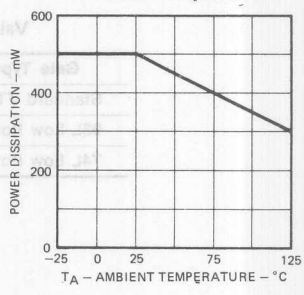

**Power Dissipation/Bit Versus Supply Voltage**



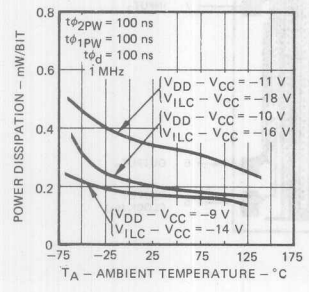

**Power Dissipation/Bit Versus Clock Amplitude**



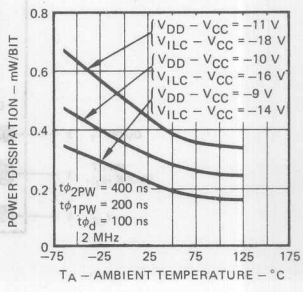

**Maximum Package Power Dissipation Versus Temperature**




**Power Dissipation/Bit at 2 MHz Versus Temperature**




**Power Dissipation/Bit at 1 MHz Versus Temperature**



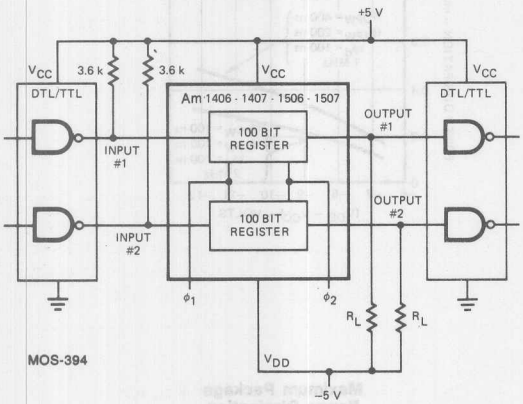

MOS-393

5

## APPLICATIONS

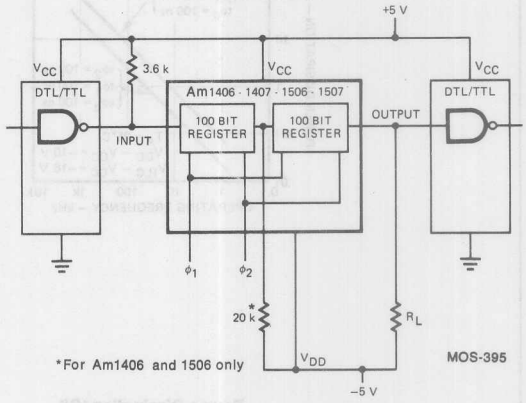
### DTL/TTL/MOS Interfaces

**Dual 100-Bit Delay**




MOS-394

**200-Bit Delay**



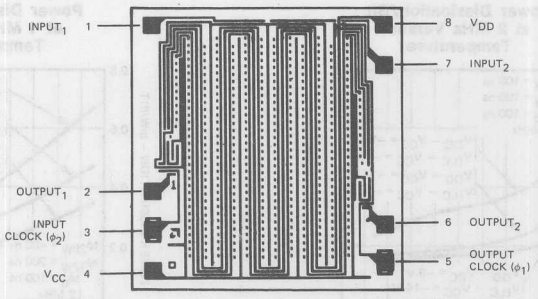

*For Am1406 and 1506 only

MOS-395

**Value of $R_L$ ($V_{DO}$ = –5.0 ±5%)**

| Gate Type | 1406, 1506 | 1407, 1507 |
|---|---|---|
| Standard TTL | 3.2k | 3.8k |
| 93L Low Power | 12.8k | 35k |
| 74L Low Power | 28k | none required |

### Metallization and Pad Layout




69 x 74 Mils

# Am1402A/Am1403A/Am1404A
# Am2802/Am2803/Am2804

## 1024-Bit Dynamic Shift Registers

### Distinctive Characteristics

- Quad 256-bit, dual 512-bit, single 1024-bit
- 10 MHz frequency operation guaranteed for Am2802, Am2803 and Am2804.
- Low power dissipation of 0.1 mW/bit at 1 MHz
- DTL and TTL compatible
- Both military and commercial grade devices available
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically tested and optically inspected die for the assemblers of hybrid products

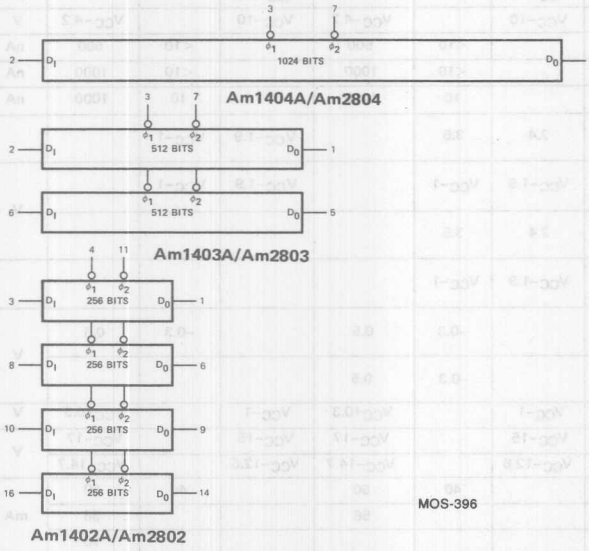
### FUNCTIONAL DESCRIPTION

The Am1402A, 3A, and 4A are 1024-bit silicon gate dynamic shift registers. The low threshold characteristics of this technology allow high-speed operation and DTL and TTL compatibility. The Am1402A is a quad 256-bit device; the Am1403A is a dual 512-bit register; and the Am1404A is a single 1024-bit register. All three devices require two-phase non-overlapping clocks, and provide a one-bit shift on each clock pulse. The Am2802, 3, and 4 registers are functionally identical to the Am1402A, 3A, and 4A, but are guaranteed to operate over frequencies from 400 Hz to 10 MHz.

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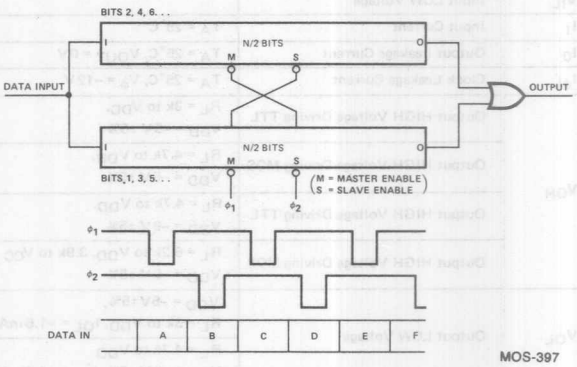
### BLOCK DIAGRAMS

**Am1402A/1403A/1404A Shift Registers**




MOS-396

**Functional Equivalent of Each Register**




MOS-397

Since the two registers shift on opposite clock pulses, a new data bit is entered on both $\phi_1$ and $\phi_2$. Data entering the register on $\phi_1$ will appear at the output on $\phi_1$ (from the negative edge of $\phi_1$ to the negative edge of $\phi_2$).

### ORDERING INFORMATION

| Part Number | Package Type | Temperature Range | Standard Speed Range Order Number | Extended Speed Range Order Number |
|---|---|---|---|---|
| Am1402A/ 2802 | Hermetic DIP | 0°C to +70°C | AM1402A | AM2802DC |
| | Hermetic DIP | −55°C to+125°C | AM1402ADM | AM2802DM |
| | Molded DIP | 0°C to +70°C | AM1402APC | AM2802PC |
| Am1403A/ 2803 | TO-99 | 0°C to +70°C | AM1403A | AM2803HC |
| | TO-99 | −55°C to +125°C | AM1403AHM | AM2803HM |
| | Molded DIP | 0°C to +70°C | AM1403APC | AM2803PC |
| Am1404A/ 2804 | TO-99 | 0°C to +70°C | AM1404A | AM2804HC |
| | TO-99 | −55°C to +125°C | AM1404AHM | AM2804HM |
| | Mini DIP Plastic | 0°C to +70°C | AM1404APC | AM2804PC |

| | |
|---|---|
| Power Dissipation (Note 1) | 600 mW |
| Data and Clock Input Voltages with respect to most Positive Supply Voltage, $V_{CC}$ | 0.3 V to −20 V |
| Power Supply Voltage, $V_{DD}$ with respect to $V_{CC}$ | 0.3 V to −20 V |

## OPERATING RANGE

| Part Number | $V_{CC}$ | $V_{DD}$ | Temperature Range |
|---|---|---|---|
| Am1402A, Am1403A, Am1404A | 5V ±5% | −4.75V to −9.45V | 0°C to +70°C |
| Am1402ADM, Am1403AHM, Am1404AHM | 5V ±5% | −4.75V to −9.45V | −55°C to +125°C |
| Am2802DC, Am2803HC, Am2804HC | 5V ±5% | −5V ±5% | 0°C to +70°C |
| Am2802DM, Am2803HM, Am2804HM | 5V ±5% | −5V ±5% | −55°C to +125°C |

## ELECTRICAL CHARACTERISTICS over operating range

| Parameters | Description | Test Conditions | | Am1402A, 3A, 4A Min. | Typ. | Max. | Am2802, 3, 4 Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | | $V_{CC}$−2.0 | | | $V_{CC}$−2.0 | | | V |
| $V_{IL}$ | Input LOW Voltage | | | $V_{CC}$−10 | | $V_{CC}$−4.2 | $V_{CC}$−10 | | $V_{CC}$−4.2 | V |
| $I_I$ | Input Current | $T_A$ = 25°C | | | <10 | 500 | | <10 | 500 | nA |
| $I_O$ | Output Leakage Current | $T_A$ = 25°C, $V_{OUT}$ = 0V | | | <10 | 1000 | | <10 | 1000 | nA |
| $I_{\phi L}$ | Clock Leakage Current | $T_A$ = 25°C, $V_\phi$ = −12V | | | 10 | 1000 | | 10 | 1000 | nA |
| $V_{OH}$ | Output HIGH Voltage Driving TTL | $R_L$ = 3k to $V_{DD}$, $V_{DD}$ = −5V ±5% | | 2.4 | 3.5 | | $V_{CC}$−1.9 | $V_{CC}$−1 | | V |
| | Output HIGH Voltage Driving MOS | $R_L$ = 4.7k to $V_{DD}$, $V_{DD}$ = −5V ±5% | | $V_{CC}$−1.9 | $V_{CC}$−1 | | $V_{CC}$−1.9 | $V_{CC}$−1 | | |
| | Output HIGH Voltage Driving TTL | $R_L$ = 4.7k to $V_{DD}$, $V_{DD}$ = −9V ±5% | | 2.4 | 3.5 | | | | | |
| | Output HIGH Voltage Driving MOS | $R_L$ = 6.2k to $V_{DD}$, 3.9k to $V_{CC}$ $V_{DD}$ = −9V ±5% | | $V_{CC}$−1.9 | $V_{CC}$−1 | | | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{DD}$ = −5V ±5%, $R_L$ = 3k to $V_{DD}$, $I_{OL}$ = −1.6mA | | | −0.3 | 0.5 | | −0.3 | 0.5 | V |
| | | $R_L$ = 4.7k to $V_{DD}$ $V_{DD}$ = −9V ±5%, $I_{OL}$ = −1.6mA | | | −0.3 | 0.5 | | | | |
| $V_{\phi H}$ | Clock Input HIGH Level | | | $V_{CC}$−1 | | $V_{CC}$+0.3 | $V_{CC}$−1 | | $V_{CC}$+0.3 | V |
| $V_{\phi L}$ | Clock Input LOW Level | $V_{DD}$ = −5V ±5% | | $V_{CC}$−15 | | $V_{CC}$−17 | $V_{CC}$−15 | | $V_{CC}$−17 | V |
| | | $V_{DD}$ = −9V ±5% | | $V_{CC}$−12.6 | | $V_{CC}$−14.7 | $V_{CC}$−12.6 | | $V_{CC}$−14.7 | |
| $I_{DD}$ (−5) (Note 1) | $V_{DD}$ Current, $V_{DD}$ = −5V ±5% | 5MHz Data Rate 33% Duty Cycle $V_{\phi L}$ = $V_{CC}$−17V | $T_A$ = 25°C | | 40 | 50 | | 40 | 50 | mA |
| | | | $T_A$ = 0°C | | | 56 | | | 56 | |
| | | | $T_A$ = −55°C | | | | | | 70 | |
| | $V_{DD}$ Current, $V_{DD}$ = −5V ±5% | 10MHz Data Rate 40% Duty Cycle $V_{\phi L}$ = $V_{CC}$−17 | $T_A$ = 25°C | | | | | 50 | 60 | mA |
| | | | $T_A$ = 0°C | | | | | | 68 | |
| | | | $T_A$ = −55°C | | | | | | 80 | |
| $I_{DD}$ (−9) (Note 1) | $V_{DD}$ Current, $V_{DD}$ = −9V ±5% | 3MHz Data Rate 26% Duty Cycle $V_{\phi L}$ = $V_{CC}$−14.7V | $T_A$ = 25°C | | 30 | 40 | | 30 | 40 | |
| | | | $T_A$ = 0°C | | | 45 | | | 45 | mA |
| | | | $T_A$ = −55°C | | | | | | 60 | |

Note: 1. Power dissipation is directly proportional to clock duty cycle and independent of frequency. The duty cycle is the clock LOW time (one clock line) divided by the clock period. At $V_{DD}$ = −9V the maximum duty cycle is 26%. The duty cycle should be kept as small as possible to minimize power dissipation.

## SWITCHING CHARACTERISTICS AND OPERATING CONDITIONS (Over Operating Range)

**Am1402A/Am1403A/Am1404A**

| Parameter | Description | Test Conditions | $V_{DD} = -5\ V \pm 5\%$ (Test Load 1) Min. | Typ. | Max. | $V_{DD} = -9\ V \pm 5\%$ (Test Load 2) Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $f_c$ | Clock Frequency Range | | (Note 1) | | 2.5 | (Note 1) | | 1.5 | MHz |
| $f_d$ | Data Repetition Rate | | (Note 1) | | 5.0 | (Note 1) | | 3.0 | MHz |
| $t_{\phi PW}$ | Clock Pulse Width | | 0.13 | | 10 | 0.17 | | 10 | μs |
| $t_{\phi d}$ | Clock Pulse Delay (Note 2) | $t_{\phi PW}$ = 130 ns | 10 | | (Note 2) | 10 | | (Note 2) | ns |
| $t_f$, $t_r$ | Clock Pulse Rise/Fall Time | | | | 1000 | | | 1000 | ns |
| $t_s$ | Data Set Up Time | $t_r = t_f \leq 50$ ns | 30 | | | 60 | | | ns |
| $t_h$ | Data Hold Time | $t_r = t_f \leq 50$ ns | 20 | | | 20 | | | ns |
| $t_{pd+}$, $t_{pd-}$ | Clock to Data Out Delay | | | | 90 | | | 110 | ns |
| $C_{IN}$* | Input Capacitance | @ 1 MHz, 250 mVPP | | 5 | 10 | | 5 | 10 | pF |
| $C_{OUT}$* | Output Capacitance | @ 1 MHz, 250 mVPP | | 5 | 10 | | 5 | 10 | pF |
| $C_\phi$* | Clock Capacitance | @ 1 MHz, 250 mVPP | | 110 | 140 | | 110 | 140 | pF |

## SWITCHING CHARACTERISTICS AND OPERATING CONDITIONS (Over Operating Range)

**Am2802/Am2803/Am2804**

Clock Pulse Width = 70nsec
Clock LOW Level = ($V_{CC}$−15)

$V_{DD} = -5\ V \pm 5\%$ (Test Load 1)

| Parameter | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $f_c$ | Clock Frequency Range | $t_r = t_f$ = 10 ns | (Note 1) | | 5.0 (Note 4) | MHz |
| $f_d$ | Data Repetition Rate (Note 1) | | (Note 3) | | 10.0 (Note 4) | MHz |
| $t_{\phi PW}$ | Clock Pulse Width | | 0.07 | | 10 | μs |
| $t_{\phi d}$ | Clock Pulse Delay | $t_{\phi PW}$ = 70 ns | 10 | | (Note 2) | ns |
| $t_f$, $t_r$ | Clock Pulse Rise/Fall Time | | | | 1000 | ns |
| $t_s$ | Data Set Up Time | | 30 | | | ns |
| $t_h$ | Data Hold Time | | 20 | | | ns |
| $t_{pd+}$, $t_{pd-}$ | Clock to Data Out Delay | | | | 90 | ns |

Notes:
1. See minimum operating frequency graph for low limits on data rep. rate.
2. Upper limit on $t_{\phi d}$ is determined by minimum frequency.
3. See max clock pulse delay graph for guarantee.
4. For additional information on 10MHz operation (5MHz clock rate) see AMD application note dated July 1973 on "Applications of Dynamic Shift Registers."

## DESCRIPTION OF TERMS

### OPERATIONAL TERMS

$V_{OH}$ Minimum logic HIGH output voltage with output HIGH current $I_{OH}$ flowing out of output.

$V_{OL}$ Maximum logic LOW output voltage with output LOW current $I_{OL}$ into junction of output and load resistor.

$V_{IH}$ Logic HIGH input voltage.
$V_{IL}$ Logic LOW input voltage.
$V_{OL}$ Clock LOW input voltage.
$V_{OH}$ Clock HIGH input voltage.
$I_I$ Input leakage current.
$I_O$ Output leakage current.
$I_{DD}$ Power supply current.
$C_{IN}$ Input capacitance.
$C_\phi$ Input clock capacitance.
$C_{OUT}$ Output capacitance.

### FUNCTIONAL TERMS

$\phi_1$, $\phi_2$ The two clock phases required by the dynamic shift register.
$f_c$ The clock frequency of the shift register.
$f_d$ The input data repetition rate.

### SWITCHING TERMS

$t_{\phi_d}$ The delay between the LOW to HIGH transition of a clock phase to the HIGH to LOW transition of the other clock phase.

$t_{\phi PW}$ The clock pulse widths necessary for correct operation.

$t_f$, $t_r$ The clock pulse rise and fall times necessary for correct operation.

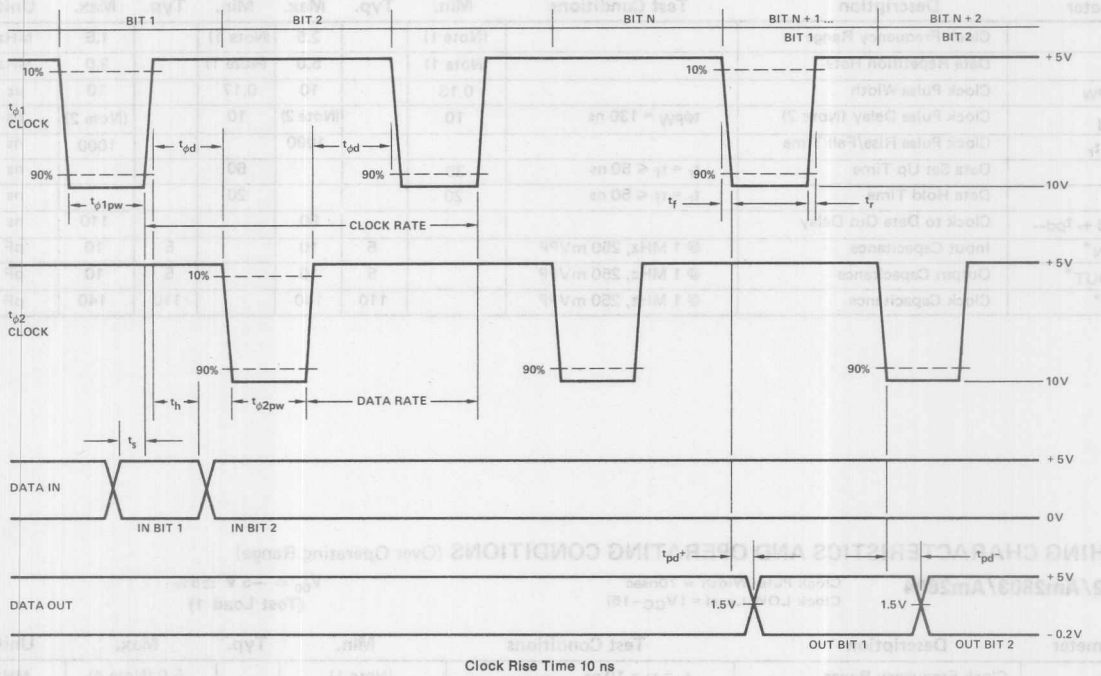
$t_s$ The time required for the input data to be present prior to the LOW to HIGH transition of the clock phase to ensure correct operation.

$t_h$ The time required for the input data to remain present after the LOW to HIGH transition of the clock phase to ensure correct operation.

$t_{pd+}$ The propagation delay from the HIGH to LOW clock phase $\phi_1$ transition to the output LOW to HIGH transition.

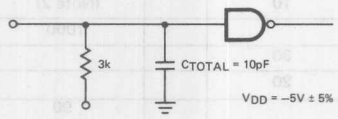
$t_{pd-}$ The propagation delay from the HIGH to LOW clock phase $\phi_2$ transition to the output HIGH to LOW transition.

## SWITCHING WAVEFORMS

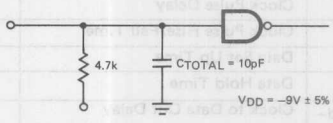



Clock Rise Time 10 ns
Clock Fall Time 10 ns
Output Load 1 TTL Load

**Test Load 1**

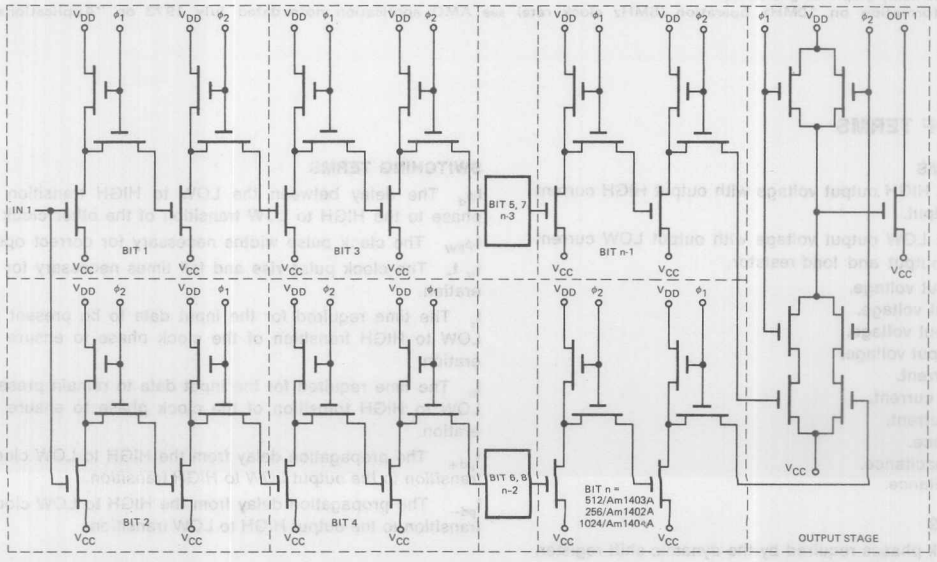



**Test Load 2**




MOS-398

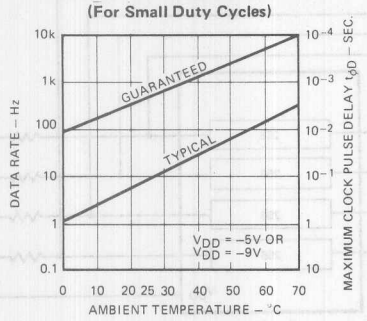
## CIRCUIT DIAGRAM



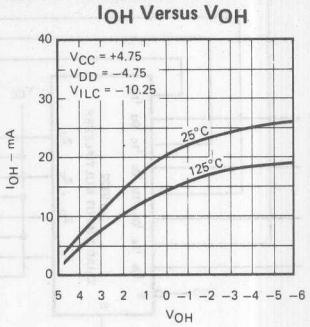

MOS-399

## POWER CHARACTERISTICS

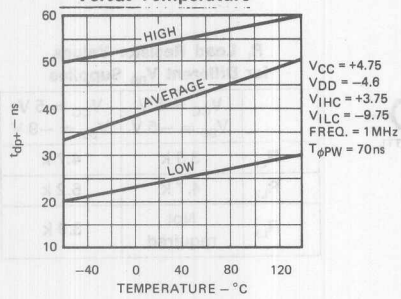
### Minimum Operating Data Rate or Maximum Clock Pulse Delay Versus Temperature (For Small Duty Cycles)



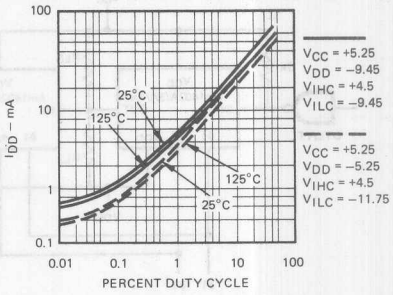

### $I_{OH}$ Versus $V_{OH}$




### Typical Range of $t_{pd+}$ Versus Temperature



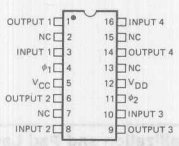

### $I_{DD}$ Versus Clock Duty Cycle



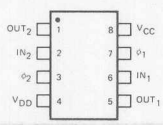

MOS-400

## ORDERING INFORMATION

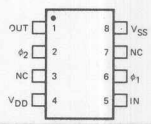
### Am2802/Am1402A



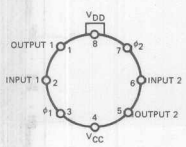

### Am2803/Am1403A



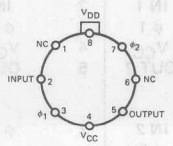

### Am2804/Am1404A




### Am2803/Am1403A




### Am2804/Am1404A

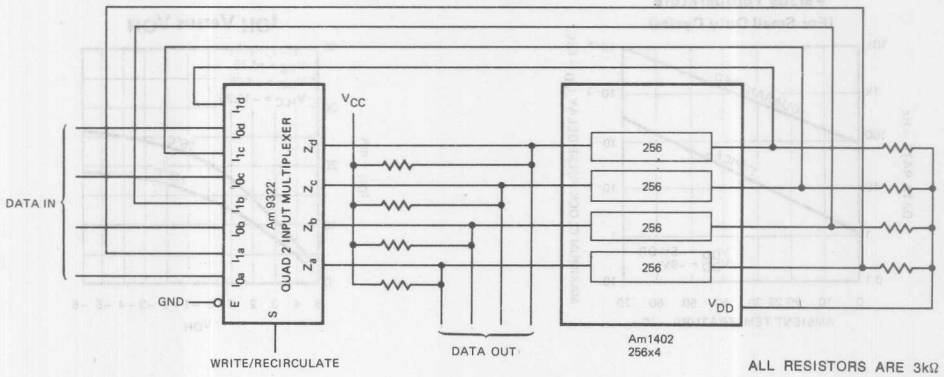



MOS-401

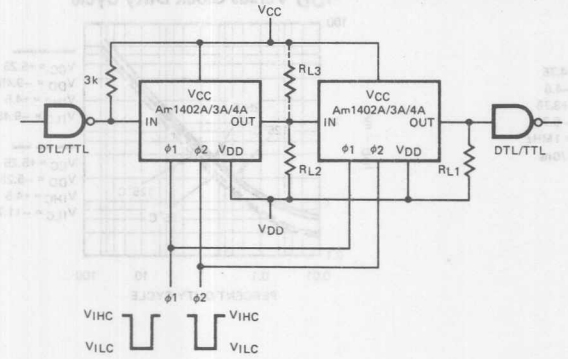
## APPLICATIONS

### 256-Bit Delay

Write Recirculate Logic




### DTL/TTL To MOS To DTL/TTL Interface



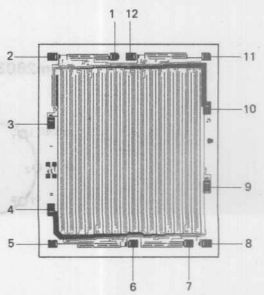

**$R_L$ Load Resistor Values for Different $V_{DD}$ Supplies**

| | $V_{CC} = 5$ V<br>$V_{DD} = -5$ V | $V_{CC} = 5$ V<br>$V_{DD} = -9$ V |
|---|---|---|
| $R_{L1}$ | 3.0 k | 4.7 k |
| $R_{L2}$ | 4.7 k | 6.2 k |
| $R_{L3}$ | Not required | 3.9 k |

MOS-402

| PAD | 1402A/2802 PIN | 1402A/2802 SIGNAL | 1403A/2803 PIN | 1403A/2803 SIGNAL | 1404A/2804 PIN | 1404A/2804 SIGNAL |
|---|---|---|---|---|---|---|
| 1 | 1 | OUT 1 | | | | |
| 2 | 3 | IN 1 | 2 | IN 1 | 2 | IN |
| 3 | 4 | $\phi$ 1 | 3 | $\phi$ 1 | 3 | $\phi$ 1 |
| 4 | 5 | $V_{CC}$ | 4 | $V_{CC}$ | 4 | $V_{CC}$ |
| 5 | 6 | OUT 2 | 5 | OUT 2 | 5 | OUT |
| 6 | 8 | IN 2 | | | | |
| 7 | 9 | OUT 3 | | | | |
| 8 | 10 | IN 3 | 6 | IN 2 | 7 | $\phi$ 2 |
| 9 | 11 | $\phi$ 2 | 7 | $\phi$ 2 | | |
| 10 | 12 | $V_{DD}$ | 8 | $V_{DD}$ | | |
| 11 | 14 | OUT 4 | 1 | OUT 1 | 8 | $V_{DD}$ |
| 12 | 16 | IN 4 | | | | |

**Metallization and Pad Layout**




DIE SIZE .109" X .131"

# Am2805/2806/2807/2808

## 512-and 1024-Bit Dynamic Shift Registers

### Distinctive Characteristics

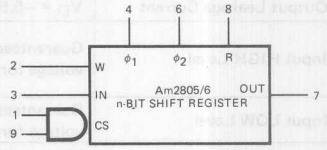
- Am2805 Plug-in Replacement Intel 1405A and Signetics 2505
  Am2806 Plug-in Replacement Signetics 2512
  Am2807 Plug-in Replacement Signetics 2524
  Am2808 Plug-in Replacement Signetics 2525
- On chip recirculate and chip select controls
- 100% reliability assurance testing in compliance with MIL-STD-883
- TTL and DTL compatible
- Full military temperature range devices available

### FUNCTIONAL DESCRIPTION

The Am2805 and Am2807 are 512-bit dynamic shift registers with recirculate logic on chip. The Am2806 and Am2808 are 1024-bit dynamic shift registers which also have built-in recirculate logic. When the write input is HIGH, data on the data input enters the first bit of the register during the $\phi_2$ clock time. If the write input is LOW, then the output of the register is written into the first bit instead. Data in the last bit of the register appears on the data output during the $\phi_1$ clock time if the read line is HIGH. If the read line is LOW, the output is OFF (high impedance state). The outputs of all four devices are open drains; they pull the output to $V_{CC}$ when ON and exhibit a very high impedance when OFF. An external pull-down resistor to ground or $V_{DD}$ must be used to establish the LOW logic level.

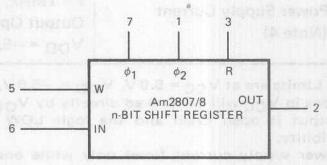
The Am2805 and Am2806 also have two chip select inputs, $CS_1$ and $CS_2$. If either of these inputs is LOW, the register recirculates and the output remains OFF, regardless of the state of the read and write lines. All inputs except the clocks are TTL/DTL compatible. A TTL input may be driven by the output if a 3k pull-down resistor to $V_{DD}$ is used. The register outputs can be wire-ORed for expansion. The devices are guaranteed to operate at speeds up to 3MHz.

### LOGIC SYMBOLS




Am2805 n = 512
Am2806 n = 1024

$V_{CC}$ = Pin 5
$V_{DD}$ = Pin 10

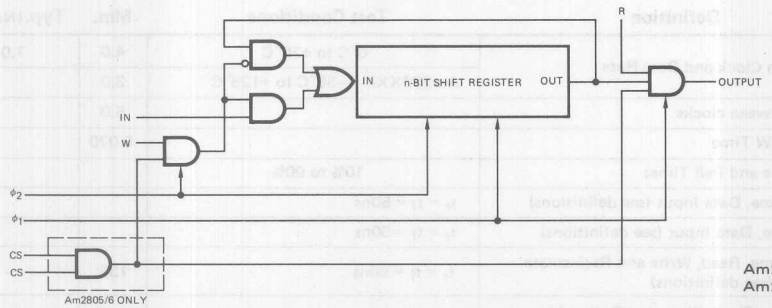



Am2807 n = 512
Am2808 n = 1024

$V_{CC}$ = Pin 8
$V_{DD}$ = Pin 4

MOS-494

### LOGIC DIAGRAM




Am2805/7 n = 512
Am2806/8 n = 1024

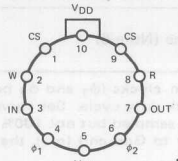
MOS-495

### ORDERING INFORMATION

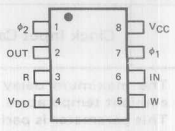
| Ambient Temperature | Package Type | Length | |
|---|---|---|---|
| | | 512 Bits | 1024 Bits |
| $0°C \leq T_A \leq +70°C$ | Molded DIP (8 Pin) | AM2807PC | AM2808PC |
| | TO-100 (10 Pin) | AM2805HC | AM2806HC |
| $-55°C \leq T_A \leq +125°C$ | TO-100 (10 Pin) | AM2805HM | AM2806HM |

### CONNECTION DIAGRAMS
Top View

**Am2805/6**




**Am2807/8**




Note: PIN 1 is marked for orientation.

MOS-496

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| DC Input Voltage with Respect to $V_{CC}$ | −20V to +0.3V |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

$V_{DD}$ = −5V ±5%, $V_{CC}$ = 5.0V ±5%
Am280XXM $T_A$ = −55°C to +125°C
Am280XXC $T_A$ = 0°C to +70°C

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage (Notes 2 & 3) | $V_{CC}$ = MIN., $I_{OH}$ = 1.6mA, ($R_L$ = 5.6kΩ) | | 3.6 | 4.0 | | Volts |
| | | $I_{OH}$ = 2.6mA, ($R_L$ = 3kΩ) | | 2.4 | 3.5 | | |
| $I_{OL}$ | Output Leakage Current | $V_O$ = −5.5V, $V_{\phi1}$ = $V_{\phi2}$ = −12V | | | 10 | 1000 | nA |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs except clocks | Am1405 | $V_{CC}$−2.0 | | $V_{CC}$+0.3 | Volts |
| | | | Am2505/12/24/25 | $V_{CC}$−1.8 | | $V_{CC}$+0.3 | |
| | | | Am2805/6/7/8 | $V_{CC}$−1.0 | | $V_{CC}$+0.3 | |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs except clocks | | $V_{CC}$−10 | | $V_{CC}$−4.2 | Volts |
| $I_I$ | Input Leakage Current | $V_{IN}$ = −5.5V, $T_A$ = 25°C | | | 10 | 500 | nA |
| $I_\phi$ | Clock Input Leakage Current | $V_\phi$ = −12V, $T_A$ = 25°C | | | 10 | 1000 | nA |
| $V_{\phi H}$ | Clock HIGH Level | | | $V_{CC}$−1.0 | | $V_{CC}$+0.3 | V |
| $V_{\phi L}$ | Clock LOW Level | | | $V_{CC}$−17 | | $V_{CC}$−14.5 | V |
| $I_{DD}$ | Power Supply Current (Note 4) | f = 1MHz, $T_A$ = 25°C Output Open $V_{DD}$ = −5.5V, $t_{\phi L}$ = 150ns | Am2805/7 | | 7 | 12 | mA |
| | | | Am2806/8 | | 10 | 20 | |

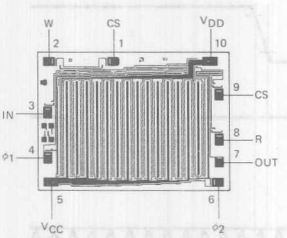
Notes: 1. Typical Limits are at $V_{CC}$ = 5.0V, $V_{DD}$ = −5.0V, 25°C Ambient and maximum loading.
2. Variations in $V_{CC}$ will be tracked directly by $V_{OH}$ and input thresholds.
3. The output is open drain and the logic LOW level must be defined by an external pull-down resistor. A 3k resistor to $V_{DD}$ provides TTL compatibility.
4. The power supply current flows only while one clock is LOW. Average power is therefore directly proportional to clock duty cycle (ratio of clock LOW time to total clock period.) See curves next page.

## SWITCHING CHARACTERISTICS ($T_A$ = 0°C to +70°C, $V_{CC}$ = +5.0V ±5%, $V_{DD}$ = −5.0V ±5%, $V_{\phi L}$ = −11V)

| Parameters | Definition | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum Clock and Data Rate | 0°C to +70°C | | 4.0 | 7.0 | | MHz |
| | | Am280XXM −55°C to +125°C | | 3.0 | | | |
| $t_{\phi d}$ | Delay Between clocks | | | 5.0 | | Note 5 | ns |
| $t_{\phi pw}$ | Clock LOW Time | | | 0.070 | | Note 8 | μs |
| $t_r$, $t_f$ | Clock Rise and Fall Times | 10% to 90% | | | | 1.0 | μs |
| $t_s$(D) | Set-up Time, Data Input (see definitions) | $t_r$ = $t_f$ = 50ns | | | | 150 | ns |
| $t_h$(D) | Hold Time, Data Input (see definitions) | $t_r$ = $t_f$ = 50ns | | | | 0 | ns |
| $t_s$(C) | Set-up Time, Read, Write and Recirculate Controls (see definitions) | $t_r$ = $t_f$ = 50ns | | 135 | | | ns |
| $t_h$(C) | Hold Time, Read, Write and Recirculate Controls (see definitions) | $t_r$ = $t_f$ = 50ns | | 0 | | | ns |
| $t_{pd}$ | Delay, Clock to Data Out | R = HIGH | 0°C to +70°C | | | 100 | ns |
| | | | −55°C to +125°C | | | 150 | |
| $C_{in}$, $C_{out}$ | Capacitance, Any Input and Output (Note 6) | f = 1MHz, $V_{IN}$ = $V_{CC}$ | | | | 5.0 | pF |
| $C_\phi$ | Clock Input Capacitance (Note 6) | f = 1MHz, $V_{IN}$ = $V_{CC}$ | Am2805/7 | | | 50 | pF |
| | | | Am2806/8 | | | 100 | |

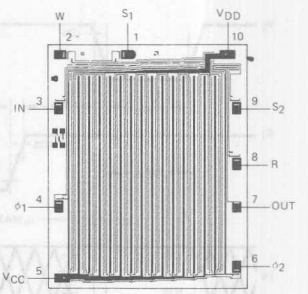
Notes: 5. The maximum delay between clocks ($\phi_1$ and $\phi_2$ both HIGH) is a function of junction temperature. The junction temperature is a function of ambient temperature and clock duty cycle. See curves for minimum frequency.
6. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.
7. For some reason known only to God and Intel, the convention for $\phi_1$ and $\phi_2$ for this device are reversed from the normal. $\phi_1$ is the output clock and $\phi_2$ is the input clock.
8. 100μsec or 50% duty cycle, whichever is less.

**Metallization and Pad Layout Am2805/7**




106 x 78 Mils

**Metalization and Pad Layout Am2806/8**




106 x 131 Mils

## DEFINITION OF TERMS

**Dynamic Shift Register** A shift register in which data storage occurs on small capacitive nodes rather than in bistable logic circuits. Dynamic shift registers must be clocked continuously to maintain the charge stored on the nodes.

$\phi_1$, $\phi_2$ The two clock pulses applied to the register. The clock is ON when it is at its negative voltage level and OFF when it is at $V_{SS}$ or $V_{CC}$. Data is accepted into the master of each bit during $\phi_2$ and is transferred to the slave of each bit during $\phi_1$.

$f_{max}$ The maximum frequency at which the register will operate. This is the data rate through the register and also the frequency of each clock signal.

$t_{\phi d}$ Clock delay time. The time elapsing between the LOW-to-HIGH transition of one clock input and the HIGH-to-LOW transition of the other clock input. During $t_{\phi d}$ both clocks are HIGH and all data is stored on capacitive nodes.

$t_{\phi pw}$ Clock pulse width. The LOW time of each clock signal. During $t_{\phi pw}$ one of the clocks is ON, and data transfer between master and slave or slave and master occurs.

$t_r$, $t_f$ Clock rise and fall times. The time required for the clock signals to change from 10% to 90% of the total level change occuring.

$t_s$(D) Data set-up time. The time prior to the LOW-to-HIGH transition of $\phi_2$ during which the data on the data input must be steady to be correctly written into the memory.

$t_h$(D) Data hold time. The time following the LOW-to-HIGH transition of $\phi_2$ during which the data must be steady. To correctly write data into the register, the data must be applied by $t_s$(D) before this transition and must not be changed until $t_h$(D) after this transition.

$t_s$(C), $t_h$(C) The set-up and hold times for the Read, Write, and Chip Select controls, relative to the LOW-to-HIGH transition of the appropriate clock phase.

$t_{pd}$ The delay from the start of a read cycle to correct data present at the register output. A read cycle is begun when $\phi_1$ is LOW AND Read is HIGH.

5


## DEFINITION OF TERMS

**Dynamic Shift Register** A shift register in which data storage occurs on small capacitive nodes rather than in bistable logic circuits. Dynamic shift registers must be clocked continuously to maintain the charge stored on the nodes.

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$t_{\phi pw}$ Clock pulse width. The LOW time of each clock signal. During $t_{\phi pw}$ one of the clocks is ON, and data transfer between master and slave or slave and master occurs.

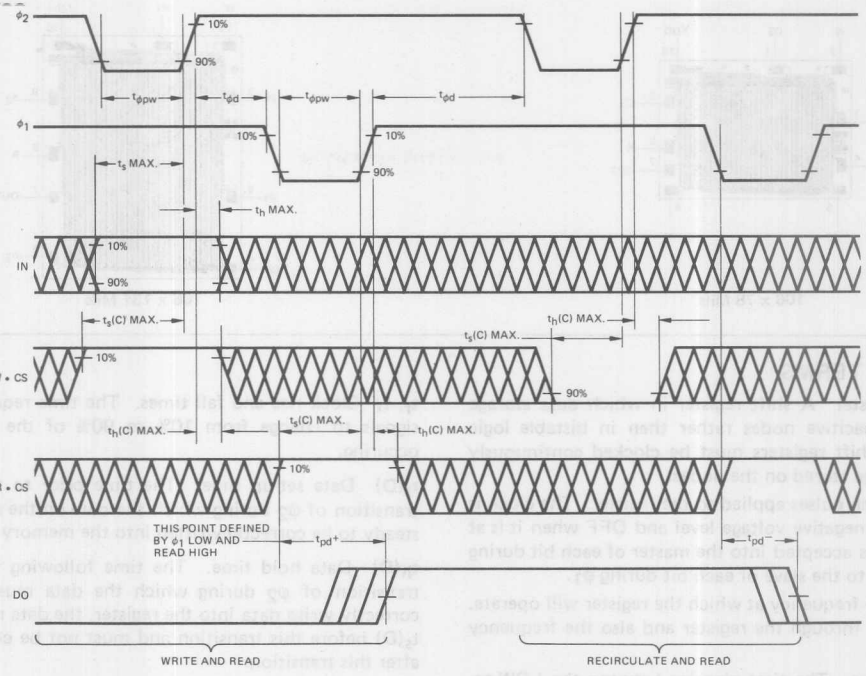
$t_r$, $t_f$ Clock rise and fall times. The time required for the clock signals to change from 10% to 90% of the total level change occuring.

$t_s$(D) Data set-up time. The time prior to the LOW-to-HIGH transition of $\phi_2$ during which the data on the data input must be steady to be correctly written into the memory.

$t_h$(D) Data hold time. The time following the LOW-to-HIGH transition of $\phi_2$ during which the data must be steady. To correctly write data into the register, the data must be applied by $t_s$(D) before this transition and must not be changed until $t_h$(D) after this transition.

$t_s$(C), $t_h$(C) The set-up and hold times for the Read, Write, and Chip Select controls, relative to the LOW-to-HIGH transition of the appropriate clock phase.

$t_{pd}$ The delay from the start of a read cycle to correct data present at the register output. A read cycle is begun when $\phi_1$ is LOW AND Read is HIGH.

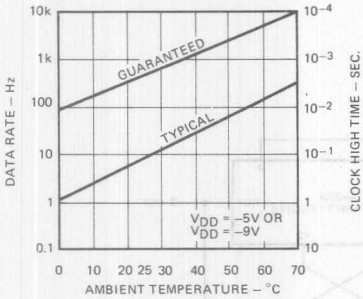



MOS-497

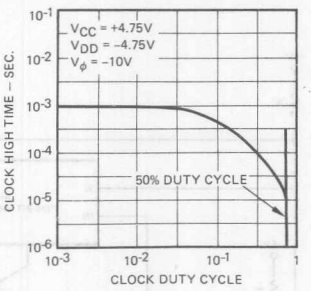
## KEY TO TIMING DIAGRAM

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| ——— | MUST BE STEADY | WILL BE STEADY |
| ——— | | |
| ▨ | MAY CHANGE FROM H TO L | WILL BE CHANGING FROM H TO L |
| ▨ | MAY CHANGE FROM L TO H | WILL BE CHANGING FROM L TO H |
| ▨ | DON'T CARE; ANY CHANGE PERMITTED | CHANGING; STATE UNKNOWN |

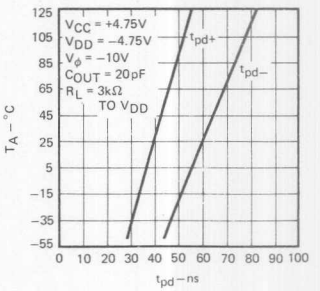
### or Maximum Clock Pulse Delay Versus Temperature



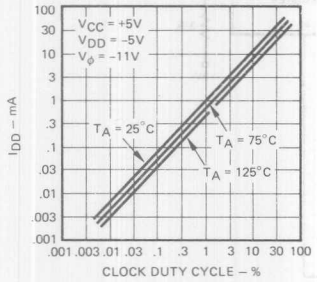

### Maximum Clock High Time Versus Clock Duty Cycle



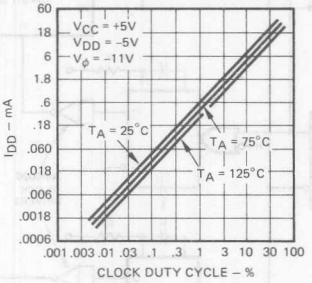

### Propagation Delay Versus Ambient Temperature



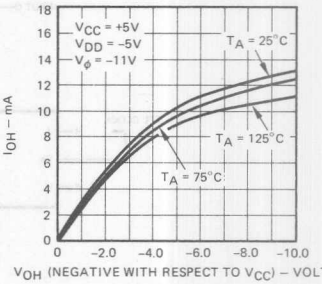

### Am2806/8 $I_{DD}$ Current Versus Clock Duty Cycle




### Am2805/7 $I_{DD}$ Current Versus Clock Duty Cycle



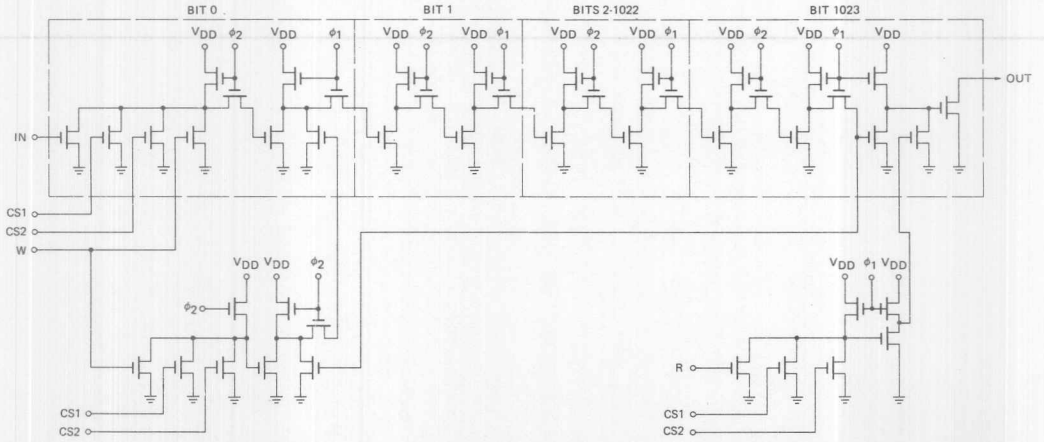

### $V_{OH}$ Versus $I_{OH}$




MOS-498

5

## SCHEMATIC DIAGRAM



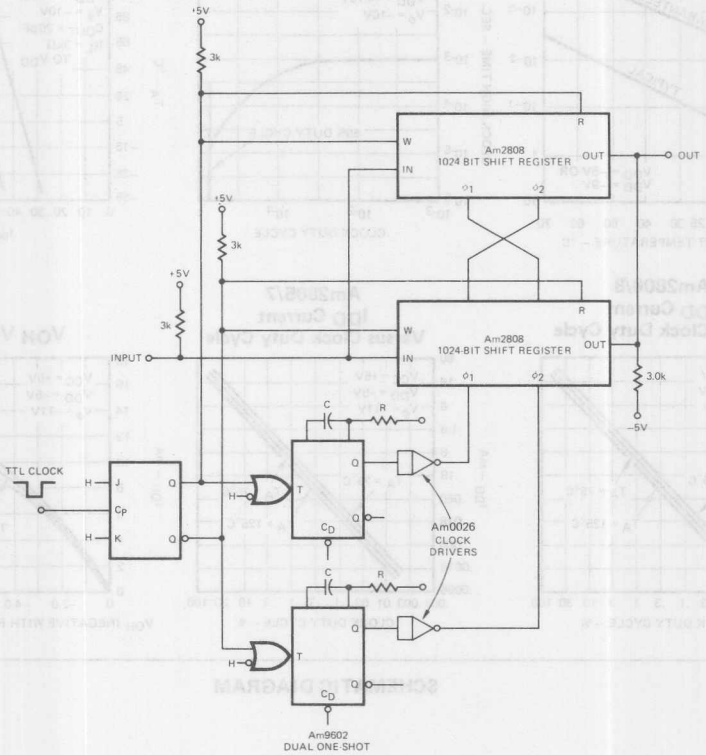

Note: No CS inputs on Am2807/8

⏚ = $V_{CC}$

MOS-499

## APPLICATIONS

**Multiplexed 2048-Bit Recirculating Register**
**$f_{max}$ = 6MHz**




MOS-500

# Am2809

## Dual 128-Bit Static Shift Register

### Distinctive Characteristics

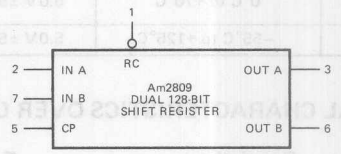
- Second source to Signetics 2521.
- TTL compatible on clock and data inputs.
- Operation guaranteed from DC-to-2.5MHz.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Low capacitance on clock and data inputs.

### FUNCTIONAL DESCRIPTION

The Am2809 is a dual 128-bit static shift register built using P-channel silicon gate MOS technology. The two registers have a common clock input which is low-threshold TTL compatible. The registers also have built-in recirculate feedback. When the recirculate control ($\overline{RC}$) is LOW, the data on the data output of each register is fed back to the corresponding register input. When $\overline{RC}$ is HIGH, each register accepts data from the data input. Each of the register outputs can drive one standard TTL load or three Am93L series low-power unit loads.

Data in the Am2809 is shifted on the LOW-to-HIGH edge of the input clock. Data on the data inputs must remain steady for a set-up time before and a hold time after this clock transition. Since storage in the register is static, the register may be halted indefinitely with the clock in the HIGH state.

### LOGIC SYMBOL

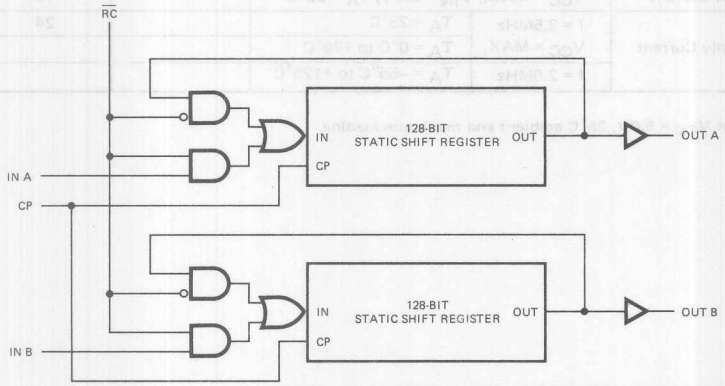



$V_{CC}$ = Pin 8
$V_{GG}$ = Pin 4

MOS-403

5

### LOGIC BLOCK DIAGRAM



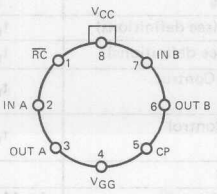

MOS-404

### ORDERING INFORMATION

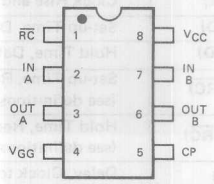
| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +70°C | AM2809PC |
| TO-5 | 0°C to +70°C | AM2809HC |
| TO-5 | −55°C to +125°C | AM2809HM |

### CONNECTION DIAGRAMS
Top Views

**Am2809HC**
**Am2809HM**




**Am2809PC**




MOS-405

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| DC Input Voltage with Respect to $V_{CC}$ | −20V to +0.3V |

## OPERATING RANGE

| Part Number | Ambient Temperature | $V_{CC}$ | $V_{GG}$ |
|---|---|---|---|
| Am2809PC<br>Am2809HC | 0°C to +70°C | 5.0V ±5% | −12V ±5% |
| Am2809HM | −55°C to +125°C | 5.0V ±5% | −12V ±5% |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −0.1mA | | $V_{CC}$ −1.5 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 1.6mA | | | −4 | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | $V_{CC}$ −1 | | $V_{CC}$ +0.3 | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | $V_{CC}$ −3.95 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0 | $T_A$ = 25°C | | 10 | 500 | nA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.4V, | $T_A$ = 25°C | | 10 | 500 | nA |
| $I_{GG}$ | Power Supply Current | f = 2.5MHz<br>$V_{CC}$ = MAX. | $T_A$ = 25°C | | 24 | 32 | mA |
| | | | $T_A$ = 0°C to +70°C | | | 38 | |
| | | f = 2.0MHz | $T_A$ = −55°C to +125°C | | | 44 | |

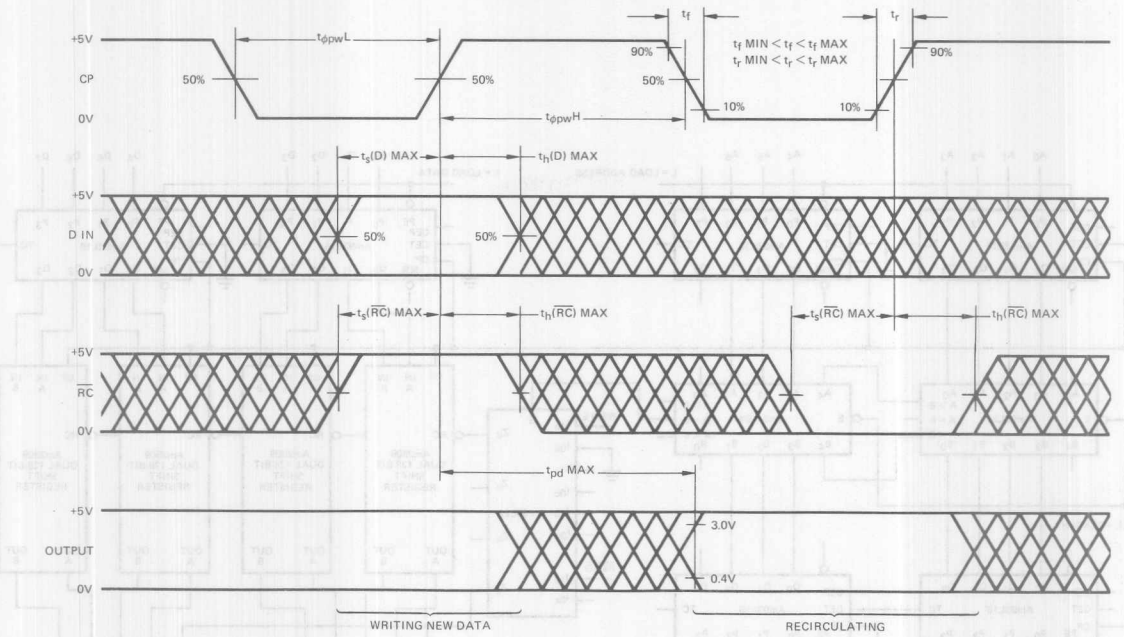
Note: 1. Typical Limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions | Am2809PC Am2809HC Min. | Typ. | Max. | Am2809HM Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $f_c$ | Clock Frequency Range | | 0 | | 2.5 | 0 | | 2.0 | MHz |
| $t_{\phi pw}H$ | Clock HIGH Time | | 0.2 | | ∞ | 0.25 | | ∞ | μs |
| $t_{\phi pw}L$ | Clock LOW Time | | 0.2 | | 100 | 0.25 | | 100 | μs |
| $t_r$, $t_f$ | Clock Rise and Fall Times | 10% to 90% | | | 1.0 | | | 1.0 | μs |
| $t_s$(D) | Set-up Time, Data Input (see definitions) | $t_r = t_f$ = 50ns | 75 | | | 100 | | | ns |
| $t_h$(D) | Hold Time, Data Input (see definitions) | $t_r = t_f$ = 50ns | 50 | | | 65 | | | ns |
| $t_s(\overline{RC})$ | Set-up Time, Recirculate Control (see definitions) | $t_r = t_f$ = 50ns | 50 | | | 100 | | | ns |
| $t_h(\overline{RC})$ | Hold Time, Recirculate Control (see definitions) | $t_r = t_f$ = 50ns | 50 | | | 65 | | | ns |
| $t_{pd}$ | Delay, Clock to Data Out | | | 170 | 300 | | 170 | 350 | ns |
| $C_{in}$ | Capacitance, Any Input (Note 2) | f = 1MHz, $V_{IN}$ = $V_{CC}$ | | 3 | 7 | | 3 | 7 | pF |

Note: 2. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.

## TIMING DIAGRAM



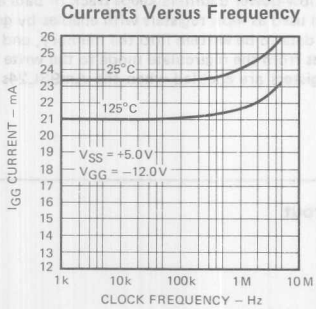

### KEY TO TIMING DIAGRAM

| WAVEFORM | INPUTS | OUTPUTS | WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|---|---|---|
| | MUST BE STEADY | WILL BE STEADY | | MAY CHANGE FROM L TO H | WILL BE CHANGING FROM L TO H |
| | MAY CHANGE FROM H TO L | WILL BE CHANGING FROM H TO L | | DON'T CARE; ANY CHANGE PERMITTED | CHANGING, STATE UNKNOWN |

MOS-406

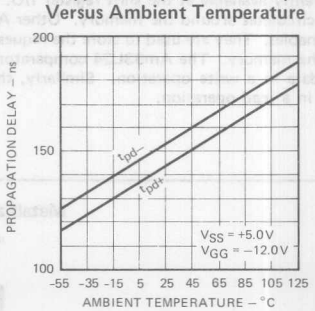
## CHARACTERISTIC CURVES

### Typical Power-Supply Currents Versus Frequency




MOS-407

### Typical Propagation Delay Versus Ambient Temperature

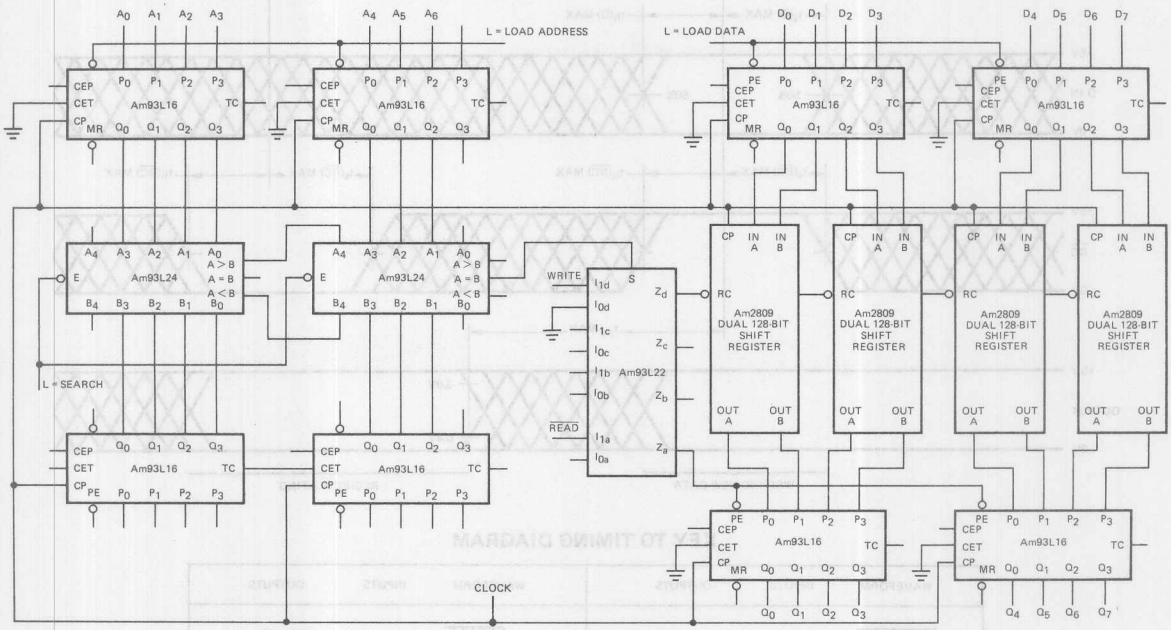



MOS-408

## DEFINITION OF TERMS

**STATIC SHIFT REGISTER** A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is LOW and is transferred to the static slaves while the clock is HIGH. The clock may be stopped indefinitely in the HIGH state, but there are limitations on the time it may reside in the LOW state.

**SET-UP and HOLD TIMES** The shift register will accept the data that is present on its input around the time the clock goes from LOW-to-HIGH. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

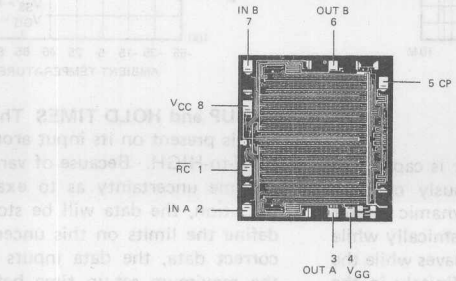



## 128-Word x 8-Bit Pseudo-Random Access Memory

Data stored in the four dual 128-bit shift registers can be accessed randomly by comparing the desired address with the address currently available at the shift register I/O. A pair of Am93L16 low-power counters keeps track of data addresses as the data circulates around the memory. Other Am93L16 counters are used as 4-bit registers with enables by grounding the count enables. They are used to store the requested address, the new data to be written into the memory, and the data read from the memory. The Am93L24 comparators switch the memories from the recirculate mode to the write mode to enter new data in a write operation. Similarly, the output storage registers are enabled when the Am93L24s indicate comparison in a read operation.

MOS-409

## Metallization and Pad Layout




86 X 95 Mils

# Am2810

## Dual 128-Bit Static Shift Register

### Distinctive Characteristics

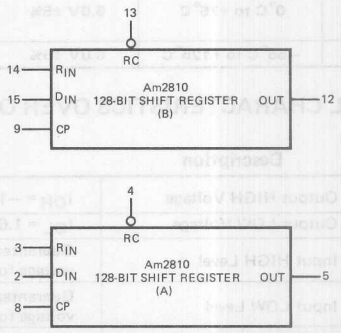
- 2nd Source to Mostek 1002P
- Built-in pull-up resistors
- 100% reliability assurance testing in compliance with MIL-STD-883
- Operation guaranteed from DC to 2MHz

### FUNCTIONAL DESCRIPTION

The Am2810 is a dual 128-bit static shift register built using P-channel silicon gate MOS technology. The two registers each have a two-input multiplexer on their inputs, so that input data may be selected from one of two sources. Each register has a separate clock input, and operates with a low-voltage TTL clock signal. The registers shift on the LOW-to-HIGH edge of the clock signal. Data at the inputs must be steady for a set-up time before and a hold time after this clock transition. Since data storage is static, the clock may be halted indefinitely in the HIGH state. The outputs of each register can drive one TTL load or three Am93L low-power TTL loads.

The two-input multiplexer on the input of each register is controlled by the RC (recirculate control) input. When RC is LOW, data is accepted on the $R_{in}$ input; when RC is HIGH, data is accepted on the $D_{in}$ input. The inputs to the registers have built-in pull-up resistors to provide total TTL compatibility. The $V_{RA}$ pin controls the pull-up resistors for register A $D_{in}$ and RC inputs. The $V_{RB}$ pin controls the pull-up resistors for the register B $D_{in}$ and RC inputs. The $V_{R\phi}$ pin controls the resistor on the clock input to both registers. When the resistor control pins are tied to $V_{GG}$ (−12V), the resistors are enabled and pull the inputs they affect up to $V_{SS}$. When the resistor control pins are tied to $V_{SS}$ the resistors are all very high impedance and the inputs they affect all exhibit normal MOS characteristics. The $R_{in}$ inputs are intended to be the recirculate inputs from an MOS output and these inputs do not have pull-up resistors associated with them.

### LOGIC SYMBOL

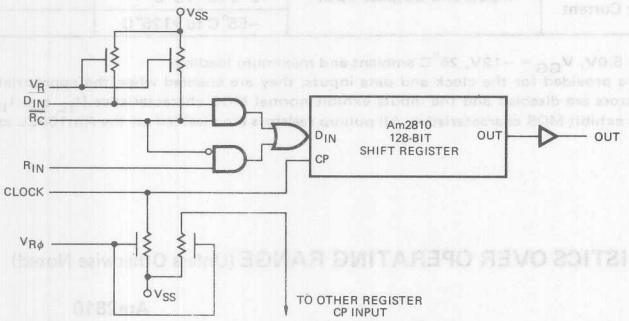



$V_{RA}$ = Pin 16
$V_{RB}$ = Pin 1
$V_{R\phi}$ = Pin 10

$V_{SS}$ = Pin 7
$V_{DD}$ = Pin 6
$V_{GG}$ = Pin 11

MOS-410

### LOGIC BLOCK DIAGRAM (One Register Shown)

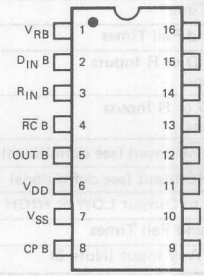



MOS-411

### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Molded DIP | 0°C to +75°C | AM2810PC |
| Hermetic DIP | 0°C to +75°C | AM2810DC |
| Hermetic DIP | −55°C to +125°C | AM2810DM |

### CONNECTION DIAGRAMS




Note: Pin 1 is marked for orientation.

MOS-412

## MAXIMUM RATING (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| $V_{DD}$ Supply Voltage | $V_{SS}$ −10V to $V_{SS}$ +0.3V |
| $V_{GG}$ Supply Voltage | $V_{SS}$ −20V to $V_{SS}$ +0.3V |
| DC Input Voltage | $V_{SS}$ −10V to $V_{SS}$ +0.3V |

## OPERATING RANGE

| Part Number | $T_A$ | $V_{SS}$ | $V_{DD}$ | $V_{GG}$ |
|---|---|---|---|---|
| Am2810XC<br>Am1002P<br>Am1002L | 0°C to +75°C | 5.0V ±5% | 0 V | −12.0V ±5% |
| Am2810XM | −55°C to +125°C | 5.0V ±5% | 0 V | −12.0V ±5% |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −100μA | | $V_{SS}$−1 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 1.6mA | | | 0.2 | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | $V_{SS}$−1 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | $V_{SS}$−4 | Volts |
| $I_{IL}$ (Note 2) | Resistors Disabled Input LOW Current | $V_{SS}$ = MAX., $V_{IN}$ = 0 V<br>$V_{RA}$ = $V_{RB}$ = $V_{R\phi}$ = $V_{SS}$ | | | | −40 | μA |
| $I_{IL}(\Omega)$ (Note 2) | Resistors Enabled Input LOW Current | $V_{SS}$ = MAX., $V_{IN}$ = 0.4V, Am2810/Am1002P only<br>$V_{RA}$ = $V_{RB}$ = $V_{R\phi}$ = $V_{GG}$ | | −0.3 | | −2.0 | mA |
| $I_{IL}(\phi)$ | Input LOW Current Clock Input | 1002L only | | −0.6 | | −4.0 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{RA}$ = $V_{RB}$ = $V_{R\phi}$ = $V_{IN}$ = $V_{SS}$ | | | | 40 | μA |
| $I_{SS}$ | $V_{SS}$ Power Supply Current | f = 1MHz<br>Inputs and Outputs Open | 0°C to +75°C | | 14 | 25 | mA |
| | | | −55°C to +125°C | | | 35 | |
| $I_{GG}$ | $V_{GG}$ Power Supply Current | | 0°C to +75°C | | −4 | −10 | |
| | | | −55°C to +125°C | | | −15 | |

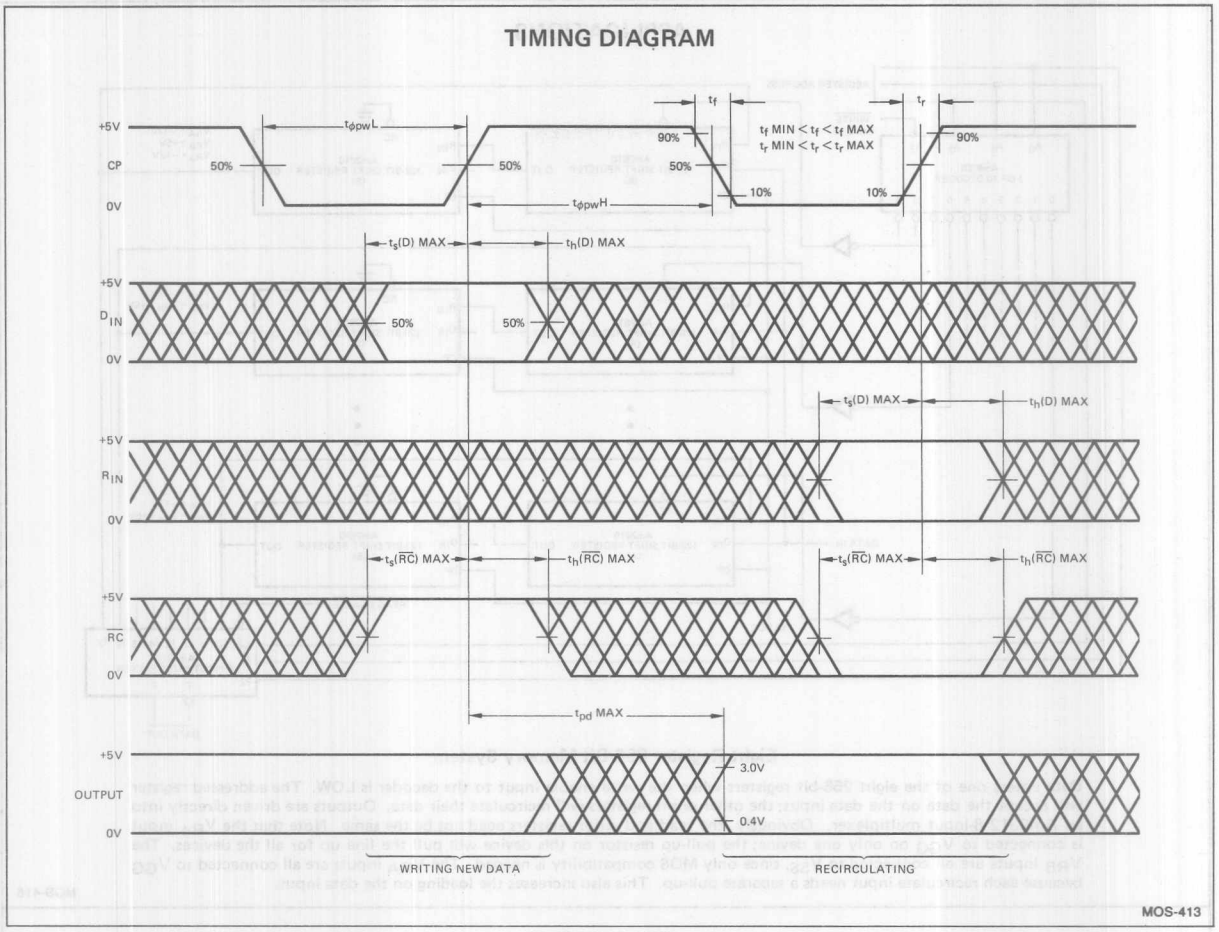
Notes: 1. Typical Limits are at $V_{SS}$ = 5.0V, $V_{GG}$ = −12V, 25°C ambient and maximum loading.
2. On chip pull-up resistors are provided for the clock and data inputs; they are enabled when the appropriate $V_R$ input is at −12V. When the $V_R$ inputs are at $V_{SS}$, the resistors are disabled and the inputs exhibit normal MOS characteristics ($I_{IL}$ and $I_{IH}$), the recirculate data inputs have no pull-up resistors and always exhibit MOS characteristics. All pull-up resistors are disabled on the Am1002L except the one on the clock.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | Am2810 Min. | Am2810 Typ. | Am2810 Max. | Am1002P/Am1002L Min. | Am1002P/Am1002L Typ. | Am1002P/Am1002L Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum Clock Frequency | | 2.0 | | | 1.0 | | | MHz |
| $t_{\phi pw}H$ | Clock HIGH Time | | 0.2 | | ∞ | 0.4 | | ∞ | μs |
| $t_{\phi pw}L$ | Clock LOW Time | | 0.2 | | 100 | 0.3 | | 10 | μs |
| $t_r$, $t_f$ | Clock Rise and Fall Times | | 10 | | 200 | 10 | | 200 | ns |
| $t_s$(D) | Set-up Time, D or R Inputs (see definitions) | $t_r$ = $t_f$ = 50ns, $V_R$ = −12V | 100 | | | 50 | | | ns |
| $t_h$(D) | Hold Time, D or R Inputs (see definitions) | $t_r$ = $t_f$ = 50ns, $V_R$ = −12V | 100 | | | 200 | | | ns |
| $t_s(\overline{RC})$ | Set-up Time, $\overline{RC}$ Input (see definitions) | | 100 | | | 100 | | | ns |
| $t_h(\overline{RC})$ | Hold Time, $\overline{RC}$ Input (see definitions) | | 200 | | | 300 | | | ns |
| $t_{pd}$ | Delay, Clock to Output LOW or HIGH | $R_L$ = 2.9kΩ, $C_L$ = 20pF | (Note 4) | | 250 | (Note 4) | | 450 | ns |
| $t_{pr}$, $t_{pf}$ | Output Rise and Fall Times | 10% to 90% | | | 100 | | | 150 | ns |
| $C_{in}$ | Capacitance, Any Input (Note 3) | f = 1MHz, $V_{IN}$ = $V_{SS}$ | | 3 | 7 | | 3 | 10 | pF |

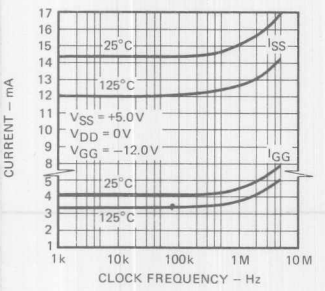
Notes: 3. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.
4. At any temperature, $t_{pd}$ min. is always much greater than $t_h$(D) max.

## TIMING DIAGRAM

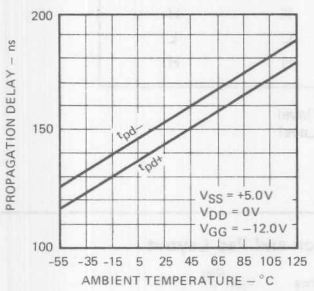



## TEST CIRCUIT

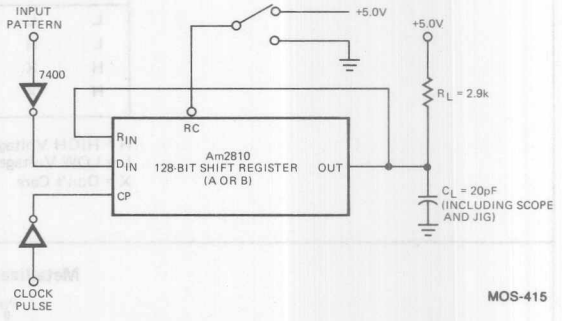
### Typical Power-Supply Currents Versus Frequency




### Typical Propagation Delay Versus Ambient Temperature




MOS-414

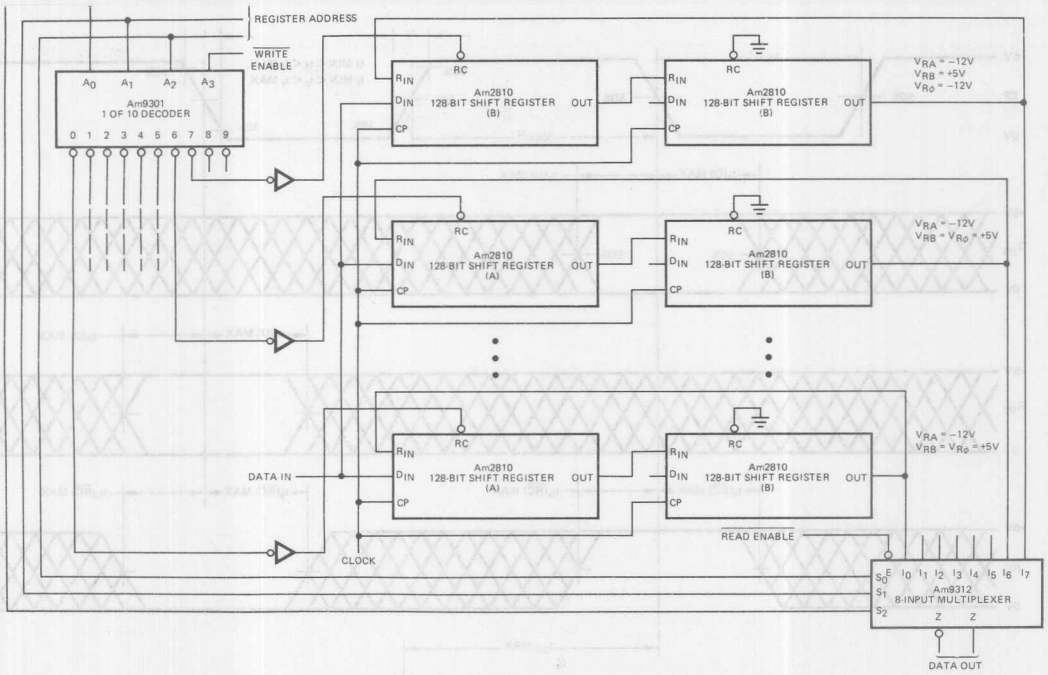



MOS-415

## DEFINITION OF TERMS

**STATIC SHIFT REGISTER** A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is LOW and is transferred to the static slaves while the clock is HIGH. The clock may be stopped indefinitely in the HIGH state, but there are limitations on the time it may reside in the LOW state.

**SET-UP and HOLD TIMES** The shift register will accept the data that is present on its input around the time the clock goes from LOW-to-HIGH. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.




**Eight Register 256-Bit Memory System**

Data enters one of the eight 256-bit registers when the write enable input to the decoder is LOW. The addressed register will accept the data on the data input; the other seven registers will recirculate their data. Outputs are driven directly into an Am9312 8-input multiplexer. Obviously, the read and write registers need not be the same. Note that the $V_{R\phi}$ input is connected to $V_{GG}$ on only one device; the pull-up resistor on this device will pull the line up for all the devices. The $V_{RB}$ inputs are all connected to $V_{SS}$, since only MOS compatibility is needed. The $V_{RA}$ inputs are all connected to $V_{GG}$ because each recirculate input needs a separate pull-up. This also increases the loading on the data input.

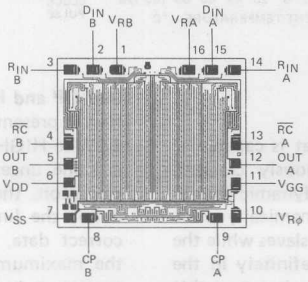
MOS-416

## TRUTH TABLE

| $\overline{RC}$ | $R_{IN}$ | $D_{IN}$ | Data Entered |
|---|---|---|---|
| L | L | X | L |
| L | H | X | H |
| H | X | L | L |
| H | X | H | H |

H = HIGH Voltage level
L = LOW Voltage Level
X = Don't Care

**Metallization and Pad Layout**




86 X 95 Mils

# Am2814/3114

## Dual 128-Bit Static Shift Register

### Distinctive Characteristics

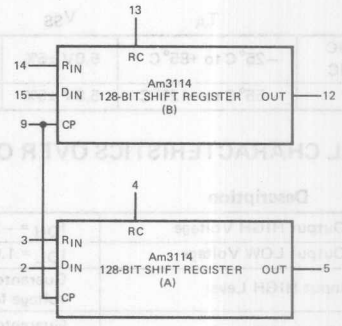
- 2nd Source to Texas Instruments 3114
- Operation guaranteed from DC to 2.5MHz.
- 100% reliability assurance testing in compliance with MIL-STD-883
- Full military grade devices available

### FUNCTIONAL DESCRIPTION

The Am3114 is a dual 128-bit static shift register built using P-channel silicon gate MOS technology. The two registers each have a two-input multiplexer on their inputs, so that input data may be selected from one of two sources. Both registers have a common clock input, and operate with a low-voltage TTL clock signal. The registers shift on the LOW-to-HIGH edge of the clock signal. Data at the inputs must be steady for a set-up time before and a hold time after this clock transition. Since data storage is static, the clock may be halted indefinitely in the HIGH state. The outputs of each register can drive one TTL load or three Am93L low-power TTL loads.

The two-input multiplexer on the input of each register is controlled by the RC (recirculate control) input. When RC is LOW, data is accepted on the $D_{in}$ input; when RC is HIGH, data is accepted on the $R_{in}$ input. The Am2814 is functionally identical to the Am3114, but is specified with higher performance.

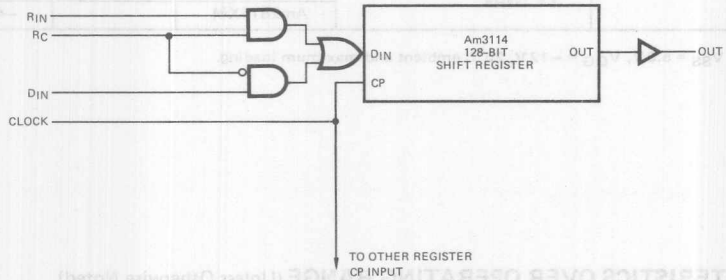
### LOGIC SYMBOL




$V_{SS}$ = Pin 7
$V_{DD}$ = Pin 6
$V_{GG}$ = Pin 11

MOS-417

### LOGIC BLOCK DIAGRAM (One Register Shown)

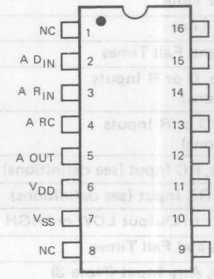



MOS-418

### ORDERING INFORMATION

| Package Type | Temperature Range | Am3114 Order Number | Am2814 Order Number |
|---|---|---|---|
| Molded DIP | −25°C to +85°C | TMS3114NC | AM2814PC |
| Hermetic DIP | −25°C to +85°C | TMS3114JC | AM2814DC |
| Hermetic DIP | −55°C to +125°C | | AM2814DM |

### CONNECTION DIAGRAM




Notes: 1. Pin 1 is marked for orientation.
2. NC = No Connection.

MOS-419

5

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| $V_{DD}$ Supply Voltage | $V_{SS}$ −10V to $V_{SS}$ +0.3V |
| $V_{GG}$ Supply Voltage | $V_{SS}$ −20V to $V_{SS}$ +0.3V |
| DC Input Voltage | $V_{SS}$ −15V to $V_{SS}$ +0.3V |

## OPERATING RANGE

| Part Number | $T_A$ | $V_{SS}$ | $V_{GG}$ | $V_{DD}$ |
|---|---|---|---|---|
| Am2814PC, DC<br>Am3114JC, NC | −25°C to +85°C | 5.0V ±5% | −11V to −13V | GND |
| Am2814DM | −55°C to +125°C | 5.0V ±5% | −11.4V to −12.6V | GND |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −200μA | | $V_{SS}$−1 | | | Volts |
| $V_{OH}$ | Output LOW Voltage | $I_{OL}$ = 1.6mA | | | 0.2 | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | Am3114 | 3.5 | | | Volts |
| | | | Am2814 | $V_{SS}$ −1.5 | | | |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | 0.6 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{SS}$ = MAX., $V_{IN}$ = 0.6V | | | | 0.5 | μA |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = $V_{SS}$ | | | | 0.5 | μA |
| $I_{SS}$ | $V_{SS}$ Power Supply Current | Inputs and Outputs Open f = 1MHz | Am3114 | | 15 | | mA |
| | | | Am2814XC | | 14 | 25 | |
| | | | Am2814XM | | 14 | 35 | |
| $I_{GG}$ | $V_{GG}$ Power Supply Current | Inputs and Outputs Open f = 1MHz | Am3114 | | −4 | | mA |
| | | | Am2814XC | | −4 | −10 | |
| | | | Am2814XM | | −4 | −15 | |

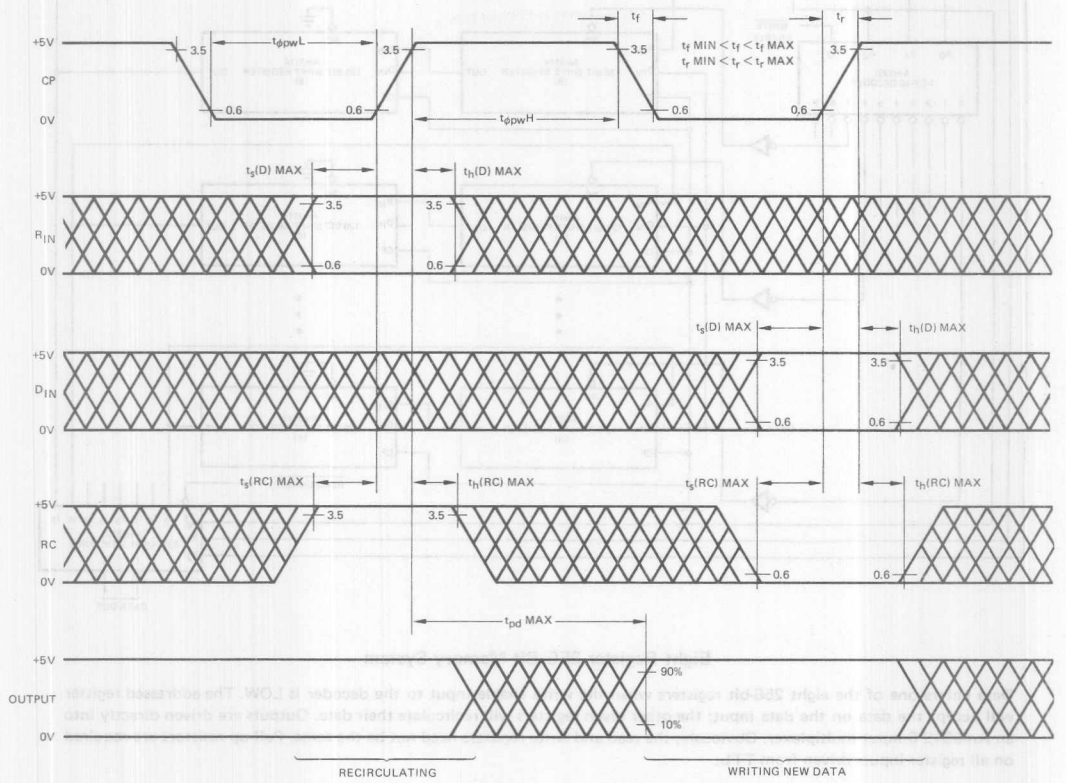
Note 1. Typical Limits are at $V_{SS}$ = 5.0V, $V_{GG}$ = −12V, 25°C ambient and maximum loading.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | Am3114 Min. | Am3114 Typ. | Am3114 Max. | Am2814 Min. | Am2814 Typ. | Am2814 Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum Clock Frequency | | 2.0 | | | 2.5 | | | MHz |
| $t_{\phi pw}H$ | Clock HIGH Time | | .330 | | ∞ | .200 | | ∞ | μs |
| $t_{\phi pw}L$ | Clock LOW Time | | .130 | | 100 | .170 | | 100 | μs |
| $t_r$, $t_f$ | Clock Rise and Fall Times | | | | 5 | | | 5 | μs |
| $t_s$(D) | Set-up Time, D or R Inputs (see definitions) | $t_r = t_f \leq 50$ns | 100 | | | 100 | | | ns |
| $t_h$(D) | Hold Time, D or R Inputs (see definitions) | | 100 | | | 100 | | | ns |
| $t_s$(RC) | Set-up Time, RC Input (see definitions) | | 100 | | | 100 | | | ns |
| $t_h$(RC) | Hold Time, RC Input (see definitions) | | 150 | | | 150 | | | ns |
| $t_{pd}$ | Delay, Clock to Output LOW or HIGH | $R_L$ = 2.7k, $C_L$ = 20pF | | | 350 | (Note 4) | | 250 | ns |
| $t_{pr}$, $t_{pF}$ | Output Rise and Fall Times | 10% to 90% | | | | | | 100 | ns |
| $C_{in}$ | Capacitance, Any Input (Note 3) | f = 1MHz, $V_{IN}$ = $V_{SS}$ | | | 13 | | 3 | 7 | pF |

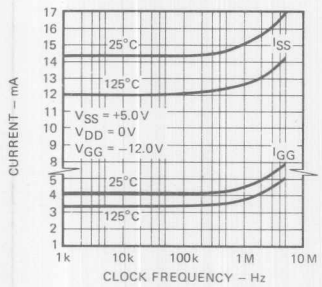
Notes: 3. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.
4. At any temperature, $t_{pd}$ min. is always much greater than $t_h$(D) max.

## TIMING DIAGRAM

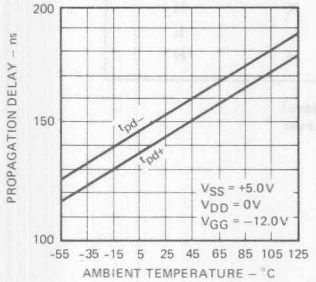



MOS-420

## Typical Power-Supply Currents Versus Frequency

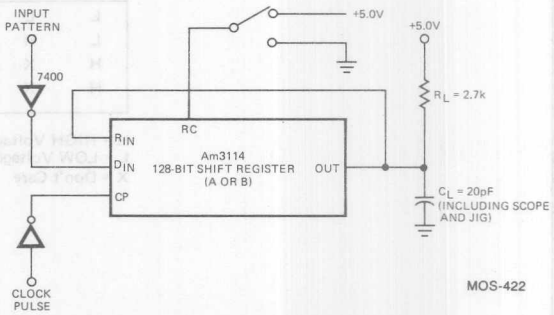



## Typical Propagation Delay Versus Ambient Temperature




MOS-421

## TEST CIRCUIT

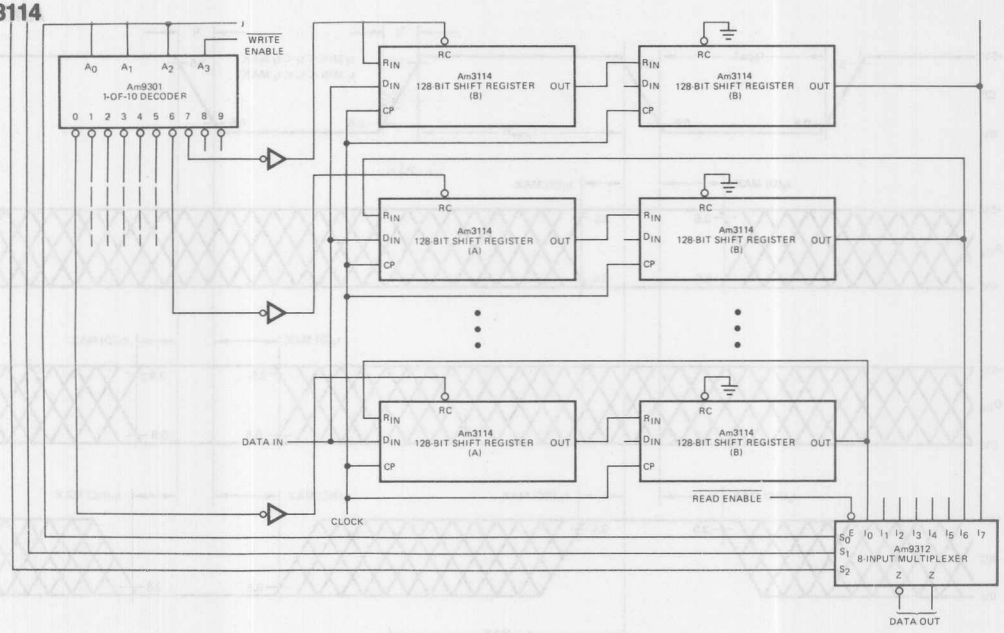



MOS-422

## DEFINITION OF TERMS

**STATIC SHIFT REGISTER** A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is LOW and is transferred to the static slaves while the clock is HIGH. The clock may be stopped indefinitely in the HIGH state, but there are limitations on the time it may reside in the LOW state.

**SET-UP and HOLD TIMES** The shift register will accept the data that is present on its input around the time the clock goes from LOW-to-HIGH. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.




**Eight Register 256-Bit Memory System**

Data enters one of the eight 256-bit registers when the write enable input to the decoder is LOW. The addressed register will accept the data on the data input; the other seven registers will recirculate their data. Outputs are driven directly into an Am9312 8-input multiplexer. Obviously, the read and write registers need not be the same. Pull-up resistors are required on all register inputs driven from TTL.

MOS-423

## TRUTH TABLE

| RC | $D_{IN}$ | $R_{IN}$ | Data Entered |
|---|---|---|---|
| L | L | X | L |
| L | H | X | H |
| H | X | L | L |
| H | X | H | H |

H = HIGH Voltage level
L = LOW Voltage Level
X = Don't Care

# Am2825 • Am2826 • Am2827

## 2048-Bit Dynamic Shift Registers

### Distinctive Characteristics

- 6 MHz data rate guaranteed
- Single 2048 and dual 1024-bit configurations
- Low power dissipation
- TTL compatible data inputs and outputs
- On chip recirculate and input select controls
- Plug-in replacement for National 5025/26/27
- Full military temperature range devices available
- 100% reliability assurance testing in compliance with MIL-STD-883

### FUNCTIONAL DESCRIPTION

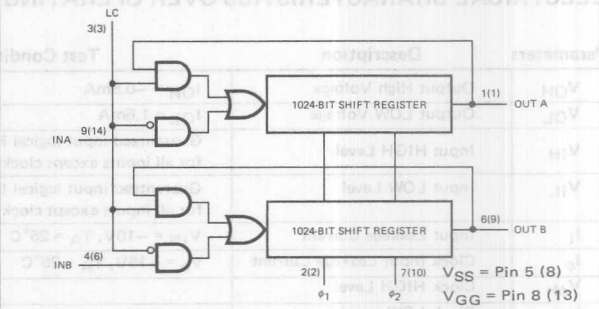
The Am2825/26/27 are military and commercial grade 2048-bit dynamic shift registers. The Am2825 is a dual 1024-bit device with on-chip recirculate and a load control (LC) common to both registers. When LC is HIGH, the two registers recirculate data; when LC is LOW new data is entered through the data inputs. The Am2826 is similar, but each register has two data inputs, selected by separate input select (IS) signals. The Am2827 is a single 2048-bit register with on-chip recirculate and a load control. All the devices can drive one standard TTL load or three Am93L series low-power TTL loads. The select, load command, and data inputs may be driven by TTL signals. Two high-voltage clock signals, $\phi 1$ and $\phi 2$, are required. Internally, each shift register consists of two multiplexed registers, so that a data shift occurs on each $\phi 1$ or $\phi 2$ clock pulse. The data rate, therefore, is double the frequency of either clock signal.

### ORDERING INFORMATION

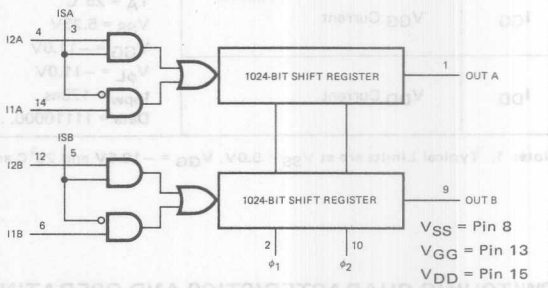
| Package Type | Temperature Range | Order Number |
|---|---|---|
| 10-Pin Molded | 0°C to +70°C | AM2825PC |
| 16-Pin Hermetic | 0°C to +70°C | AM2825DC |
| 16-Pin Hermetic | –55°C to +125°C | AM2825DM |
| 16-Pin Molded | 0°C to +70°C | AM2826PC |
| 16-Pin Hermetic | 0°C to +70°C | AM2826DC |
| 16-Pin Hermetic | –55°C to +125°C | AM2826DM |
| 8-Pin Molded | 0°C to +70°C | AM2827PC |
| 8-Pin Hermetic | –55°C to +125°C | AM2827DM |
| 8-Pin Hermetic | 0°C to +70°C | AM2827DC |

### LOGIC DIAGRAMS

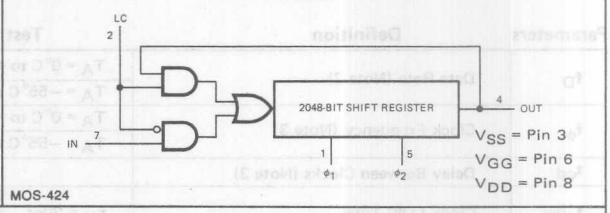
**Am2825**




**Am2826**



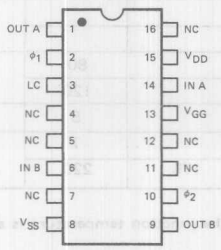

**Am2827**



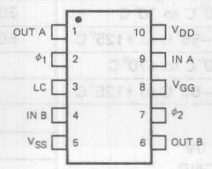

MOS-424

### CONNECTION DIAGRAMS
Top View

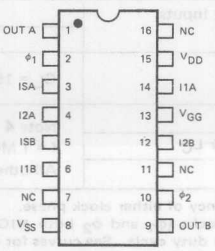
**Am2825**



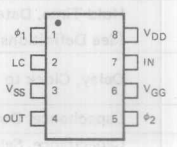

**Am2825**




**Am2826**




**Am2827**




MOS-425

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| DC Input Voltage with Respect to $V_{SS}$ | −20V to +0.3V |

## OPERATING RANGE

| Part Number | $V_{SS}$ | $V_{DD}$ | $V_{GG}$ | $T_A$ |
|---|---|---|---|---|
| AM2825/6/7DM | +5.0V ±5% | 0V | −10.0V to −11.0V | −55°C to +125°C |
| AM2825/6/7PC,DC | +5.0V ±5% | 0V | −10.0V to −11.0V | 0°C to +70°C |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = −0.5mA | | 2.4 | | $V_{SS}$ | Volts |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 1.6mA | | 0.0 | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs except clocks | | $V_{SS}$ −1.0 | | $V_{SS}$ +0.3 | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs except clocks | | $V_{SS}$ −10 | | $V_{SS}$ −4.2 | Volts |
| $I_I$ | Input Leakage Current | $V_{IN}$ = −10V, $T_A$ = 25°C | | | 10 | 500 | nA |
| $I_\phi$ | Clock Input Leakage Current | $V_\phi$ = −15V, $T_A$ = 25°C | | | 50 | 1000 | nA |
| $V_\phi H$ | Clock HIGH Level | | | $V_{SS}$ −1.0 | | $V_{SS}$ +0.3 | Volts |
| $V_\phi L$ | Clock LOW Level | | | $V_{GG}$ −0.3 | | $V_{GG}$ +0.8 | Volts |
| $I_{GG}$ | $V_{GG}$ Current | $T_A$ = 25°C<br>$V_{SS}$ = 5.25V<br>$V_{GG}$ = −11.0V<br>$V_{\phi L}$ = −11.0V<br>$t_{\phi pw}$ = 125ns<br>Data = 11110000... | .01MHz<$f_\phi$<0.1MHz | | 2.5 | 5 | mA |
| | | | $f_\phi$ = 1.0MHz | | 2.5 | 5 | |
| | | | $f_\phi$ = 3.0MHz | | 2.5 | 5 | |
| $I_{DD}$ | $V_{DD}$ Current | | .01MHz<$f_\phi$<0.1MHz | | 4 | 6 | mA |
| | | | $f_\phi$ = 1.0MHz | | 20 | 30 | |
| | | | $f_\phi$ = 3.0MHz | | 45 | 65 | |

Note: 1. Typical Limits are at $V_{SS}$ = 5.0V, $V_{GG}$ = −10.5V and 25°C ambient.

## SWITCHING CHARACTERISTICS AND OPERATING REQUIREMENTS OVER OPERATING RANGE

| Parameters | Definition | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $f_D$ | Data Rate (Note 2) | $T_A$ = 0°C to +70°C | | 0.02 | | 6.0 | MHz |
| | | $T_A$ = −55°C to +125°C | | 0.12 | | 4.0 | |
| $f_\phi$ | Clock Frequency (Note 3) | $T_A$ = 0°C to +70°C | | 0.01 | | 3.0 | |
| | | $T_A$ = −55°C to +125°C | | 0.06 | | 2.0 | |
| $t_\phi d$ | Delay Between Clocks (Note 3) | | | 10 | | Note 3 | ns |
| $t_\phi pw$ | Clock LOW Time | $t_{\phi t}$ = 20ns | 0°C to +70°C | 0.125 | | 10 | μs |
| | | | −55°C to +125°C | 0.180 | | 10 | |
| $t_\phi t$ | Clock Rise and Fall Times | 10% to 90% | | | | 0.5 | μs |
| $t_s$ | Set-Up Time, Data and Select Inputs (See Definitions) | | 0°C to 70°C | 40 | | | ns |
| | | | −55°C to +125°C | 60 | | | |
| $t_h$ | Hold Time, Data and Select Inputs (See Definitions) | | 0°C to 70°C | 30 | | | ns |
| | | | −55°C to +125°C | 50 | | | |
| $t_{pd}$ | Delay, Clock to Data Out | $C_L$ = 15pF | 0°C to +70°C | | | 80 | ns |
| | | | −55°C to +125°C | | | 120 | |
| $C_{(D)}$ | Capacitance, Data Input | Note 4<br>f = 1 MHz, $V_{IN}$ = 0V<br>All other pins at GND | | | | 5 | pF |
| $C_{(S)}$ | Capacitance, Select Input or $L_C$ | | | | | 7 | pF |
| $C_{(\phi)}$ | Capacitance, Clock Input | | | | 175 | 220 | |

Notes: 2. The Data Rate is twice the frequency of either clock phase.
3. The maximum delay between clocks ($\phi_1$ and $\phi_2$ both HIGH) is a function of junction temperature. The junction temperature is a function of ambient temperature and clock duty cycle. See curves for minimum frequency on page 3.
4. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.

## TRUTH TABLES

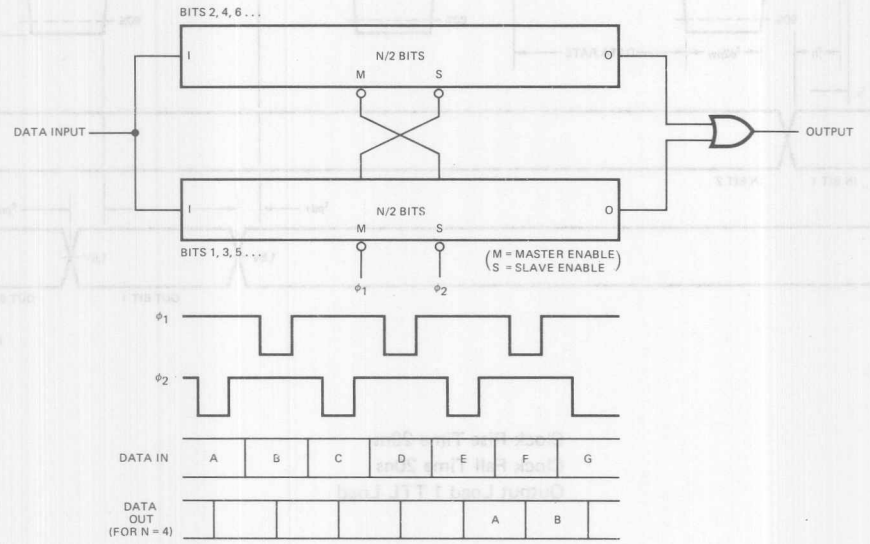
**Am2825 and Am2827**

| LC | IN | OUT | DATA ENTERED |
|---|---|---|---|
| L | L | X | L |
| L | H | X | H |
| H | X | L | L |
| H | X | H | H |

**Am2826**

| IS | INPUT 1 | INPUT 2 | DATA ENTERED |
|---|---|---|---|
| L | L | X | L |
| L | H | X | H |
| H | X | L | L |
| H | X | H | H |

## FUNCTIONAL EQUIVALENT OF EACH REGISTER




Since the two registers shift on opposite clock pulses, a new data bit is entered on both $\phi_1$ and $\phi_2$. Data entering the register on $\phi_1$ will appear at the output on $\phi_1$ (from the negative edge of $\phi_1$ to the negative edge of $\phi_2$).

MOS-426

## DEFINITION OF TERMS

**Dynamic Shift Register** A shift register in which data storage occurs on small capacitive nodes rather than in bistable logic circuits. Dynamic shift registers must be clocked continuously to maintain the charge stored on the nodes.

**$\phi_1$, $\phi_2$** The two clock pulses applied to the register. The clock is ON when it is at its negative voltage level and OFF when it is at $V_{SS}$. Data is accepted into the master of each bit during one phase and is transferred to the slave of each bit during the other phase.

**$t_{\phi d}$** Clock delay time. The time elapsing between the LOW-to-HIGH transition of one clock input and the HIGH-to-LOW transition of the other clock input. During $t_{\phi d}$ both clocks are HIGH and all data is stored on capacitive nodes.

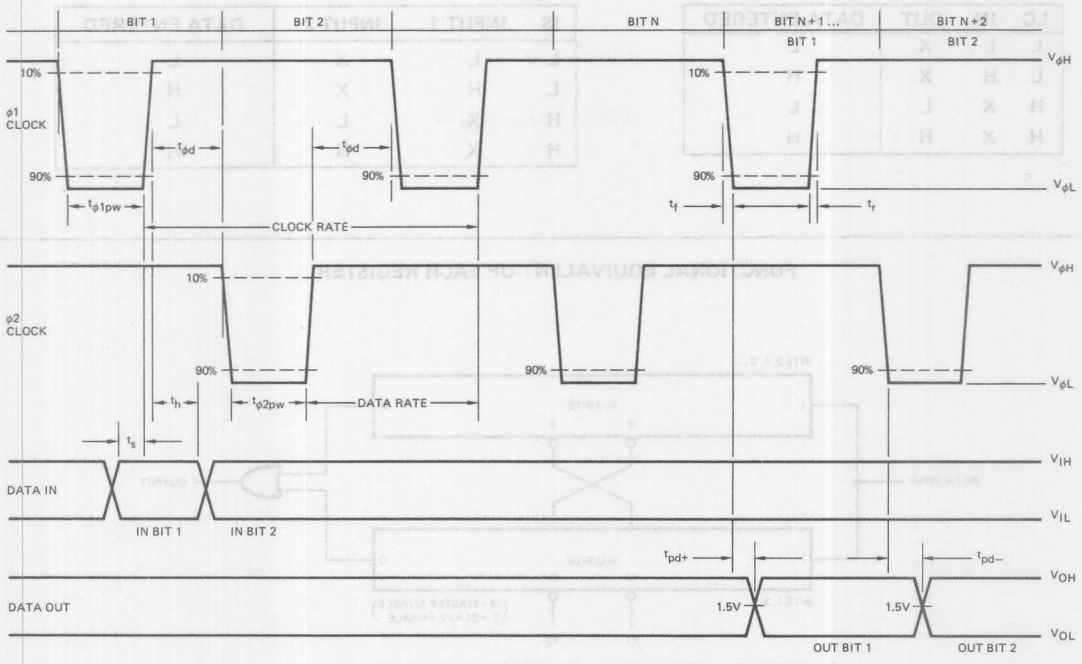
**$t_{\phi pw}$** Clock pulse width. The LOW time of each clock signal. During $t_{\phi pw}$ one of the clocks is ON, and data transfer between master and slave or slave and master occurs.

**$t_{\phi t}$** Clock rise and fall times. The time required for the clock signals to change from 10% to 90% of the total level change occuring.

**$t_s(D)$** Data set-up time. The time prior to the LOW-to-HIGH transition of $\phi$ during which the data on the data input must be steady to be correctly written into the memory.

**$t_h(D)$** Data hold time. The time following the LOW-to-HIGH transition of $\phi$ during which the data must be steady. To correctly write data into the register, the data must be applied by $t_s(D)$ before this transition and must not be changed until $t_h(D)$ after this transition.

**$t_{pd}$** The delay from a HIGH-to-LOW clock transition to correct data present at the register output.

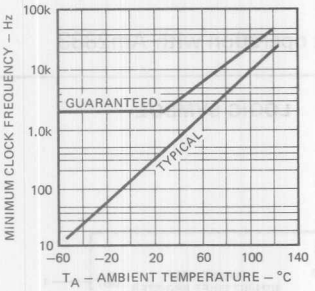



MOS-427

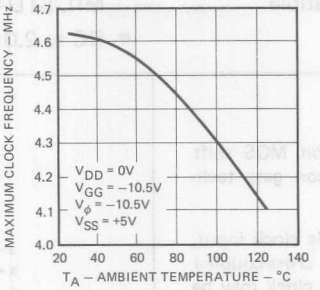
Clock Rise Time 20ns
Clock Fall Time 20ns
Output Load 1 TTL Load

## OPERATING CHARACTERISTICS

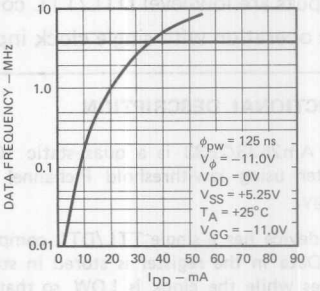
**Guaranteed Minimum Clock Frequency Versus Temperature**



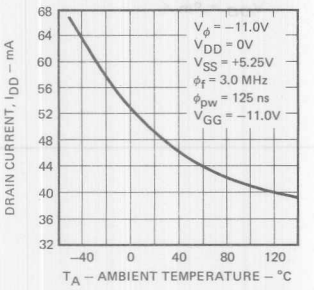

**Maximum Clock Frequency Versus Temperature**



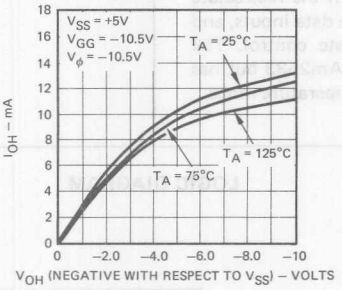

**Typical Power Supply Current Versus Data Rate**



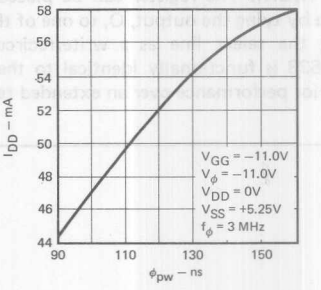

**Typical Power Supply Current Versus Temperature**




**$V_{OH}$ Versus $I_{OH}$**



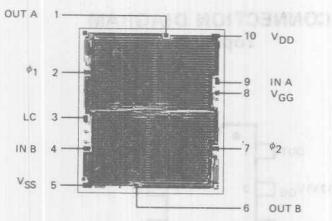

**Typical Power Supply Current Versus Clock Pulse Width $t_{\phi pw}$**




MOS-428

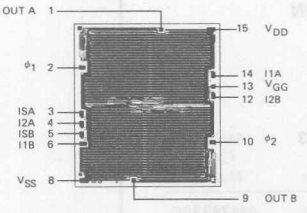
### Metallization and Pad Layouts

**Am2825**



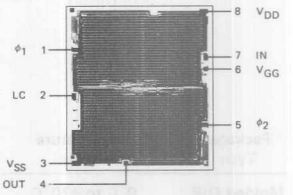

DIE SIZE 0.145" X 0.162"

**Am2826**




DIE SIZE 0.145" X 0.162"

**Am2827**




DIE SIZE 0.145" X 0.162"

# Am2833/2533

## 1024-Bit Static Shift Registers

### Distinctive Characteristics

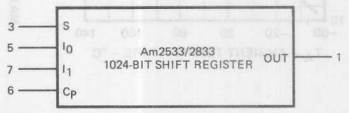
- Second source to Signetics 2533
- All inputs are low-level DTL/TTL compatible
- Static operation with single clock input.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- DC to 2.0MHz operation with Am2833

### FUNCTIONAL DESCRIPTION

The Am2533/2833 is a quasi-static 1024-bit MOS shift register using low-threshold P-channel silicon gate technology.

The device has a single TTL/DTL compatible clock input, Cp. Data in the register is stored in static, cross-coupled latches while the clock is LOW, so that the clock may be stopped indefinitely in the LOW state. When the clock shifts from LOW to HIGH to LOW a dynamic transfer of data occurs from one static latch to the next. The input of the register is a two-input multiplexer with both data inputs available. A select line, S, determines whether data will be accepted from the $I_0$ input (S = LOW) or the $I_1$ input (S = HIGH). The register can be placed in the recirculate mode by tying the output, O, to one of the data inputs, and using the select line as a write/recirculate control. The Am2833 is functionally identical to the Am2533 but has superior performance over an extended temperature range.

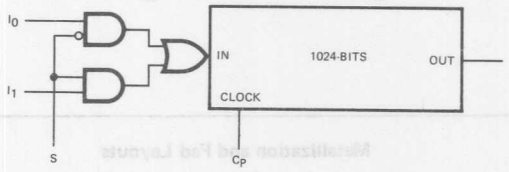
### LOGIC SYMBOL




$V_{CC}$ = Pin 8
$V_{GG}$ = Pin 2
$V_{DD}$ = Pin 4

MOS-429

### LOGIC DIAGRAM

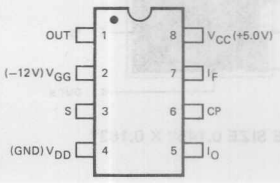



MOS-430

### ORDERING INFORMATION

| Package Type | Temperature Range | Am2533 Order Number | Am2833 Order Number |
|---|---|---|---|
| Molded DIP | 0°C to +70°C | AM2533V | AM2833PC |
| Hermetic DIP | 0°C to +70°C | AM2533DC | AM2833DC |
| Hermetic DIP | −55°C to +125°C | | AM2833DM |

### CONNECTION DIAGRAM
Top View




Note: Pin 1 marked for orientation

MOS-431

## MAXIMUM RATING (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| $V_{DD}$ Supply Voltage | $V_{CC}$ −20V to $V_{CC}$ +0.3V |
| $V_{GG}$ Supply Voltage | $V_{CC}$ −20V to $V_{CC}$ +0.3V |
| DC Input Voltage | $V_{CC}$ −20V to $V_{CC}$ +0.3V |

## OPERATING RANGE

| Part No. | Temperature | $V_{CC}$ | $V_{GG}$ | $V_{DD}$ |
|---|---|---|---|---|
| Am2833PC/Am2533PC Am2833DC/Am2533DC | 0°C to +70°C | 5.0V ±5% | −12V ±5% | 0V |
| Am2833DM | −55°C to +125°C | 5.0V ±5% | −12V ±5% | 0V |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −100μA | | 2.4 | 3.5 | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 1.6mA | | | 0.2 | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | $V_{CC}$ −1 (Note 3) | | $V_{CC}$+0.3 | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | $V_{GG}$ | | 0.8 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0V, $T_A$ = 25°C | | | 10 | 500 | nA |
| $I_{IH}$ | Input HIGH Current | $T_A$ = 25°C, $V_{IN}$ = $V_{CC}$ −1.0 (Note 3) | | −150 | −300 | | μA |
| $I_{IT}$ | Peak input transition current (Note 3) | 1.5 ≤ $V_{SS}$ − $V_{IN}$ ≤ 4.0, $T_A$ = 25°C | | | | −1.6 | mA |
| $V_{Imax}$ | Voltage at maximum input current | $T_A$ = 25°C | | $V_{SS}$−4.0 | $V_{SS}$−3.0 | $V_{SS}$−1.5 | V |
| $I_{CC}$ | $V_{CC}$ Power Supply Current | f = 1.5MHz | Am2533 | | 16 | 30 | mA |
| | | f = 2.0MHz | Am2833PC, DC | | 16 | 54 | |
| | | | Am2833DM | | 20 | 70 | |
| $I_{GG}$ | $V_{GG}$ Power Supply Current | f = 1.5MHz | Am2533 | | −5.0 | −7.5 | mA |
| | | f = 2.0MHz | Am2833PC, DC | | −5.0 | −14 | |
| | | | Am2833DM | | −7.0 | −18 | |

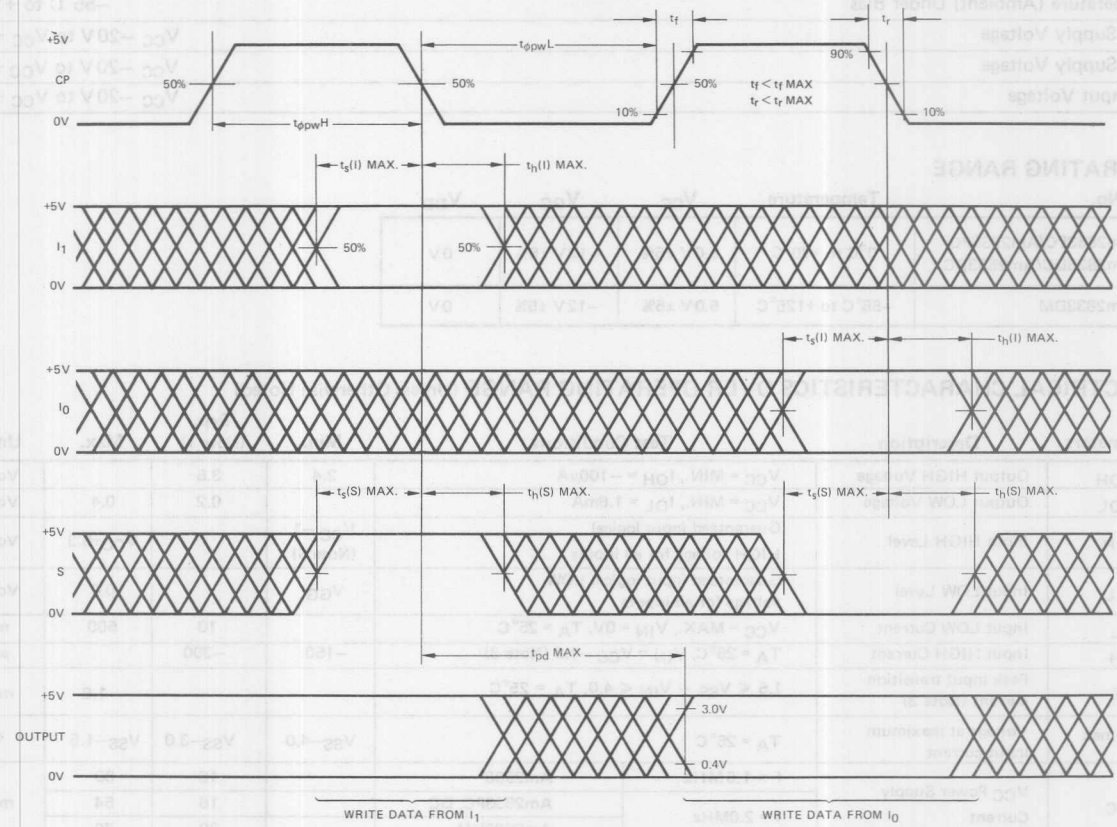
Notes:
1. Typical limits are at $V_{CC}$ = 5.0V, $V_{GG}$ = −12V, 25°C ambient.
2. Power supply currents are with inputs and outputs open.
3. A special input pull-up circuit becomes active at $V_{IN}$ = $V_{SS}$ −3.5V to pull the internal input node up to the MOS threshold. To return the internal node to the LOW state, current must be drawn from the MOS input. This current is maximum at approximately 2.0V.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | Am2533 Min. | Am2533 Typ. (Note 1) | Am2533 Max. | Am2833 Min. | Am2833 Typ. (Note 1) | Am2833 Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum Clock Frequency | | 1.5 | 2.0 | | 2.0 | 3.0 | | MHz |
| $t_{\phi pw}L$ | Clock LOW Time | | 0.250 | | ∞ | 0.200 | | ∞ | μs |
| $t_{\phi pw}H$ | Clock HIGH Time | | 0.350 | | 100 | 0.250 | | 100 | μs |
| $t_r$, $t_f$ | Clock Rise and Fall Times | | | | 1 | | | 1 | μs |
| $t_s(I)$ | Set-up Time, $I_0$ or $I_1$ Input (see definitions) | $t_r$ = $t_f$ ≤ 25ns | 50 | | | 50 | | | ns |
| $t_h(I)$ | Hold Time, $I_0$ or $I_1$ Input (see definitions) | | 50 | | | 50 | | | ns |
| $t_s(S)$ | Set-up Time, S Input (see definitions) | | 80 | | | 80 | | | ns |
| $t_h(S)$ | Hold Time, S Input (see definitions) | | 50 | | | 50 | | | ns |
| $t_{pd}$ | Delay, Clock to Output LOW or HIGH | $R_L$ = 2.9k, $C_L$ = 20pF | | | 300 | | | 300 | ns |
| $t_{pr}$, $t_{pf}$ | Output Rise and Fall Times | 10% to 90% | | | 150 | | | 150 | ns |
| $C_{in}$ | Capacitance, Any Input (Note 2) | f = 1MHz, $V_{IN}$ = $V_{CC}$ | | 3 | 5 | | 3 | 5 | pF |

Notes:
1. Typical limits are at $V_{CC}$ = 5.0V, $V_{GG}$ = −12.0V and $T_A$ = 25°C
2. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.

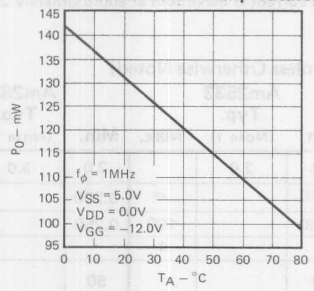
## TIMING DIAGRAM



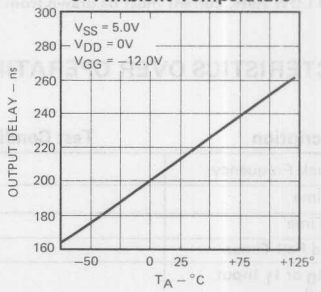

MOS-432

## TYPICAL PERFORMANCE CURVES

**Power Dissipation Versus Ambient Temperature**




**$t_{pd}$ as a Function of Ambient Temperature**



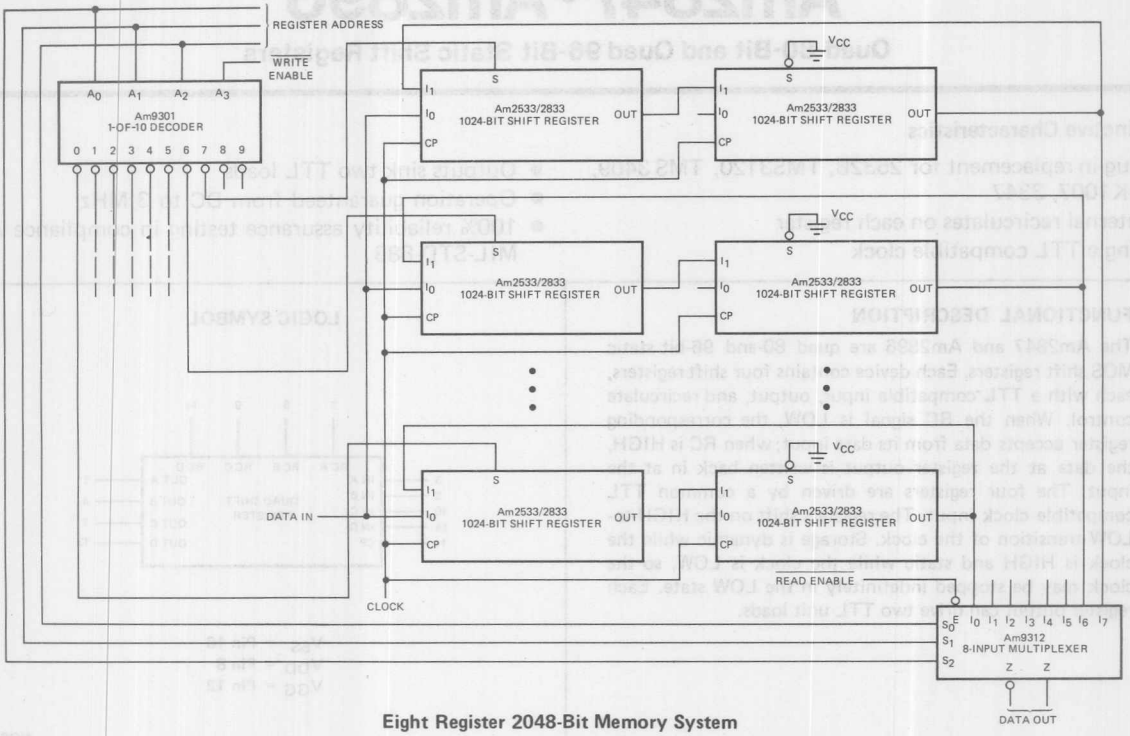

MOS-433

## DEFINITION OF TERMS

**STATIC SHIFT REGISTER** A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is HIGH and is transferred to the static slaves while the clock is LOW. The clock may be stopped indefinitely in the LOW state, but there are limitations on the time it may reside in the HIGH state.

**SET-UP and HOLD TIMES** The shift register will accept the data that is present on its input around the time the clock goes from HIGH-to-LOW. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

## APPLICATIONS




**Eight Register 2048-Bit Memory System**

Data enters one of the eight 2048-bit registers when the write enable input to the decoder is LOW. The addressed register will accept the data on the data input; the other seven registers will recirculate their data. Outputs are driven directly into an Am9312 8-input multiplexer. Obviously, the read and write registers need not be the same.

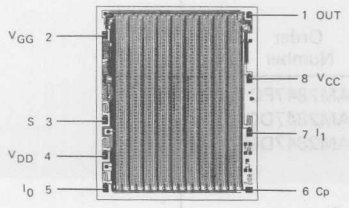
MOS-434

## TRUTH TABLE

| S | $I_0$ | $I_1$ | Data Entered |
|---|---|---|---|
| L | L | X | L |
| L | H | X | H |
| H | X | L | L |
| H | X | H | H |

H = HIGH Voltage level
L = LOW Voltage Level
X = Don't Care

## Metallization and Pad Layout




DIE SIZE: 0.133" X 0.163"

# Am2847 • Am2896

## Quad 80-Bit and Quad 96-Bit Static Shift Registers

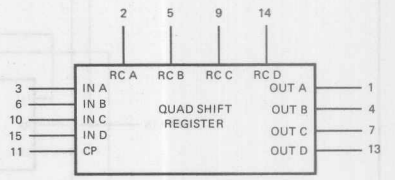
### Distinctive Characteristics

- Plug-in replacement for 2532B, TMS3120, TMS 3409, MK1007, 3347
- Internal recirculates on each register
- Single TTL compatible clock
- Outputs sink two TTL loads
- Operation guaranteed from DC to 3 MHz
- 100% reliability assurance testing in compliance with MIL-STD-883

### FUNCTIONAL DESCRIPTION

The Am2847 and Am2896 are quad 80-and 96-bit static MOS shift registers. Each device contains four shift registers, each with a TTL-compatible input, output, and recirculate control. When the RC signal is LOW, the corresponding register accepts data from its data input; when RC is HIGH, the data at the register output is written back in at the input. The four registers are driven by a common TTL compatible clock input. The registers shift on the HIGH-to-LOW transition of the clock. Storage is dynamic while the clock is HIGH and static while the clock is LOW, so the clock may be stopped indefinitely in the LOW state. Each register output can drive two TTL unit loads.

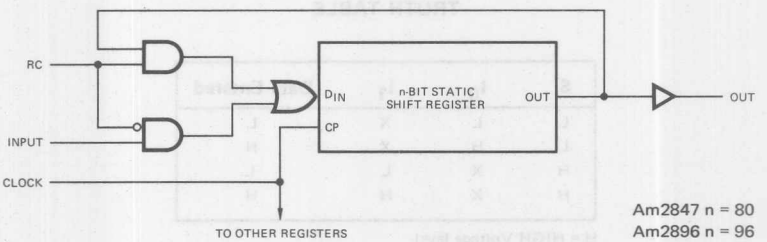
### LOGIC SYMBOL




$V_{SS}$ = Pin 16
$V_{DD}$ = Pin 8
$V_{GG}$ = Pin 12

MOS-435

### LOGIC BLOCK DIAGRAM
(One Register Shown)




Am2847 n = 80
Am2896 n = 96

MOS-436

### ORDERING INFORMATION

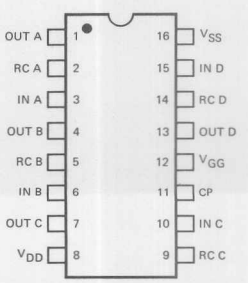
**Am2847 Quad 80-Bit**

| Package Type | Temperature Range | Order Number |
|---|---|---|
| 16-Pin Molded DIP | 0°C to +70°C | AM2847PC |
| 16-Pin Hermetic DIP | 0°C to +70°C | AM2847DC |
| 16-Pin Hermetic DIP | −55°C to +125°C | AM2847DM |

**Am2896 Quad 96-Bit**

| | | |
|---|---|---|
| 16-Pin Molded DIP | 0°C to +70°C | AM2896PC |
| 16-Pin Hermetic DIP | 0°C to +70°C | AM2896DC |
| 16-Pin Hermetic DIP | −55°C to +125°C | AM2896DM |

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

MOS-437

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +160°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| $V_{DD}$ Supply Voltage | $V_{SS}$ −10V to $V_{SS}$ +0.3V |
| $V_{GG}$ Supply Voltage | $V_{SS}$ −20V to $V_{SS}$ +0.3V |
| DC Input Voltage | $V_{SS}$ −20V to $V_{SS}$ +0.3V |

## OPERATING RANGE

| Part Number | Ambient Temperature | $V_{SS}$ | $V_{DD}$ | $V_{GG}$ |
|---|---|---|---|---|
| Am2847DM<br>Am2896DM | −55°C to +125°C | 5.0V ±5% | 0V | −12V ±5% |
| Am2847PC, DC<br>Am2896PC, DC | 0°C to +70°C | 5.0V ±5% | 0V | −12V ±5% |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −0.5mA | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 3.2mA | 0°C to 70°C | | | 0.4 | Volts |
| | | $I_{OL}$ = 2.4mA | −55° to 125°C | | | | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | $V_{SS}$ −1.0 | | $V_{SS}$ +0.3 | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | $V_{SS}$ −18.5 | | 0.8 | Volts |
| $I_{LI}$ | Input Leakage Current | $V_{IN}$ = −5.0V, all other pins connected to $V_{SS}$ | | | | 1.0 | μA |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0.4V | | | −1.0 | −1.6 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = $V_{SS}$ −1.0V | | −0.1 | | | mA |
| $I_{DD}$ | $V_{DD}$ Power Supply Current | Output open, f = 2.5MHz | 0°C to 70°C | | 25 | 35 | mA |
| | | | −55°C to 125°C | | | 45 | |
| $I_{GG}$ | $V_{GG}$ Power Supply Current | | 0°C to 70°C | | 10 | 15 | |
| | | | −55°C to 125°C | | | 20 | |

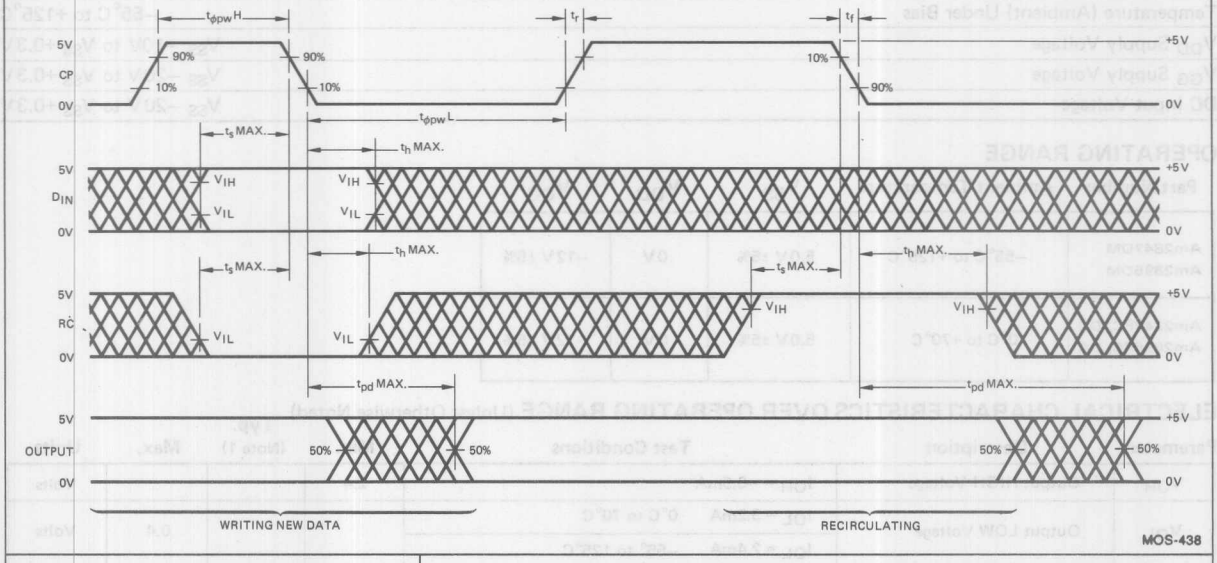
Note: 1. Typical Limits are at $V_{SS}$ = 5.0V, $V_{GG}$ = −12V, 25°C ambient.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| f | Clock Frequency | 0°C to 70°C | | 0 | | 3.0 | MHz |
| | | −55°C to 125°C | | | | 2.5 | |
| $t_{\phi pw}H$ | Clock HIGH Time | 0°C to 70°C | | .140 | | 100 | μs |
| | | −55°C to 125°C | | .150 | | 10 | |
| $t_{\phi pw}L$ | Clock LOW Time | 0°C to 70°C | | .140 | | ∞ | μs |
| | | −55°C to 125°C | | .180 | | | |
| $t_r$, $t_f$ | Clock Rise and Fall Times | | | 10 | | 200 | ns |
| $t_s$ | Set-Up Time, D or RC Inputs (see definitions) | $t_r$ = $t_f$ = 10ns | 0°C to 70°C | 120 | | | ns |
| | | | −55°C to 125°C | 120 | | | |
| $t_h$ | Hold Time, D or RC Inputs (see definitions) | $t_r$ = $t_f$ = 10ns | 0°C to 70°C | 40 | | | ns |
| | | | −55°C to 125°C | 60 | | | |
| $t_{pd}$ | Delay, Clock to Output LOW or HIGH | $R_L$ = 4k, $C_L$ = 10pF | 0°C to 70°C | (Note 3) | | 200 | ns |
| | | | −55°C to 125°C | | | 280 | |
| $C_{in}$ | Capacitance, Data Clock and RC Inputs (Note 2) | f = 1MHz, $V_{IN}$ = $V_{SS}$ | | | 3.0 | 7.0 | pF |
| $C_\phi$ | Capacitance, Clock Input (Note 2) | f = 1MHz, $V_{IN}$ = $V_{SS}$ | | | 3.0 | 7.0 | pF |

Notes: 2. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.
3. At any temperature, $t_{pd}$ min. is always much greater than $t_h$(D) max.

## TIMING DIAGRAM

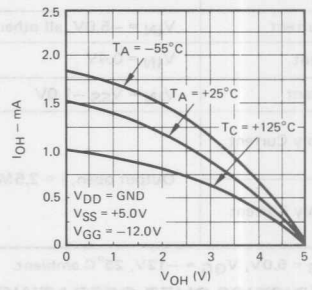



## KEY TO TIMING DIAGRAM

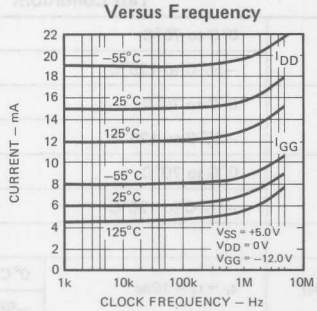
| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | MUST BE STEADY | WILL BE STEADY |
| | MAY CHANGE FROM H TO L | WILL BE CHANGING FROM H TO L |
| | MAY CHANGE FROM L TO H | WILL BE CHANGING FROM L TO H |
| | DON'T CARE: ANY CHANGE PERMITTED | CHANGING: STATE UNKNOWN |

## PERFORMANCE CURVES

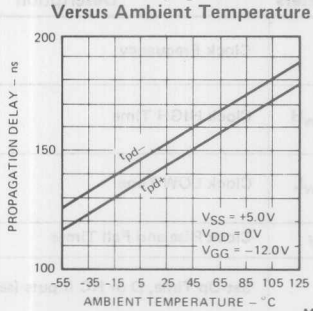
**Typical Data Output HIGH Current Versus Data Output Voltage**




**Typical Power-Supply Currents Versus Frequency**




**Typical Propagation Delay Versus Ambient Temperature**



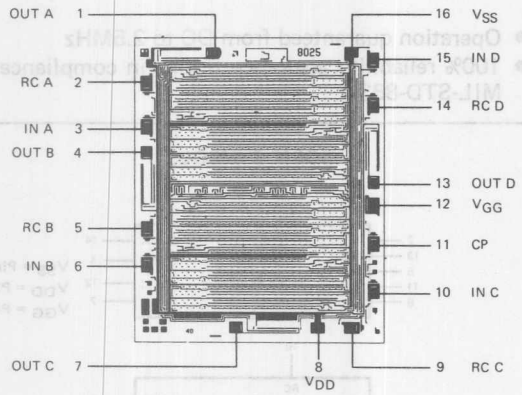

## DEFINITION OF TERMS

**STATIC SHIFT REGISTER** A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is HIGH and is transferred to the static slaves while the clock is LOW. The clock may be stopped indefinitely in the LOW state, but there are limitations on the time it may reside in the HIGH state.

**SET-UP and HOLD TIMES** The shift register will accept the data that is present on its input around the time the clock goes from HIGH-to-LOW. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

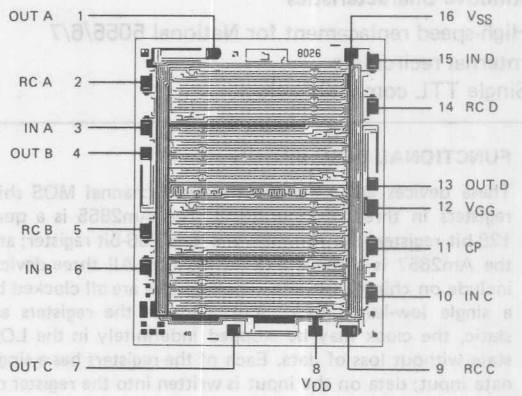
## Metallization and Pad Layouts

### Am2847




DIE SIZE 0.106" X 0.128"

### Am2896




DIE SIZE 0.106" X 0.128"

5

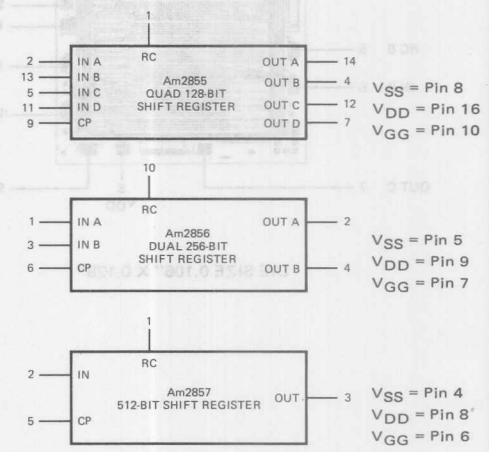
## Distinctive Characteristics

- High-speed replacement for National 5055/6/7
- Internal recirculate
- Single TTL compatible clock
- Operation quaranteed from DC to 2.5MHz
- 100% reliability assurance testing in compliance with MIL-STD-883

### FUNCTIONAL DESCRIPTION

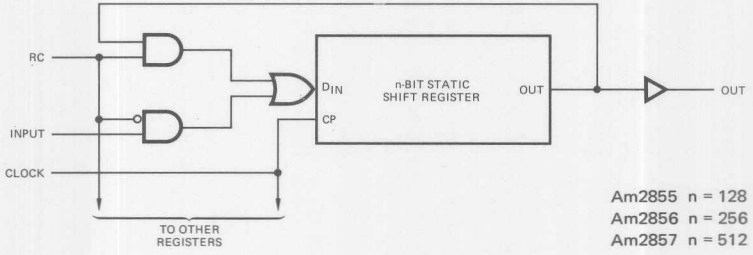
These devices are a family of static P-channel MOS shift registers in three configurations. The Am2855 is a quad 128-bit register; the Am2856 is a dual 256-bit register; and the Am2857 is a single 512-bit register. All three devices include on chip recirculate. The registers are all clocked by a single low-level clock input. Because the registers are static, the clock may be stopped indefinitely in the LOW state without loss of data. Each of the registers has a single data input; data on the input is written into the register on the HIGH-to-LOW clock edge. A single recirculate control (RC) on each chip determines whether the registers on that chip are to write data in from the data inputs or recirculate the data appearing on the output. If RC is LOW, new data is written in; if RC is HIGH then the data on the output will be written back into the register input on the next clock pulse.

### LOGIC SYMBOLS




MOS-440

### LOGIC BLOCK DIAGRAM
(One Register Shown)



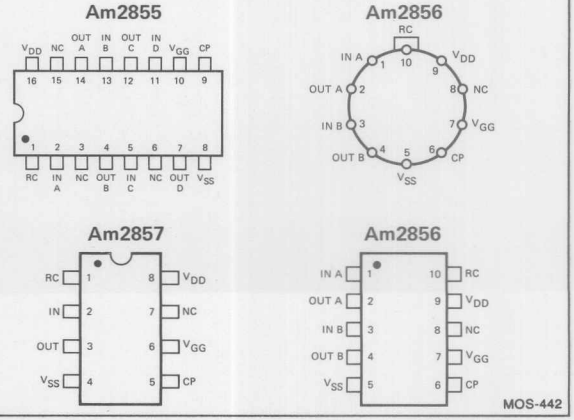

Am2855 n = 128
Am2856 n = 256
Am2857 n = 512

MOS-441

### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| 16-Pin Molded DIP | 0°C to +70°C | AM2855PC |
| 16-Pin Hermetic DIP | 0°C to +70°C | AM2855DC |
| 16-Pin Hermetic DIP | –55°C to +125°C | AM2855DM |
| 10-Pin Plastic DIP | 0°C to +70°C | AM2856PC |
| TO-100 Can | 0°C to +70°C | AM2856HC |
| TO-100 Can | –55°C to +125°C | AM2856HM |
| 8-Pin Molded DIP | 0°C to +70°C | AM2857PC |
| 8-Pin Hermetic DIP | 0°C to +70°C | AM2857DC |
| 8-Pin Hermetic DIP | –55°C to +125°C | AM2857DM |

### CONNECTION DIAGRAMS




MOS-442

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +160°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| $V_{DD}$ Supply Voltage | $V_{SS}$ −10V to $V_{SS}$ +0.3V |
| $V_{GG}$ Supply Voltage | $V_{SS}$ −20V to $V_{SS}$ +0.3V |
| DC Input Voltage | $V_{SS}$ −20V to $V_{SS}$ +0.3V |

## OPERATING RANGE

| Part Number | Ambient Temperature | $V_{SS}$ | $V_{DD}$ | $V_{GG}$ |
|---|---|---|---|---|
| Am2855DM<br>Am2856HM<br>Am2857DM | −55°C to +125°C | 5.0V ±5% | 0V | −12V ±5% |
| Am2855PC, DC<br>Am2856HC<br>Am2857PC, DC | 0°C to +70°C | 5.0V ±5% | 0V | −12V ±5% |

5

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −0.5mA | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 1.6mA | | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | $V_{SS}$ −1.0 | | $V_{SS}$ +0.3 | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | $V_{SS}$ −18.5 | | $V_{SS}$ −4.2 | Volts |
| $I_{IL}$ | Input Leakage Current | $V_{IN}$ = −10.0V, all other pins GND, $T_A$ = 25°C | | 0.01 | 0.5 | μA |
| $I_{DD}$ | $V_{DD}$ Power Supply Current | $T_A$ = 25°C, $t_{\phi pw}H$ = 160 ns, Data = 1010. . . , output open, f = 2.5 MHz | | 20.0 | 28.0 | mA |
| $I_{GG}$ | $V_{GG}$ Power Supply Current | | | 12.0 | 16.0 | mA |

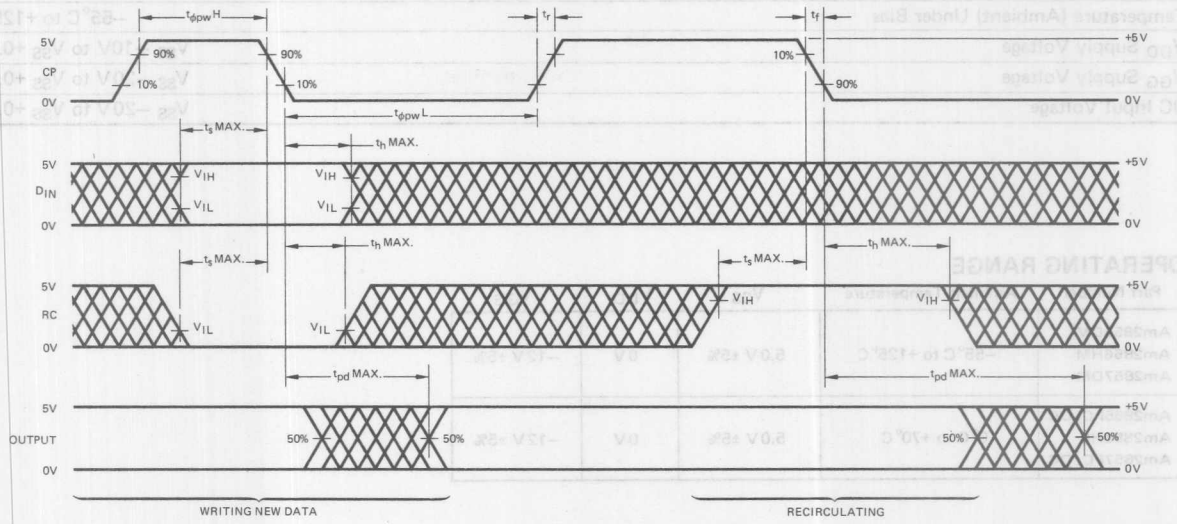
Note: 1. Typical Limits are at $V_{SS}$ = 5.0V, $V_{GG}$ = −12V, 25°C ambient and maximum loading.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| f | Clock Frequency | | 0 | | 2.5 | MHz |
| $t_{\phi pw}H$ | Clock HIGH Time | | 0.16 | | 10.0 | μs |
| $t_{\phi pw}L$ | Clock LOW Time | | 0.200 | | ∞ | μs |
| $t_r$, $t_f$ | Clock Rise and Fall Times | | 10 | | 200 | ns |
| $t_s$ | Set-up Time, D or RC Inputs (see definitions) | $t_r = t_f$ = 50ns | 100 | | | ns |
| $t_h$ | Hold Time, D or RC Inputs (see definitions) | $t_r = t_f$ = 50ns | 40 | | | ns |
| $t_{pd}$ | Delay, Clock to Output LOW or HIGH | $R_L$ = 4k, $C_L$ = 10pF | (Note 3) | 160 | 280 | ns |
| $C_{in}$ | Capacitance, Data In and RC Inputs (Note 2) | f = 1MHz, $V_{IN}$ = $V_{SS}$ | | 3 | 7 | pF |
| $C_\phi$ | Capacitance, Clock Input (Note 2) | f = 1MHz, $V_{IN}$ = $V_{SS}$ | | 3 | 7 | pF |

Notes: 2. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.
3. At any temperature, $t_{pd}$ min. is always much greater than $t_h$(D) max.

## TIMING DIAGRAM



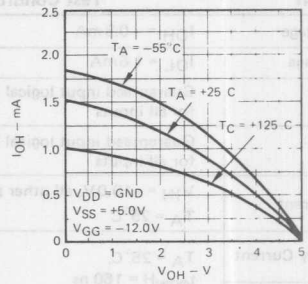

MOS-443

## KEY TO TIMING DIAGRAM

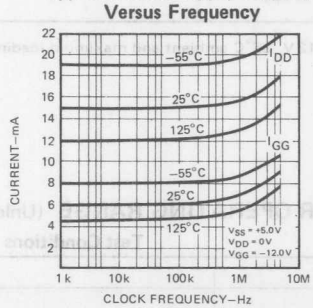
| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | MUST BE STEADY | WILL BE STEADY |
| | MAY CHANGE FROM H TO L | WILL BE CHANGING FROM H TO L |
| | MAY CHANGE FROM L TO H | WILL BE CHANGING FROM L TO H |
| | DON'T CARE: ANY CHANGE PERMITTED | CHANGING: STATE UNKNOWN |

## PERFORMANCE CURVES

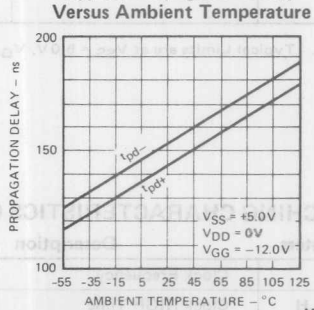
**Typical Data Output HIGH Current Versus Data Output Voltage**




**Typical Power-Supply Currents Versus Frequency**




**Typical Propagation Delay Versus Ambient Temperature**




MOS-444

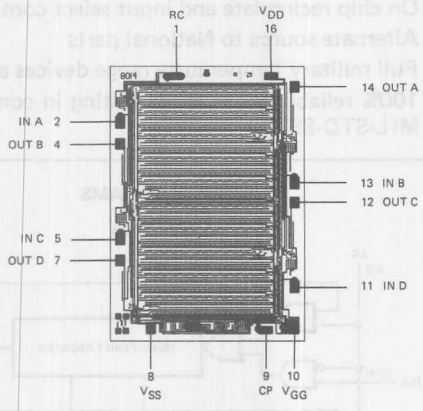
## DEFINITION OF TERMS

**STATIC SHIFT REGISTER** A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is HIGH and is transferred to the static slaves while the clock is LOW. The clock may be stopped indefinitely in the LOW state, but there are limitations on the time it may reside in the HIGH state.

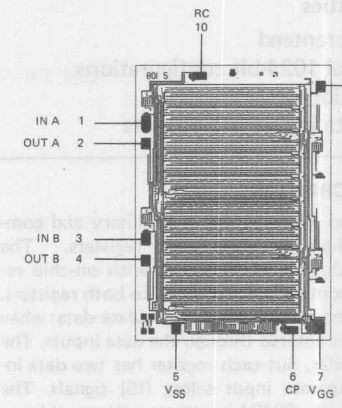
**SET-UP and HOLD TIMES** The shift register will accept the data that is present on its input around the time the clock goes from HIGH-to-LOW. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

## Metallization and Pad Layouts

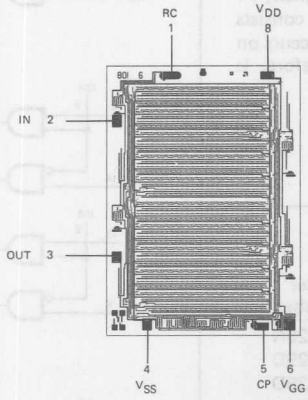
### Am2855




### Am2856




### Am2857




DIE SIZES: 0.101" X 0.142"

5

# Am4025/5025 • Am4026/5026 • Am4027/5027

## 2048-Bit Dynamic Shift Registers

**Distinctive Characteristics**

- 6 MHz data rate guaranteed
- Single 2048 and dual 1024-bit configurations
- Low power dissipation
- TTL compatible data inputs and outputs
- On chip recirculate and input select controls
- Alternate source to National parts
- Full military temperature range devices available
- 100% reliability assurance testing in compliance with MIL-STD-883

### FUNCTIONAL DESCRIPTION

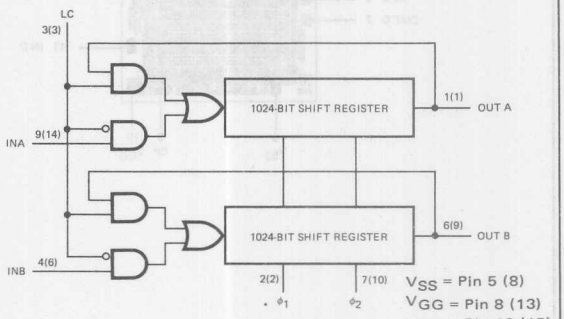
The Am4025/6/7 and Am5025/6/7 are military and commercial grade 2048-bit dynamic shift registers. The Am4025/5025 is a dual 1024-bit device with on-chip recirculate and a load control (LC) common to both registers. When LC is HIGH, the two registers recirculate data; when LC is LOW new data is entered through the data inputs. The Am4026/5026 is similar, but each register has two data inputs, selected by separate input select (IS) signals. The Am4027/5027 is a single 2048-bit register with on-chip recirculate and a load control. All the devices can drive one standard TTL load or three Am93L series low-power TTL loads. The select, load command, and data inputs may be driven by TTL signals. Two high-voltage clock signals, $\phi 1$ and $\phi 2$, are required. Internally, each shift register consists of two multiplexed registers, so that a data shift occurs on each $\phi 1$ or $\phi 2$ clock pulse. The data rate, therefore, is double the frequency of either clock signal.

### ORDERING INFORMATION

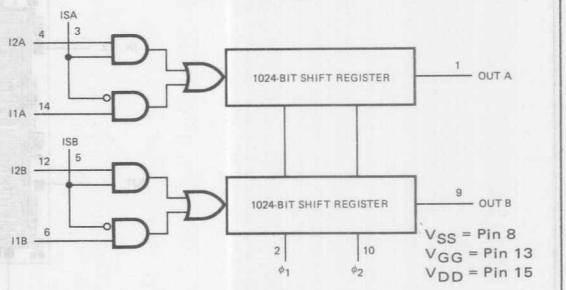
| Package Type | Temperature Range | Order Number |
|---|---|---|
| 10-Pin Molded | 0°C to +70°C | MM5025N |
| 16-Pin Hermetic | 0°C to +70°C | MM5025D |
| 16-Pin Hermetic | –55°C to +125°C | MM4025D |
| 16-Pin Molded | 0°C to +70°C | MM5026N |
| 16-Pin Hermetic | 0°C to +70°C | MM5026DC |
| 16-Pin Hermetic | –55°C to +125°C | MM4026D |
| 8-Pin Molded | 0°C to +70°C | MM5027N |
| 8-Pin Hermetic | 0°C to +70°C | AM5027DC |
| 8-Pin Hermetic | –55°C to +125°C | AM4027DM |

### LOGIC DIAGRAMS

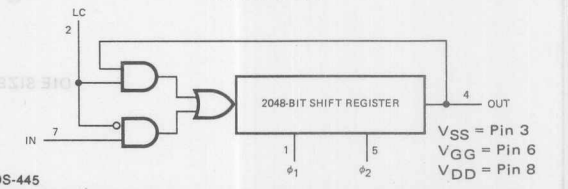
**Am4025/5025**




**Am4026/5026**



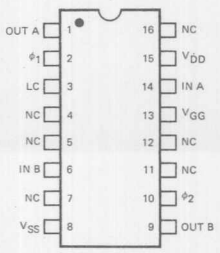

**Am4027/5027**



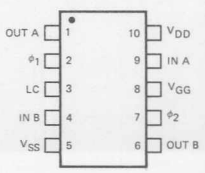

MOS-445

### CONNECTION DIAGRAMS
**Top Views**

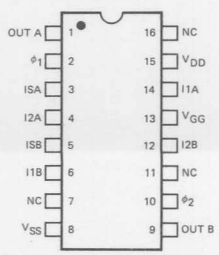
**MM4025D**



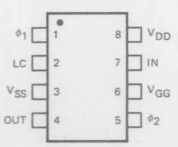

**MM5025N**




**MM4026/5026**




**MM4027/5027**




MOS-446

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| DC Input Voltage with Respect to $V_{CC}$ | −20V to +0.3V |

## OPERATING RANGE

| Part Number | $V_{SS}$ | $V_{DD}$ | $V_{GG}$ | $T_A$ |
|---|---|---|---|---|
| MM4025/6/7 | +5.0V ±5% | 0V | −12V ±10% | −55°C to +125°C |
| MM5025/6/7 | +5.0V ±5% | 0V | −12V ±10% | 0°C to +70°C |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = −0.5mA | | 2.4 | | $V_{SS}$ | Volts |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 1.6mA | | 0.0 | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs except clocks | | $V_{SS}$ −1.7 | | $V_{SS}$ +0.3 | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs except clocks | | $V_{SS}$ −10 | | $V_{SS}$ −4.2 | Volts |
| $I_I$ | Input Leakage Current | $V_{IN}$ = −10V, $T_A$ = 25°C | | | 10 | 500 | nA |
| $I_\phi$ | Clock Input Leakage Current | $V_\phi$ = −15V, $T_A$ = 25°C | | | 50 | 1000 | nA |
| $V_{\phi H}$ | Clock HIGH Level | | | $V_{SS}$ −1.0 | | $V_{SS}$ +0.3 | Volts |
| $V_{\phi L}$ | Clock LOW Level | | | $V_{SS}$ −18.5 | | $V_{SS}$ −14.5 | Volts |
| $I_{GG}$ | $V_{GG}$ Current | $T_A$ = 25°C, $V_{SS}$=5.0V, $V_{GG}$=−12.0V, $V_{\phi L}$ = −12.0V, t = 115ns, Data = 11110000... | .01MHz<f<0.1MHz | | 2 | 3.5 | mA |
| | | | f = 1.0MHz | | 2 | 3.5 | |
| | | | f = 3.0MHz | | 2 | 3.5 | |
| $I_{DD}$ | $V_{DD}$ Current | | .01MHz<f<0.1MHz | | 8 | 15 | mA |
| | | | f = 1.0MHz | | 22 | 32 | |
| | | | f = 3.0MHz | | 48 | 70 | |

Note: 1. Typical Limits are at $V_{SS}$ = 5.0V, $V_{GG}$ = −12.0V and 25°C ambient.

## SWITCHING CHARACTERISTICS AND OPERATING REQUIREMENTS OVER OPERATING RANGE

| Parameters | Definition | Test Conditions | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|
| $f_D$ | Data Rate (Note 2) | $T_A$ = 0°C to +70°C | 0.02 | | 6.0 | MHz |
| | | $T_A$ = −55°C to +125°C | 0.12 | | 2.0 | |
| $f_\phi$ | Clock Frequency (Note 3) | $T_A$ = 0°C to +70°C | .01 | | 3.0 | |
| | | $T_A$ = −55°C to +125°C | 0.06 | | 1.0 | |
| $t_{\phi d}$ | Delay Between Clocks (Note 3) | | 10 | | Note 3 | ns |
| $t_{\phi pw}$ | Clock LOW Time | $t_{\phi t}$ = 20ns | 0.115 | | 10 | µs |
| $t_{\phi t}$ | Clock Rise and Fall Times | 10% to 90% | | | 0.5 | µs |
| $t_s$ | Set-Up Time, Data and Select Inputs (See Definitions) | | | | 35 | ns |
| $t_h$ | Hold Time, Data and Select Inputs (See Definitions) | | 20 | | | ns |
| $t_{\phi p}$ | Period From Start of (Note 3) One Phase to Start of Other Phase | $T_A$ = 0°C to +70°C | 0.165 | | 100 | µs |
| | | $T_A$ = −55°C to +125°C | 0.165 | | 16.5 | |
| $t_{pd}$ | Delay, Clock to Data Out | $C_L$ = 15pF | | | 80 | ns |
| $C_{(D)}$ | Capacitance, Data Input | $V_{IN}$ = 0, f = 1MHz, All other pins GND (Note 4) | | | 5 | pF |
| $C_{(S)}$ | Capacitance, Select Input or $L_C$ | | | | 7 | pF |
| $C_{(\phi)}$ | Capacitance, Clock Input | $V_\phi$ = 0, f = 1MHz, All other pins GND | | 165 | 190 | |

Notes: 2. The Data Rate is twice the frequency of either clock phase.
3. The maximum delay between clocks ($\phi_1$ and $\phi_2$ both HIGH) is a function of junction temperature. The junction temperature is a function of ambient temperature and clock duty cycle. See curves for minimum frequency on page 3.
4. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.

## TRUTH TABLES

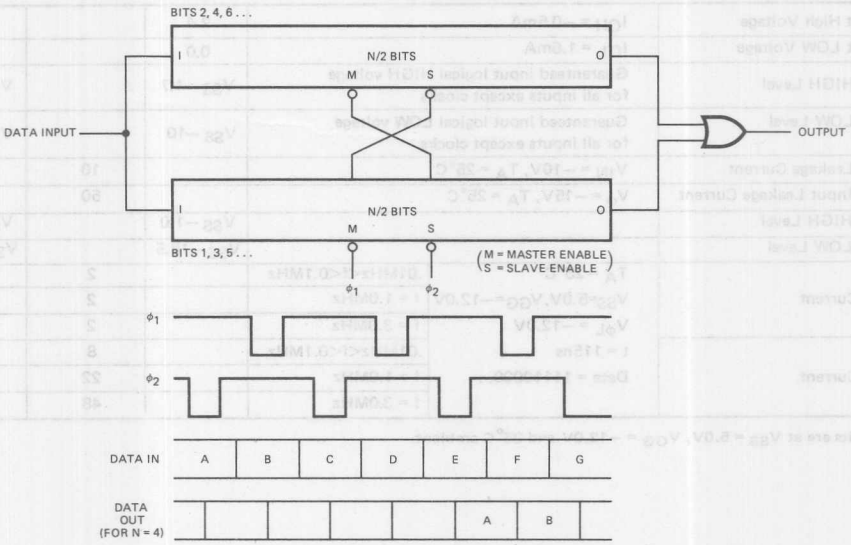
**Am4025/5025 and Am4027/5027**

| LC | IN | OUT | DATA ENTERED |
|---|---|---|---|
| L | L | X | L |
| L | H | X | H |
| H | X | L | L |
| H | X | H | H |

**Am4026/5026**

| IS | INPUT 1 | INPUT 2 | DATA ENTERED |
|---|---|---|---|
| L | L | X | L |
| L | H | X | H |
| H | X | L | L |
| H | X | H | H |

## FUNCTIONAL EQUIVALENT OF EACH REGISTER




Since the two registers shift on opposite clock pulses, a new data bit is entered on both $\phi_1$ and $\phi_2$. Data entering the register on $\phi_1$ will appear at the output on $\phi_1$ (from the negative edge of $\phi_1$ to the negative edge of $\phi_2$).

MOS-447

## DEFINITION OF TERMS

**Dynamic Shift Register** A shift register in which data storage occurs on small capacitive nodes rather than in bistable logic circuits. Dynamic shift registers must be clocked continuously to maintain the charge stored on the nodes.

**$\phi_1$, $\phi_2$** The two clock pulses applied to the register. The clock is ON when it is at its negative voltage level and OFF when it is at $V_{SS}$. Data is accepted into the master of each bit during one phase and is transferred to the slave of each bit during the other phase.

**$t_{\phi d}$** Clock delay time. The time elapsing between the LOW-to-HIGH transition of one clock input and the HIGH-toLOW transition of the other clock input. During $t_{\phi d}$ both clocks are HIGH and all data is stored on capacitive nodes.

**$t_{\phi pw}$** Clock pulse width. The LOW time of each clock signal. During $t_{\phi pw}$ one of the clocks is ON, and data transfer between master and slave or slave and master occurs.

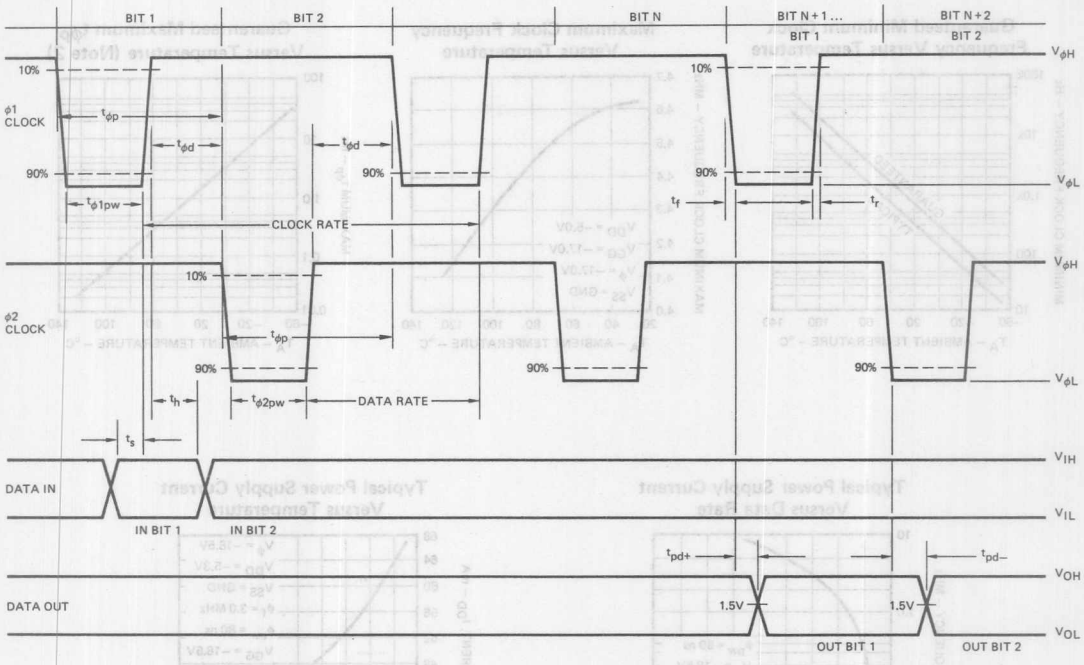
**$t_{\phi t}$** Clock rise and fall times. The time required for the clock signals to change from 10% to 90% of the total level change occuring.

**$t_s$(D)** Data set-up time. The time prior to the LOW-to-HIGH transition of $\phi$ during which the data on the data input must be steady to be correctly written into the memory.

**$t_h$(D)** Data hold time. The time following the LOW-to-HIGH transition of $\phi$ during which the data must be steady. To correctly write data into the register, the data must be applied by $t_s$(D) before this transition and must not be changed until $t_h$(D) after this transition.

**$t_{pd}$** The delay from a HIGH-to-LOW clock transition to correct data present at the register output.

## SWITCHING WAVEFORMS



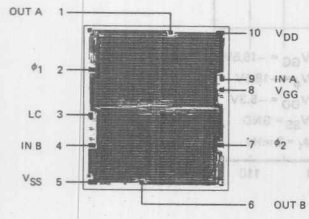

Clock Rise Time 20ns
Clock Fall Time 20ns
Output Load 1 TTL Load

MOS-448

5

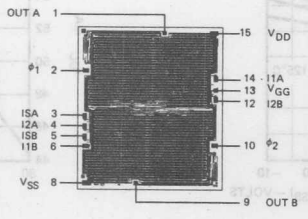
### Metallization and Pad Layouts

**Am4025/5025**



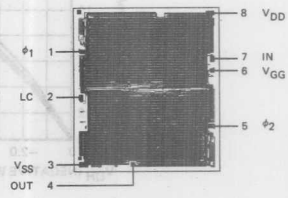

DIE SIZE 0.145" X 0.162"

**Am4026/5026**



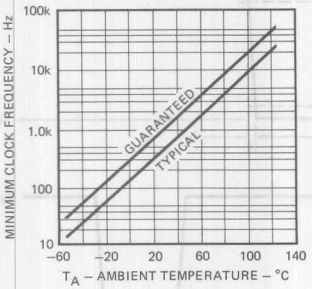

DIE SIZE 0.145" X 0.162"

**Am4027/5027**

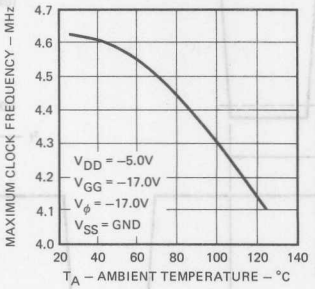



DIE SIZE 0.145" X 0.162"

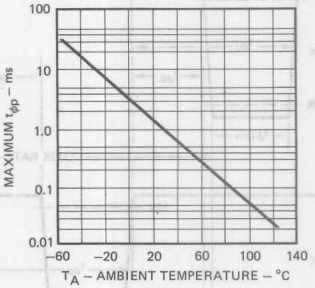
### Guaranteed Minimum Clock Frequency Versus Temperature



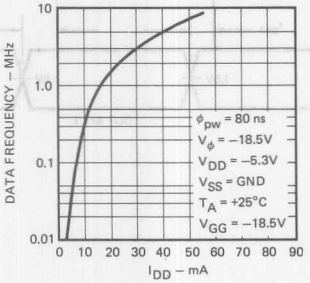

### Maximum Clock Frequency Versus Temperature



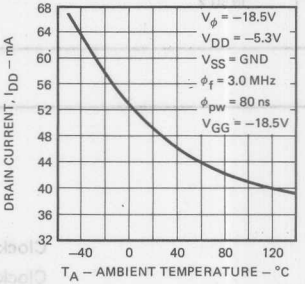

### Guaranteed Maximum $t_{\phi p}$ Versus Temperature (Note 2)



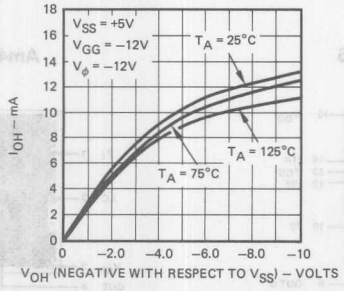

### Typical Power Supply Current Versus Data Rate



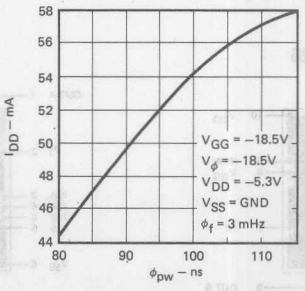

### Typical Power Supply Current Versus Temperature




### $V_{OH}$ Versus $I_{OH}$




### Typical Power Supply Current Versus Clock Pulse Width $t_{\phi pw}$




MOS-449

# Am4055/5055 • Am4056/5056 • Am4057/5057

## Quad 128-Bit, Dual 256-Bit and Single 512-Bit Static Shift Registers

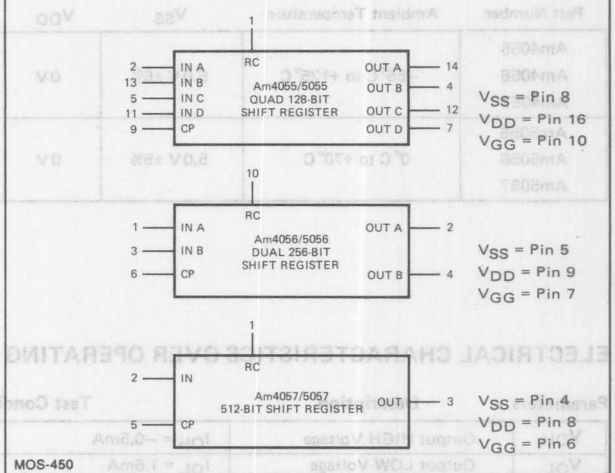
### Distinctive Characteristics

- Internal recirculate
- Single TTL compatible clock
- Operation guaranteed from DC to 1.5MHz
- 100% reliability assurance testing in compliance with MIL-STD-883

### FUNCTIONAL DESCRIPTION

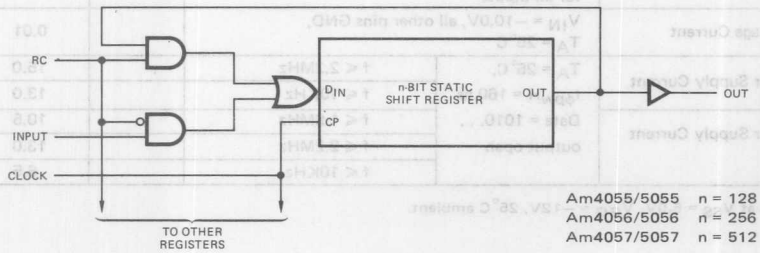
These devices are a family of static P-channel MOS shift registers in three configurations. The Am4055/5055 is a quad 128-bit register; the Am4056/5056 is a dual 256-bit register; and the Am4057/5057 is a single 512-bit register. All three devices include on chip recirculate. The registers are all clocked by a single low-level clock input. Because the registers are static, the clock may be stopped indefinitely in the LOW state without loss of data. Each of the registers has a single data input; data on the input is written into the register on the HIGH-to-LOW clock edge. A single recirculate control (RC) on each chip determines whether the registers on that chip are to write data in from the data inputs or recirculate the data appearing on the output. If RC is LOW, new data is written in; if RC is HIGH then the data on the output will be written back into the register input on the next clock pulse.

### LOGIC SYMBOLS




MOS-450

### LOGIC BLOCK DIAGRAM
(One Register Shown)




Am4055/5055 n = 128
Am4056/5056 n = 256
Am4057/5057 n = 512

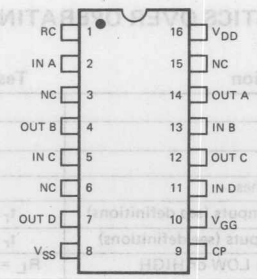
MOS-451

### ORDERING INFORMATION

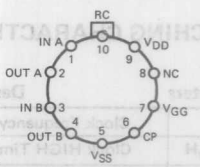
| Package Type | Temperature Range | Order Number |
|---|---|---|
| 16-Pin Molded DIP | 0°C to +70°C | MM5055N |
| 16-Pin Hermetic DIP | 0°C to +70°C | MM5055D |
| 16-Pin Hermetic DIP | –55°C to +125°C | MM4055D |
| TO-100 Can | 0°C to +70°C | MM5056H |
| TO-100 Can | –55°C to +125°C | MM4056H |
| 8-Pin Molded DIP | 0°C to +70°C | MM5057N |
| 8-Pin Hermetic DIP | 0°C to +70°C | MM5057D |
| 8-Pin Hermetic DIP | –55°C to +125°C | MM4057D |

### CONNECTION DIAGRAMS

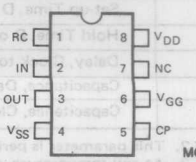
Am4055/5055




Am4056/5056




Am4057/5057




MOS-452

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +160°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| $V_{DD}$ Supply Voltage | $V_{SS}$ −10V to $V_{SS}$ +0.3V |
| $V_{GG}$ Supply Voltage | $V_{SS}$ −20V to $V_{SS}$ +0.3V |
| DC Input Voltage | $V_{SS}$ −20V to $V_{SS}$ +0.3V |

## OPERATING RANGE

| Part Number | Ambient Temperature | $V_{SS}$ | $V_{DD}$ | $V_{GG}$ |
|---|---|---|---|---|
| Am4055<br>Am4056<br>Am4057 | −55°C to +125°C | 5.0V ±5% | 0V | −12V ±5% |
| Am5055<br>Am5056<br>Am5057 | 0°C to +70°C | 5.0V ±5% | 0V | −12V ±5% |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −0.5mA | | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 1.6mA | | | | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 4055/6/7 | $V_{SS}$−1.0 | | $V_{SS}$+0.3 | Volts |
| | | | | 5055/6/7 | $V_{SS}$−1.5 | | $V_{SS}$+0.3 | |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | $V_{SS}$−18.5 | | $V_{SS}$−4.2 | Volts |
| $I_{IL}$ | Input Leakage Current | $V_{IN}$ = −10.0V, all other pins GND, $T_A$ = 25°C | | | | 0.01 | 0.5 | µA |
| $I_{DD}$ | $V_{DD}$ Power Supply Current | $T_A$ = 25°C, $t_{\phi pw}H$ = 160 ns Data = 1010... output open | f ≤ 2.2MHz | | | 15.0 | 20.0 | mA |
| | | | f ≤ 10KHz | | | 13.0 | 18.0 | |
| $I_{GG}$ | $V_{GG}$ Power Supply Current | | f ≤ 1.6MHz | | | 10.5 | 15.5 | |
| | | | f ≤ 2.2MHz | | | 13.0 | 19.0 | |
| | | | f ≤ 10KHz | | | 6.5 | 9.0 | |

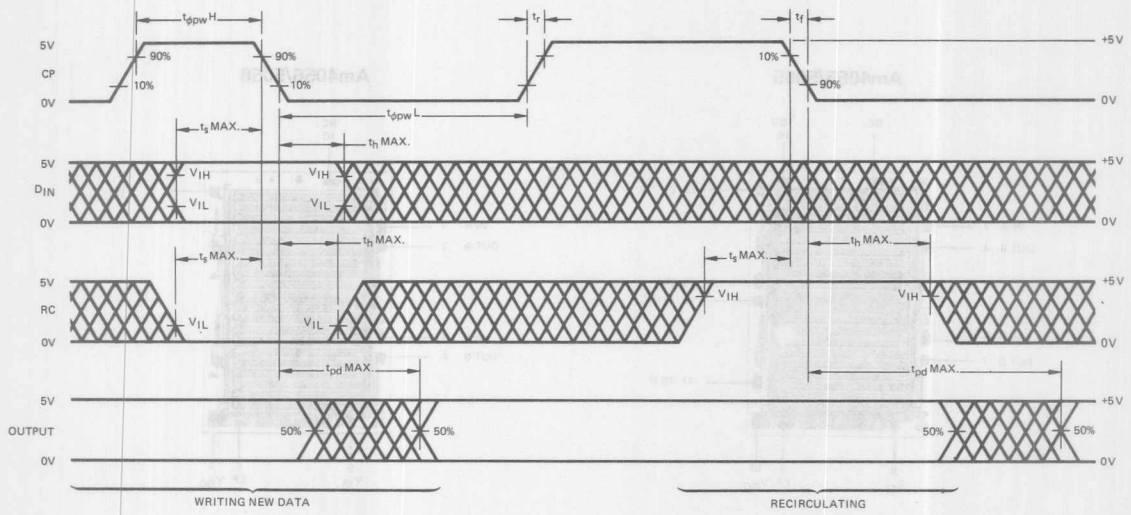
Note: 1. Typical Limits are at $V_{SS}$ = 5.0V, $V_{GG}$ = −12V, 25°C ambient.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | Am4055/6/7 Min. | Am4055/6/7 Typ. | Am4055/6/7 Max. | Am5055/6/7 Min. | Am5055/6/7 Typ. | Am5055/6/7 Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| f | Clock Frequency | | 0 | | 1.0 | 0 | | 1.5 | MHz |
| $t_{\phi pw}H$ | Clock HIGH Time | | 0.4 | | 1.0 | 0.23 | | 100 | µs |
| $t_{\phi pw}L$ | Clock LOW Time | | 0.4 | | ∞ | 0.3 | | ∞ | µs |
| $t_r$, $t_f$ | Clock Rise and Fall Times | | | | 200 | | | 200 | ns |
| $t_s$ | Set-up Time, D or RC Inputs (see definitions) | $t_r = t_f \leq$ 10ns | 260 | | | 110 | | | ns |
| $t_h$ | Hold Time, D or RC Inputs (see definitions) | $t_r = t_f \leq$ 10ns | 120 | | | 40 | | | ns |
| $t_{pd}$ | Delay, Clock to Output LOW or HIGH | $R_L$ = 4k, $C_L$ = 10pF | | 350 | 700 | | 250 | 345 | ns |
| $C_{in}$ | Capacitance, Data and RC Inputs (Note 2) | f = 1MHz, $V_{IN} = V_{SS}$ | | 4 | 7 | | 4 | 7 | pF |
| $C_\phi$ | Capacitance, Clock Input (Note 2) | f = 1MHz, $V_{IN} = V_{SS}$ | | | 14 | | | 14 | pF |

Notes: 2. This parameter is periodically sampled but not 100% tested. It is guaranteed by design.
3. At any temperature, $t_{pd}$ min. is always much greater than $t_h$ (D) max.

## TIMING DIAGRAM




MOS-453

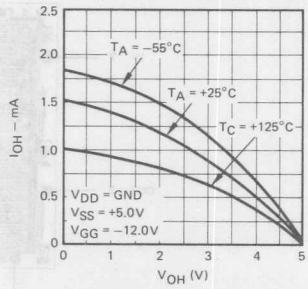
5

## KEY TO TIMING DIAGRAM

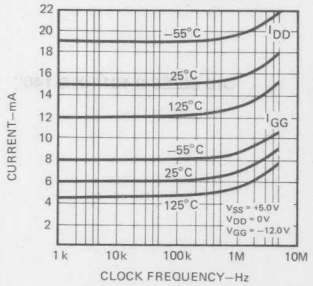
| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| ——— | MUST BE STEADY | WILL BE STEADY |
| ▨ | MAY CHANGE FROM H TO L | WILL BE CHANGING FROM H TO L |
| ▨ | MAY CHANGE FROM L TO H | WILL BE CHANGING FROM L TO H |
| ▨ | DON'T CARE; ANY CHANGE PERMITTED | CHANGING, STATE UNKNOWN |

## PERFORMANCE CURVES

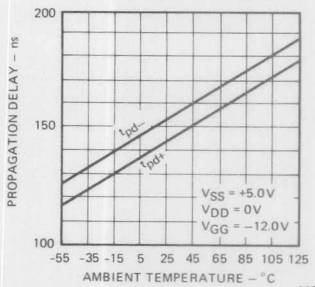
**Typical Data Output HIGH Current Versus Data Output Voltage**




**Typical Power-Supply Currents Versus Frequency**




**Typical Propagation Delay Versus Ambient Temperature**



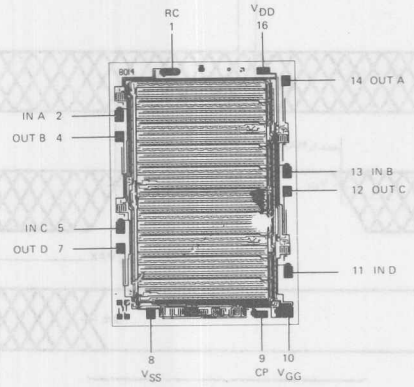

MOS-454

## DEFINITION OF TERMS

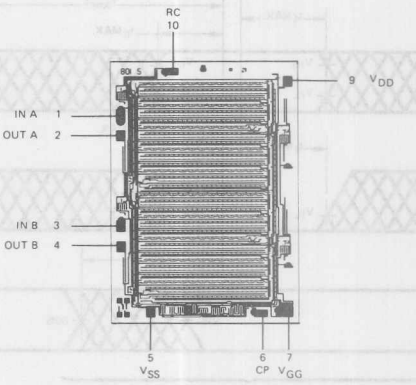
**STATIC SHIFT REGISTER** A shift register that is capable of maintaining stored data without being continuously clocked. Most static shift registers are constructed with dynamic master and static slave flip-flops. The data is stored dynamically while the clock is HIGH and is transferred to the static slaves while the clock is LOW. The clock may be stopped indefinitely in the LOW state, but there are limitations on the time it may reside in the HIGH state.

**SET-UP and HOLD TIMES** The shift register will accept the data that is present on its input around the time the clock goes from HIGH-to-LOW. Because of variations in individual devices, there is some uncertainty as to exactly when, relative to this clock transition, the data will be stored. The set-up and hold times define the limits on this uncertainty. To guarantee storing the correct data, the data inputs should not be changed between the maximum set-up time before the clock transition and the maximum hold time after the clock transition. Data changes within this interval may or may not be detected.

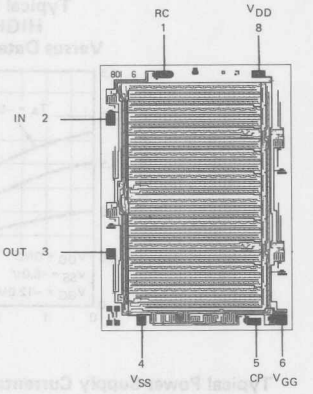
## Am4055/5055




## Am4056/5056




## Am4047/5057

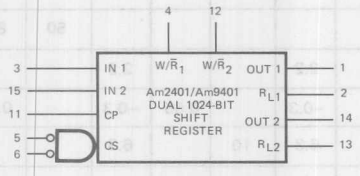



DIE SIZES 0.101" X 0.140"

## Distinctive Characteristics

- Single +5V power supply
- High speed – 2MHz min.
- Single phase TTL clock
- Low clock capacitance – 7.0pF max.
- Low Power 315 mW max. @ 2MHz
  40 μW/bit typ. @ 2 MHz
- Chip select, write, and recirculate logic on chip
- 100% reliability assurance testing in accordance with MIL-STD-883

## LOGIC SYMBOL



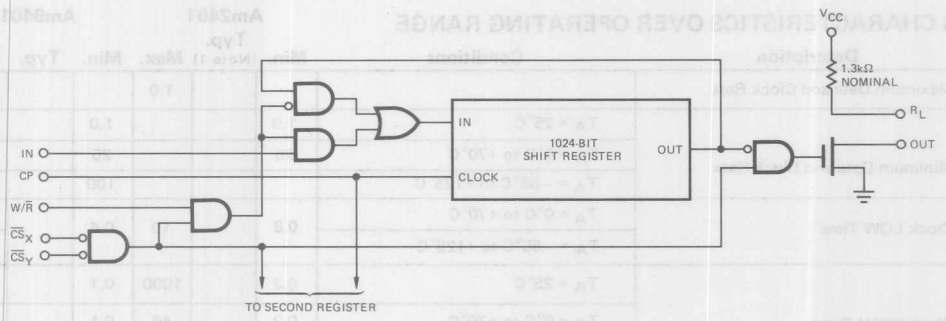

$V_{CC}$ = Pin 16
GND = Pin 8

MOS-455

## FUNCTIONAL DESCRIPTION

The Am9401 is a dual 1024-bit dynamic shift register built using ion-implanted, N-channel, silicon gate MOS technology. The device operates from a single +5 volt power supply and all inputs and outputs, including the clock, are directly TTL compatible. Data is entered into the register on the LOW-to-HIGH transition of the clock input. New data appears on the output following the HIGH-to-LOW clock transition. There are two chip select inputs, $\overline{CS}_X$ and $\overline{CS}_Y$; if either is HIGH then the data in both registers recirculates and the outputs go to a HIGH impedance OFF state. If both chip selects are LOW, then the outputs will be LOW for LOW data and OFF for HIGH data (similar to TTL open collectors). When the chip is selected, the write-recirculate lines control the entry of new data. If $W/\overline{R}$ is HIGH new data is written into the corresponding register; if $W/\overline{R}$ is LOW, the data on the output is recirculated. An internal pull-up resistor to $V_{CC}$ is provided at $R_L$. This point may be connected to the output to establish the HIGH logic level. Many register outputs may be connected together with the $R_L$ connected only once. The Am9401 is a high performance plug-in replacement for the Am2401.

## LOGIC BLOCK DIAGRAM



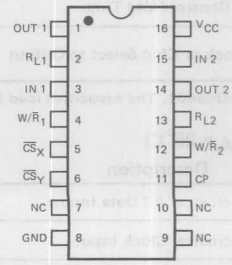

Note: Only one register shown.

MOS-456

## ORDERING INFORMATION

| Package Type | Temperature Range | Order Number | Order Number |
|---|---|---|---|
| 16-Pin Molded DIP | 0°C to +70°C | AM9401PC | P2401 |
| 16-Pin Hermetic DIP | 0°C to +70°C | AM9401DC | C2401 |
| 16-Pin Hermetic DIP | –55°C to +125°C | AM9401DM | |

## CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

MOS-457

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +160°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Power Dissipation | 1W |
| Voltage on Any Pin | −0.5V to +7.0V |

## OPERATING RANGE

| Part Number | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Am9401, 2401PC, DC | 0°C to +70°C | 5.0V ± 5% |
| Am9401DM | −55°C to +125°C | 5.0V ± 5% |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Conditions | Am2401 Min. | Am2401 Typ. (Note 1) | Am2401 Max. | Am9401 Min. | Am9401 Typ. | Am9401 Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | $V_{IN}$ = 5.25V | | | 10 | | | 10 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = 5.25V | | | 100 | | | 100 | µA |
| $I_{CC}$ | $V_{CC}$ Current | $V_{CC}$ = MAX., 80% Duty Cycle, $T_A$ = 25°C | | | 70 | | | 50 | mA |
| | | $V_{CC}$ = MAX., 80% Duty Cycle, $T_A$ = 0°C to +70°C | | | 80 | | | 60 | mA |
| | | $V_{CC}$ = MAX., 80% Duty Cycle, $T_A$ = −55°C to +125°C | | | | | 50 | 80 | mA |
| $V_{IH}$ | Input HIGH Level | | 2.2 | | | 2.2 | | | Volts |
| $V_{IL}$ | Input LOW Level | | −0.3 | | 0.65 | −0.3 | | 0.65 | Volts |
| $I_{OL}$ | Output LOW Current | $V_{OL}$ = 0.45V | 6.3 | 10 | | 6.3 | | | mA |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 1.6mA, $R_L$ connected | | | 0.45 | | | 0.45 | Volts |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −1mA, $R_L$ connected | 2.4 | | $V_{CC}$ | 2.4 | | $V_{CC}$ | Volts |
| $R_L$ | Internal Load Resistor | | 0.5 | 1.5 | 3.0 | 0.5 | | 3.0 | kΩ |

Note: 1. Typical values are at 25°C and $V_{CC}$ = 5.0 V.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

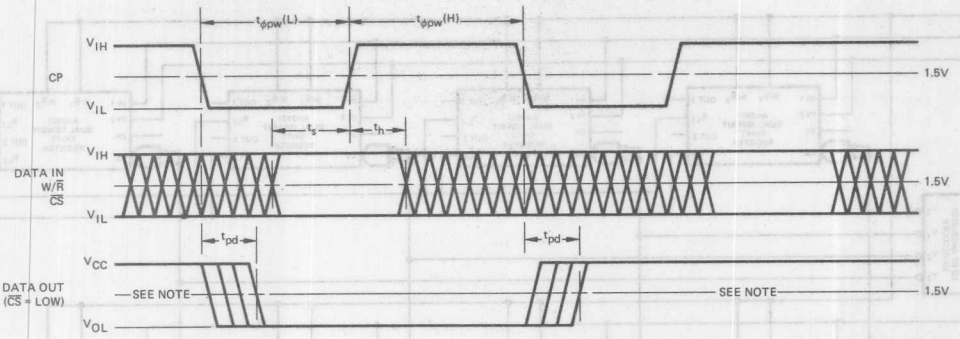
| Parameters | Description | Conditions | Am2401 Min. | Am2401 Typ. (Note 1) | Am2401 Max. | Am9401 Min. | Am9401 Typ. | Am9401 Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum Data and Clock Rate | | | | 1.0 | | | 2.0 | MHz |
| $f_{min}$ | Minimum Data and Clock Rate | $T_A$ = 25°C | 1.0 | | | 1.0 | | | kHz |
| | | $T_A$ = 0°C to +70°C | 25 | | | 25 | | | kHz |
| | | $T_A$ = −55°C to +125°C | | | | 100 | | | kHz |
| $t_{\phi pw}(L)$ | Clock LOW Time | $T_A$ = 0°C to +70°C | 0.8 | | 10 | 0.4 | | 10 | µs |
| | | $T_A$ = −55°C to +125°C | 0.8 | | 10 | 0.4 | | 9 | µs |
| $t_{\phi pw}(H)$ | Clock HIGH Time | $T_A$ = 25°C | 0.2 | | 1000 | 0.1 | | 1000 | µs |
| | | $T_A$ = 0°C to +70°C | 0.2 | | 40 | 0.1 | | 40 | µs |
| | | $T_A$ = −55°C to +125°C | | | | 0.1 | | 1.0 | µs |
| $t_r$, $t_f$ | Clock Rise and Fall Times | | | | 50 | | | 50 | ns |
| $t_s$ | Data and Control Set-Up Time | | 200 | | | 80 | | | ns |
| $t_h$ | Data and Control Hold Time | | 150 | | | 150 | | | ns |
| $t_{pd}$ | Delay, Clock or Chip Select to Output | $R_L$ connected (Note 2), $C_L$ = 100pF, Load = 1 TTL gate | | 250 | 500 | | 160 | 320 Note 2 | ns |

Note: 2. $C_L$ = 20pF for Am9401. The capacitive load is limited primarily by the internal load register.

## CAPACITANCE ($T_A$ = 25°C)

| Parameters | Description | Conditions | Am2401 Min. | Am2401 Typ. | Am2401 Max. | Am9401 Min. | Am9401 Typ. | Am9401 Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $C_{IN}$ | Capacitance, All Data Inputs | f = 1 MHz, $V_{IN}$ = 250 mV, All Pins at $R_L$ Ground | | 4.0 | 7.0 | | 4.0 | 7.0 | pF |
| $C_\phi$ | Capacitance, Clock Input | | | 4.0 | 7.0 | | 4.0 | 7.0 | pF |
| $C_{OUT}$ | Capacitance, Data Output | | | 10 | 14 | | 5.0 | 10 | pF |

## SWITCHING WAVEFORMS

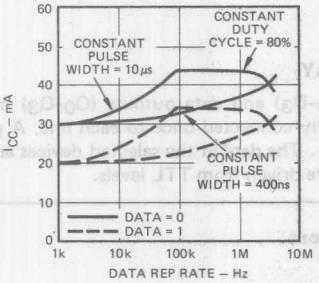



Note: HIGH level on output is established by externally connected load resistor.

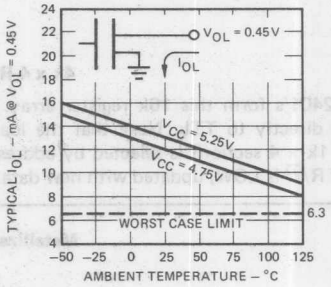
MOS-458

## TYPICAL PERFORMANCE CHARACTERISTICS

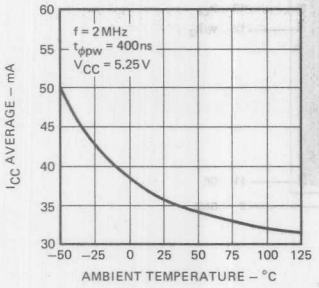
**Power Supply Current ($I_{CC}$) Versus Data Rep. Rate**



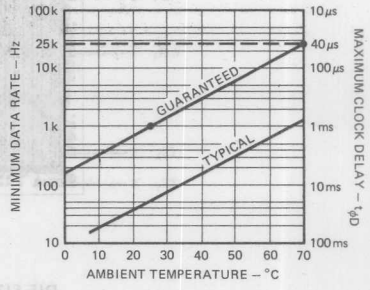

**Temperature Dependence of Output LOW Level Sink Capability**




**Power Supply Current ($I_{CC}$) Versus Ambient Temperature (0°C)**




**Minimum Data Rate and Maximum Clock Delay Versus Ambient Temperature**

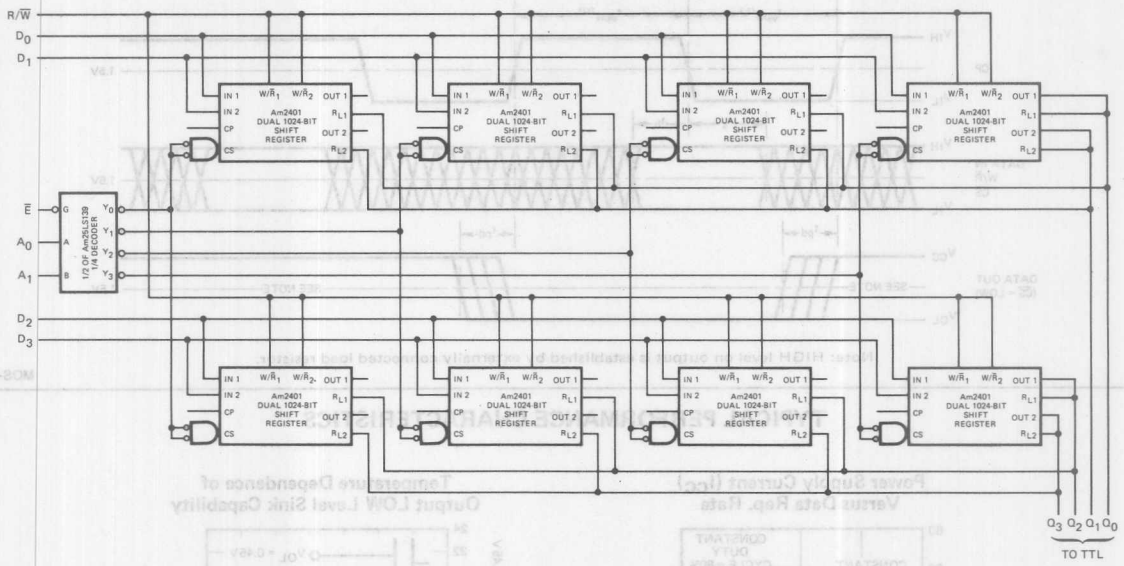



MOS-459

## TRUTH TABLE

| W/$\overline{R}$ | $\overline{CS}_X$ | $\overline{CS}_Y$ | $D_{IN}$ | DATA ENTERED | OUTPUT | OPERATION |
|---|---|---|---|---|---|---|
| X | X | H | X | $D_{IN}$ (t-1024) | OFF | Deselected, Recirculate |
| X | H | X | X | $D_{IN}$ (t-1024) | OFF | Deselected, Recirculate |
| H | L | L | L | LOW | $D_{IN}$ (t-1024) | Read, Write |
| H | L | L | H | HIGH | $D_{IN}$ (t-1024) | Read, Write |
| L | L | L | X | $D_{IN}$ (t-1024) | $D_{IN}$ (t-1024) | Read, Recirculate |

## APPLICATIONS

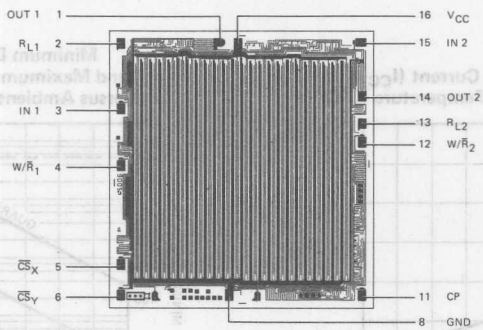



### 4k x 4 REGISTER ARRAY

Eight Am2401's form this 16k register array. Data inputs ($D_0$-$D_3$) and data outputs ($Q_0$-$Q_3$) may be connected directly to TTL. Note that the load resistors are only connected once to each line. A pair of devices (a 1k x 4 section) is selected by address bits $A_0$ and $A_1$. The data in the selected devices are read out and, if R/$\overline{W}$ is LOW, updated with new data. All clock lines are driven from TTL levels.

MOS-460

### Metallization and Pad Layout




DIE SIZE 0.133" X 0.142"

## NUMERICAL INDEX


| | | Page |
|---|---|---|
| Am2812/2812A | 32 x 8 First-In First-Out Memory | 6-1 |
| Am2813/Am2813A | 32 x 9 First-In First-Out Memory | 6-1 |
| Am2841/3341/ 2841A | 64 x 4 First-In First-Out Memory | 6-7 |

# First-In First-Out Memory

## NUMERICAL INDEX


| | | Page |
|---|---|---|
| Am2812/2812A | 32 x 8 First-In First-Out Memory | 6-1 |
| Am2813/Am2813A | 32 x 9 First-In First-Out Memory | 6-1 |
| Am2841/3341/ 2841A | 64 x 4 First-In First-Out Memory | 6-7 |


6

# Am2812 / Am2812A • Am2813 / Am2813A

## 32x8 and 32x9 First–In First–Out Memories

### Distinctive Characteristics

- Completely independent read and write operations
- "Half-full" flag
- Am2812 has serial or parallel input and output
- Data rates up to 1 MHz

## FUNCTIONAL DESCRIPTION

The Am2812 and Am2813 are 32 word by 8-bit and 9-bit first-in first-out memories, respectively. Both devices have completely independent read and write controls and have three-state outputs controlled by an output enable pin (OE). Data on the data inputs ($D_i$) are written into the memory by a pulse on load (PL). The data word automatically ripples through the memory until it reaches the output or another data word. Data is read from the memory by applying a shift out pulse on PD. This dumps the word on the outputs ($Q_i$) and the next word in the buffer moves to the output. An output ready signal (OR) indicates that data is available at the output and also provides a memory empty signal. An input ready (IR) signal indicates that the device is ready to accept data and also provides a memory full signal. Both the Am2812 and Am2813 have master reset inputs which clear all data from the device (reset to all LOWs), and a FLAG signal which goes HIGH when the memory contains more than 15 words.

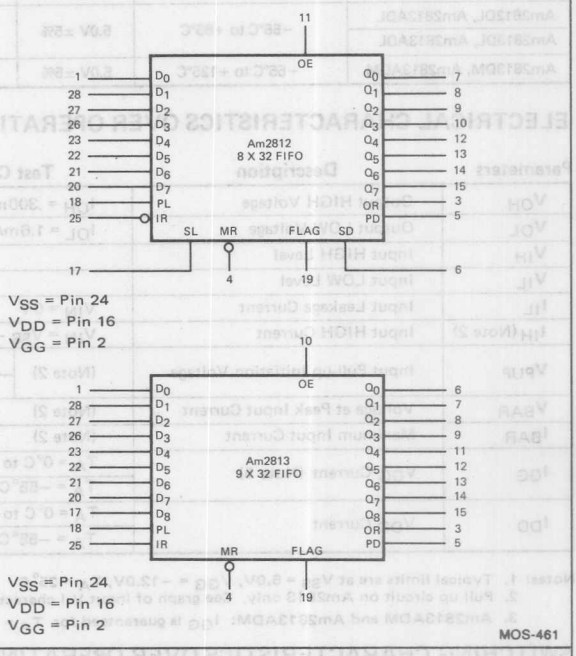
The Am2812 can perform input and output data transfer on a bit-serial basis as well as on 8-bit parallel words. The input buffer is in reality an 8-bit shift register which can be loaded in parallel by the PL command or can be loaded serially through the $D_0$ input by using the SL clock. When 8 bits have been shifted into the input buffer serially, the 8-bit word automatically moves in parallel through the memory. The output includes a built-in parallel-to-serial converter, so that data can be shifted out of the $Q_7$ output by using the SD clock. After 8 clock pulses a new 8-bit word appears at the outputs.

The timing and function of the four control signals, PL, IR, PD, and OR, are designed so that two FIFOs can be placed end to end, with OR of the first driving PL of the second and IR of the second driving PD of the first. With this simple interconnection, strings of FIFOs can control each other reliably to make a FIFO array any number of words deep.

## ORDERING INFORMATION

| Package Type | Frequency | Temperature Range | Am2812 Order Number | Am2813 Order Number |
|---|---|---|---|---|
| Hermetic DIP | 500KHz | 0°C to +70°C | AM2812DC | AM2813DC |
| Hermetic DIP | 500KHz | −55°C to +85°C | AM2812DL | AM2813DL |
| Hermetic DIP | 1MHz | 0°C to +70°C | AM2812ADC | AM2813ADC |
| Hermetic DIP | 1MHz | −55°C to +85°C | AM2812ADL | AM2813ADL |
| Hermetic DIP | 500KHz | −55°C to +125°C | – | AM2813DM |
| Hermetic DIP | 1MHz | −55°C to +125°C | – | AM2813ADM |

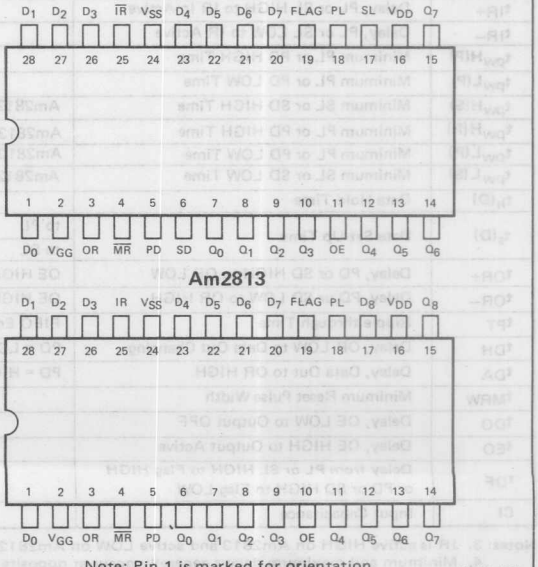
## LOGIC SYMBOLS




MOS-461

## CONNECTION DIAGRAMS

### Top Views




Note: Pin 1 is marked for orientation.

MOS-462

6

| | |
|---|---|
| $V_{DD}$ Supply Voltage | $V_{SS}$ −7V to $V_{SS}$ +0.3V |
| $V_{GG}$ Supply Voltage | $V_{SS}$ −20V to $V_{SS}$ +0.3V |
| DC Input Voltage | $V_{SS}$ −10V to $V_{SS}$ +0.3V |

## OPERATING RANGE

| Part Number | Ambient Temperature | $V_{SS}$ | $V_{DD}$ | $V_{GG}$ |
|---|---|---|---|---|
| Am2812DC, Am2812ADC<br>Am2813DC, Am2813ADC | 0°C to +70°C | 5.0V ±5% | 0V | −12V ±5% |
| Am2812DL, Am2812ADL<br>Am2813DL, Am2813ADL | −55°C to +85°C | 5.0V ±5% | 0V | −12 ±5% |
| Am2813DM, Am2813ADM | −55°C to +125°C | 5.0V ±5% | 0V | −12V ±5% |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = .300mA | | $V_{SS}$ −1.0 | | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 1.6mA | | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Level | | | $V_{SS}$ −1.0 | | | V |
| $V_{IL}$ | Input LOW Level | | | | | 0.8 | V |
| $I_{IL}$ | Input Leakage Current | $V_{IN}$ = 0V (Note 2) | | | | 1.0 | μA |
| $I_{IH}$ (Note 2) | Input HIGH Current | $V_{IN}$ = $V_{SS}$ −1.0V (Note 2) | | 250 | | | μA |
| $V_{PUP}$ | Input Pull-up Initiation Voltage | (Note 2) | $V_{SS}$ = MIN. | | | 2.0 | V |
| | | | $V_{SS}$ = MAX. | | | 2.2 | V |
| $V_{BAR}$ | Voltage at Peak Input Current | (Note 2) | | | | $V_{SS}$ −1.5 | V |
| $I_{BAR}$ | Maximum Input Current | (Note 2) | | | | 1.6 | mA |
| $I_{GG}$ | $V_{GG}$ Current (Note 5) | $T_A$ = 0°C to +70°C | | | 14 | 22 | mA |
| | | $T_A$ = −55°C to +85°C | | | | 27 | |
| $I_{DD}$ | $V_{DD}$ Current | $T_A$ = 0°C to +70°C | | | 30 | 45 | mA |
| | | $T_A$ = −55°C to +85°C | | | | 55 | |

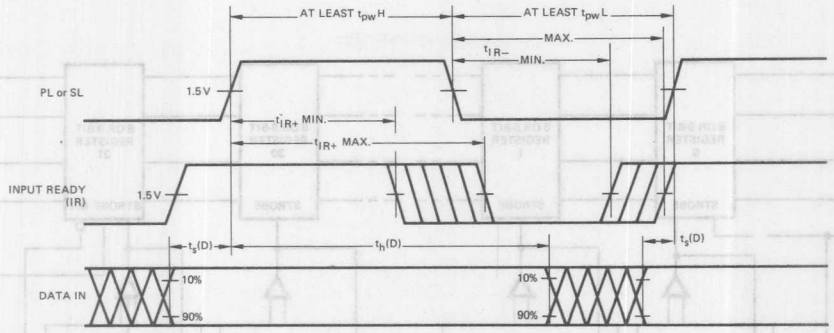
Notes: 1. Typical limits are at $V_{SS}$ = 5.0V, $V_{GG}$ = −12.0V, $T_A$ = 25°C
2. Pull up circuit on Am2813 only. See graph of input V-I characteristics.
3. Am2813ADM and Am2813ADM: $I_{GG}$ is guaranteed for $T_A$ = −55°C to +125°C

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

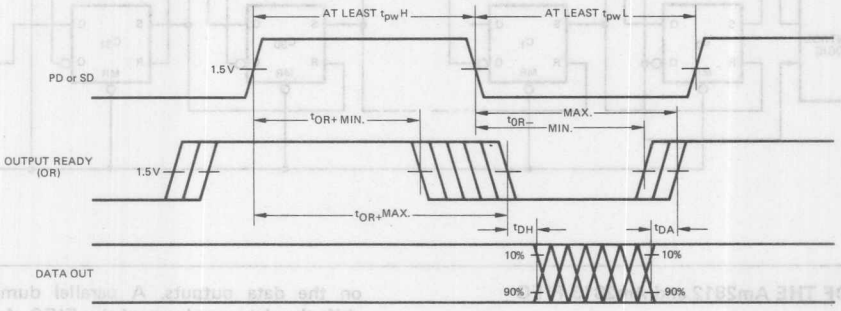
| Parameters | Conditions/Note | Test Conditions | Am2812/Am2813 Min. | Typ. | Max. | Am2812A/Am2813A Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $f_p$ | Maximum Parallel Load or Dump Frequency | | 0.5 | | | 1.0 | | | MHz |
| $t_{IR+}$ | Delay, PL or SL HIGH to IR In-Active | | 100 | 300 | 1100 | 80 | 300 | 450 | ns |
| $t_{IR-}$ | Delay, PL or SL LOW to IR Active | | 100 | 250 | 800 | 80 | 250 | 400 | ns |
| $t_{pw}H(P)$ | Minimum PL or PD HIGH Time | | 100 | | 100 | 80 | | | ns |
| $t_{pw}L(P)$ | Minimum PL or PD LOW Time | | 100 | | 100 | 80 | | | ns |
| $t_{pw}H(S)$ | Minimum SL or SD HIGH Time | Am2812 only | 350 | | 350 | 300 | | | ns |
| $t_{pw}H(P)$ | Minimum PL or PD HIGH Time | Am2813ADM Only | | | | 200 | | | ns |
| $t_{pw}L(P)$ | Minimum PL or PD LOW Time | Am2813ADM Only | | | | 200 | | | ns |
| $t_{pw}L(S)$ | Minimum SL or SD LOW Time | Am2812 only | 350 | | 350 | 300 | | | ns |
| $t_h(D)$ | Data Hold Time | | | 190 | 300 | | 170 | 250 | ns |
| $t_s(D)$ | Data Set-Up Time | to PL | | | 0 | | | 0 | ns |
| | | to SL | | | 100 | | | 90 | |
| $t_{OR+}$ | Delay, PD or SD HIGH to OR LOW | OE HIGH | 100 | 450 | 1100 | 100 | 350 | 520 | ns |
| $t_{OR-}$ | Delay, PD or SD LOW to OR HIGH | OE HIGH | 100 | 400 | 850 | 100 | 300 | 470 | ns |
| $t_{PT}$ | Ripple through Time | FIFO Empty | | | 10 | | | 8 | μs |
| $t_{DH}$ | Delay, OR LOW to Data Out Changing | PD = LOW | 50 | 200 | | 50 | 200 | | ns |
| $t_{DA}$ | Delay, Data Out to OR HIGH | PD = HIGH | 0 | 100 | | 0 | 100 | | ns |
| $t_{MRW}$ | Minimum Reset Pulse Width | | | | 600 | | | 500 | ns |
| $t_{DO}$ | Delay, OE LOW to Output OFF | | | | 600 | | | 500 | ns |
| $t_{EO}$ | Delay, OE HIGH to Output Active | | | | 600 | | | 500 | ns |
| $t_{DF}$ | Delay from PL or SL HIGH to Flag HIGH or PD or SD HIGH to Flag LOW | | | 0.5 | 1.0 | | 0.5 | 1.0 | μs |
| CI | Input Capacitance | | | | 7 | | | 7 | pF |

Notes: 3. IR is active HIGH on Am2813 and active LOW on Am2812.
4. Minimum and maximum delays generally occur at opposite temperature extremes. Devices at approximately the same temperature will have compatible switching characteristics and will drive each other.

## TIMING DIAGRAM




Note: IR inverted on Am2812.

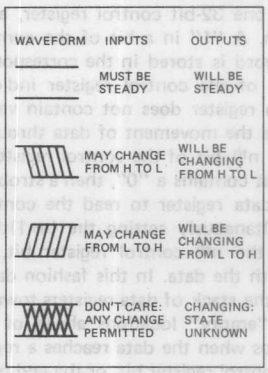



MOS-466

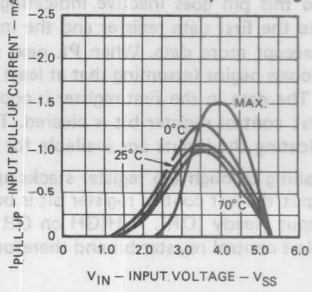
## USER NOTES

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on PD, the OR signal always goes LOW before there is any change in output data and always stays LOW until after the new data has appeared on the outputs, so anytime OR is HIGH, there is good, stable data on the outputs.
3. If PD is held HIGH while the memory is empty and a word is written into the input, then that word will fall through the memory to the output. OR will go HIGH for one internal cycle (at least $t_{OR+}$) and then will go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until PD has been brought LOW.
4. When the master reset is brought LOW, the control register and the outputs are cleared. $\overline{IR}$ goes HIGH and OR goes LOW. If PL is HIGH when the master reset goes HIGH then the data on the inputs will be written into the memory and $\overline{IR}$ will return to the HIGH state until PL is brought LOW. If PL is LOW when the master reset is ended, then $\overline{IR}$ will go LOW but the data on the inputs will not enter the memory until PL goes HIGH.
5. The output enable pin inhibits dump commands while it is LOW and forces the Q outputs to a high impedance state.
6. The serial load and dump lines should not be used for interconnecting two FIFOs. Use the parallel interconnection instead.
7. If less than eight bits have been shifted in using the serial load command, a parallel load pulse will destroy the data in the partially filled input register.

## KEY TO TIMING DIAGRAM

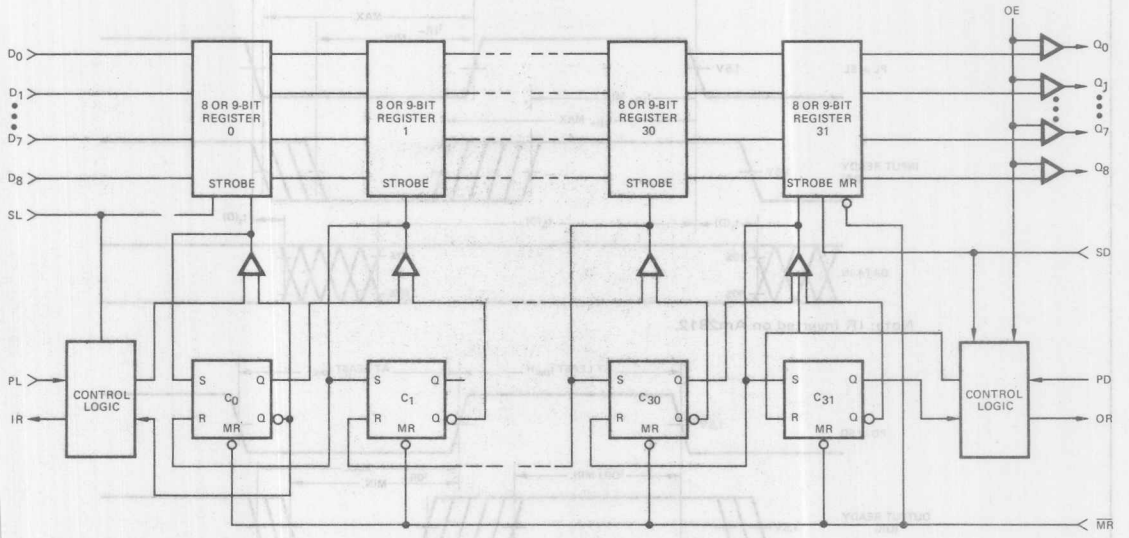



### Pull-up Characteristic Input Current Versus Input Voltage




MOS-467

## LOGIC BLOCK DIAGRAM




MOS-463

### DESCRIPTION OF THE Am2812 and Am2813 FIFO OPERATION

The Am2812 and Am2813 FIFOs consist internally of 32 data registers and one 32-bit control register, as shown in the logic block diagram. A "1" in a bit of the control register indicates that a data word is stored in the corresponding data register. A "0" in a bit of the control register indicates that the corresponding data register does not contain valid data. The control register directs the movement of data through the data registers. Whenever the $n^{th}$ bit of the control register contains a "1" and the (n+1)th bit contains a "0", then a strobe is generated causing the (n+1)th data register to read the contents of the $n^{th}$ data register, simultaneously setting the (n+1)th control register bit and clearing the $n^{th}$ control register bit, so that the control flag moves with the data. In this fashion data in the data register moves down the stack of data registers toward the output as long as there are "empty" locations ahead of it. The fall through operation stops when the data reaches a register n with a "1" in the (n+1)th control register bit, or the end of the register.

Data is initially loaded from the data inputs by applying a LOW-to-HIGH transition on the parallel load (PL) input. A "1" is placed in the first control register bit simultaneously. The first control register bit is returned buffered, to the input ready (IR) output, and this pin goes inactive indicating that data has been entered into the first data register and the input is now "busy", unable to accept more data. When PL next goes LOW, the fall-through process begins (assuming that at least the second location is empty). The data in the first register is copied into the second, and the first control register bit is cleared. This causes IR to go active, indicating the inputs are available for another data word.

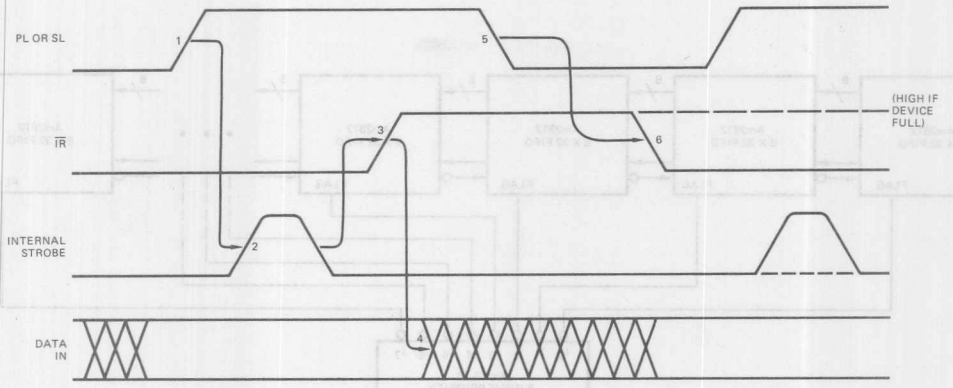
The data falling through the register stacks up at the output end. At the output the last control register bit is buffered and brought out as Output Ready (OR). A HIGH on OR indicates there is a "1" in the last control register bit and therefore there is valid data on the data outputs. A parallel dump command is used to shift the data word out of the FIFO. A LOW-to-HIGH transition on PD clears the last register bit, causing OR to go LOW, indicating that the data on the outputs may no longer be valid. When PD goes LOW, the "0" which is now present at the last control register bit allows the data in the next to the last register to move into the last register position and on to the outputs. The "0" in the control register then "bubbles" back toward the input as the data shifts toward the output.

If the memory is emptied by reading out all the data, then when the last word is being read out and PD goes HIGH, OR will go LOW as before, but when PD next goes LOW, there is no data to move into the last location, so OR remains LOW until more data arrives at the output. Similarly, when the memory is full data written into the first location will not shift into the second when PL goes LOW, and IR will remain inactive instead of returning to an active state.

The pairs of input and output control signals are designed so that the PD input of one FIFO can be driven by the IR output of another, and the OR output of the first FIFO can drive the PL input of the second, allowing simple expansion of the FIFO to any depth. Wider buffers are formed by allowing parallel rows of FIFOs to operate together, as shown in the application on the last page.

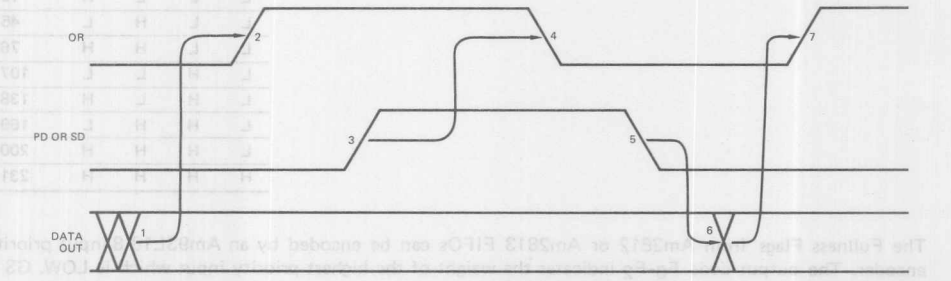
Because the input ready signal is active LOW on the Am2812 a peculiarity occurs when several devices are placed end-to-end. When the second unit of two Am2812's fills up, the data out of the first is not dumped immediately. That is, no shift out command occurs, so that the data last written into the second device remains on the output of the first until an empty location bubbles up from the output. The net effect is that n Am2812s connected end-to-end store 31n+1 words (instead of 32n). The Am2813 stores 32n words in this configuration, because IR is active HIGH and does dump the last word written into the second device.

## Am2812 TIMING DIAGRAM




**Am2812 INPUT TIMING**

When data is steady PL is brought HIGH (1) causing internal data strobe to be generated (2). When data has been loaded, $\overline{IR}$ goes HIGH (3) and data may be changed (4). $\overline{IR}$ remains HIGH until PL is brought LOW (5); then $\overline{IR}$ goes LOW (6) indicating new data may be entered.




**Am2812 OUTPUT TIMING**

When data out is steady (1), OR goes HIGH (2). When PD goes HIGH (3), OR goes LOW (4). When PD goes LOW again (5), the output data changes (6) and OR returns HIGH (7).

The input and output timing diagrams above illustrate the sequence of control on the Am2812. Note that PL matches OR and $\overline{IR}$ matches PD in time, as though the signals were driving each other. The Am2813 pattern is similiar, but IR is active HIGH instead of active LOW (shown in timing diagram on next page).

### FLAG OUTPUT

A flag output is available on the Am2812 and Am2813 to indicate whether the FIFO is more or less than half full. The flag signal is generated by summing the "1s" in the control flip-flops, and therefore is not affected by the movement of data through the register. The flag signal goes HIGH when the 13th, 14th, 15th, or 16th word is loaded into the FIFO. It will remain HIGH until there are less than 15+1/–2 words in the memory. It is always HIGH if there are more than 16 words in the FIFO.

### RESET

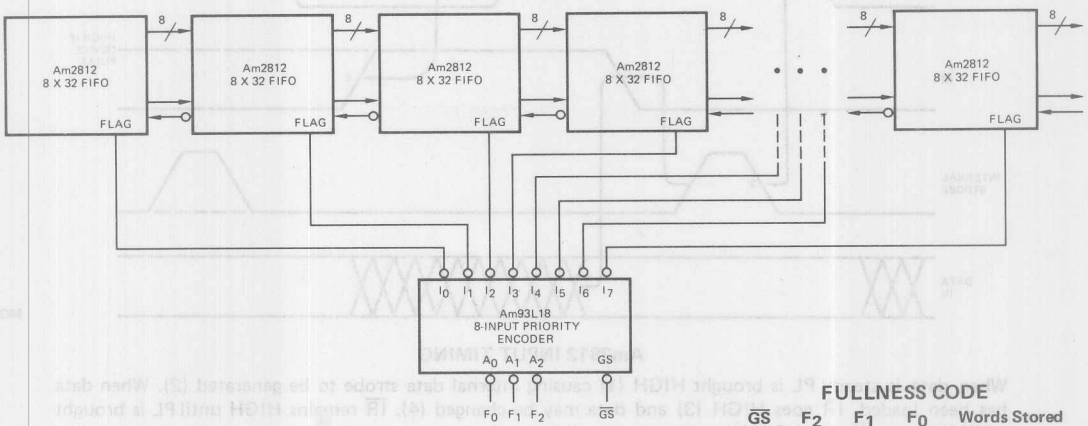
An over-riding master reset ($\overline{MR}$) is used to clear all control register bits and set all the outputs LOW.

### SERIAL INPUT AND OUTPUT (Am2812 ONLY)

The Am2812 also has the ability to read or write serial bit streams, rather than 8-bit words. The device then works like a 256 by 1-bit FIFO. A serial data stream can be loaded into the device by using the serial load input and applying data to $D_0$ input. Inputs $D_1$–$D_7$ must be grounded. The SL signal operates just like the PL input, causing IR to go HIGH and LOW as the bits are entered. The data is simply shifted across the 8-bit input register until 8 bits have been entered; the 8 bits then fall through the register as though they had been loaded in parallel. Following the 8th SL pulse, IR will remain inactive if the FIFO is full.

A corresponding operation occurs on the output, with clock pulses on SD causing successive bits of data to appear on the $O_7$ output. OR moves HIGH and LOW with SD exactly as it does with PD. When 8 bits have been shifted out, the next word appears at the output. If a PD command is applied after the 8 bits on the outputs have been partially shifted out, the remainder of the word is dumped and a new 8-bit word is brought to the output. OR will stay LOW if the FIFO is empty.

When the serial input or output clock is used, the corresponding parallel control line should be grounded and when the PD or PL controls are used the corresponding serial clocks should be grounded.



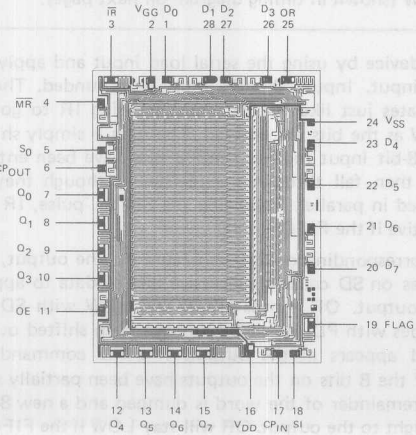

**FULLNESS CODE**

| $\overline{GS}$ | $F_2$ | $F_1$ | $F_0$ | Words Stored |
|---|---|---|---|---|
| L | L | L | L | 0 – 15 |
| L | L | L | H | 13 – 47 |
| L | L | H | L | 45 – 78 |
| L | L | H | H | 76 – 109 |
| L | H | L | L | 107 – 140 |
| L | H | L | H | 138 – 171 |
| L | H | H | L | 169 – 202 |
| L | H | H | H | 200 – 233 |
| H | H | H | H | 231 – 249 |

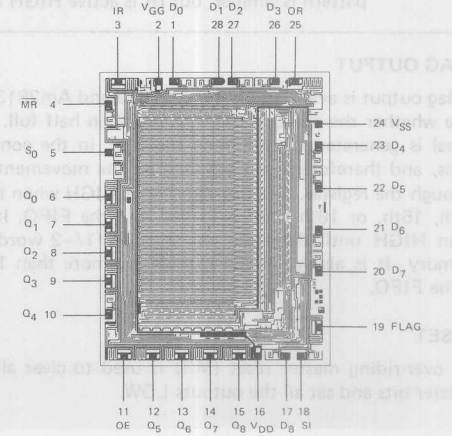
The Fullness Flags from Am2812 or Am2813 FIFOs can be encoded by an Am93L18 8-input priority encoder. The output code $F_0$–$F_2$ indicates the weight of the highest priority input which is LOW. GS is group signal; it is HIGH if all the inputs are HIGH.

## Metallization and Pad Layouts

**Am2812**




**Am2813**




DIE SIZE 0.128" X 0.168"

# Am2841/3341/2841A

## 64 x 4 First-In First-Out Memories

### Distinctive Characteristics

- Plug-In replacement for Fairchild 3341
- Asynchronous buffer for up to 64 four-bit words
- Easily expandable to larger buffers
- Am2841 has 1MHz guaranteed data rate
- Am2841A has 1.2MHz guaranteed data rate
- 100% reliability assurance testing in compliance with MIL-STD-883
- Special input circuit provides true TTL compatibility

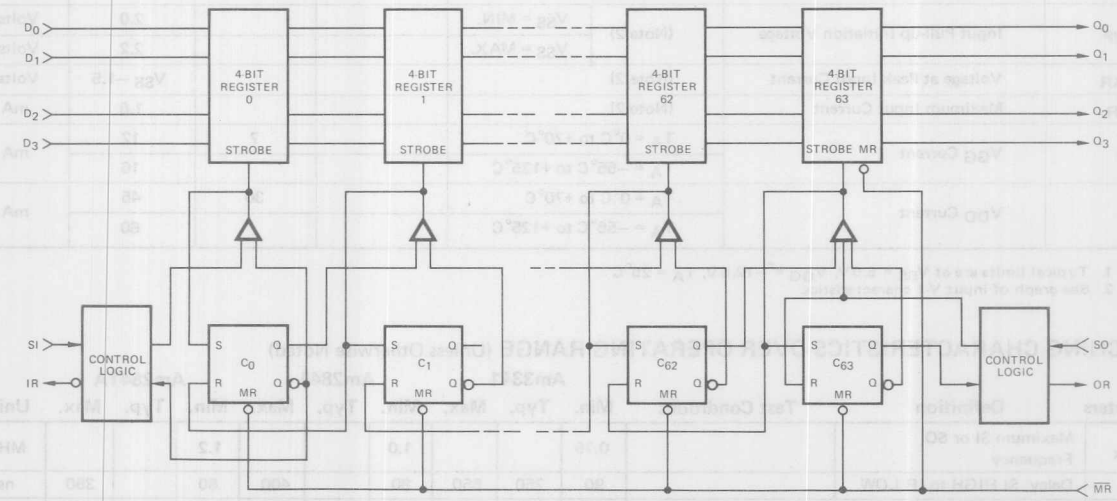
### FUNCTIONAL DESCRIPTION

The Am3341/Am2841/Am2841A is an asynchronous first-in first-out memory stack, organized as 64 four-bit words. The device accepts a four-bit parallel word $D_0$—$D_3$ under control of the shift in (SI) input. Data entered into the FIFO immediately ripples through the device to the outputs $Q_0$—$Q_3$. Up to 64 words may be entered before any words are read from the memory. The stored words line up at the output end in the order in which they were written. A read command on the shift out input (SO) causes the next to the last word of data to move to the output and all data shifts one place down the stack. Input ready (IR) and output ready (OR) signals act as memory full and memory empty flags and also provide the necessary pulses for interconnecting FIFOs to obtain deeper stacks.

Parallel expansion to wider words only requires that rows of FIFOs be placed side by side.

Reading and writing operations are completely independent, so the device can be used as a buffer between two digital machines operating asynchronously and at widely differing clock rates. Special input circuits are provided on all inputs to pull the input signals up to an MOS $V_{IH}$ when a TTL $V_{OH}$ is reached, providing true TTL compatibility without the inconvenience and extra power drain of external pull-up resistors. A detailed description of the operation is on pages 4 and 5 of this data sheet. The Am2841 and Am2841A are functionally identical to the Am3341, but are higher performance devices.

### LOGIC BLOCK DIAGRAM

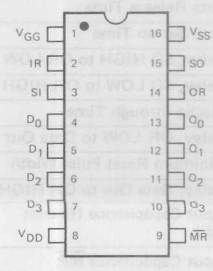



MOS-469

### ORDERING INFORMATION

| Package Type | Temperature Range | Am3341 Order Number | Am2841 Order Number | Am2841A Order Number |
|---|---|---|---|---|
| Molded DIP | 0°C to +70°C | AM3341PC | AM2841PC | AM2841APC |
| Hermetic DIP | 0°C to +70°C | AM3341DC | AM2841DC | AM2841ADC |
| Hermetic DIP | −55°C to +125°C | | AM2841DM | |

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

MOS-470

## MAXIMUM RATING (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| $V_{DD}$ Supply Voltage | $V_{SS}$ −7V to $V_{SS}$ +0.3V |
| $V_{GG}$ Supply Voltage | $V_{SS}$ −20V to $V_{SS}$ +0.3V |
| DC Input Voltage | $V_{SS}$ −10V to $V_{SS}$ +0.3V |

## OPERATING RANGE

| Part No. | Ambient Temperature | $V_{SS}$ | $V_{DD}$ | $V_{GG}$ |
|---|---|---|---|---|
| Am3341PC, DC<br>Am2841PC, DC<br>Am2841APC, DC | 0°C to +70°C | +5.0 ±5% | GND | −12.0 ±5% |
| Am2841DM | −55°C to +125°C | +5.0 ±5% | GND | −12.0 ±5% |

## ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Description | Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = .300mA | | $V_{SS}$ −1.0 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 1.6mA | | | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Level | | | $V_{SS}$ −1.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | | | | | 0.8 | Volts |
| $I_{IL}$ | Input Leakage Current | $V_{IN}$ = 0V | | | | 1.0 | μA |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = $V_{SS}$ −1.0V | | 250 | | | μA |
| $V_{PUP}$ | Input Pull-up Initiation Voltage | (Note 2) | $V_{SS}$ = MIN. | | | 2.0 | Volts |
| | | | $V_{SS}$ = MAX. | | | 2.2 | Volts |
| $V_{BAR}$ | Voltage at Peak Input Current | (Note 2) | | | | $V_{SS}$ −1.5 | Volts |
| $I_{BAR}$ | Maximum Input Current | (Note 2) | | | | 1.6 | mA |
| $I_{GG}$ | $V_{GG}$ Current | $T_A$ = 0°C to +70°C | | | 7 | 12 | mA |
| | | $T_A$ = −55°C to +125°C | | | | 16 | |
| $I_{DD}$ | $V_{DD}$ Current | $T_A$ = 0°C to +70°C | | | 30 | 45 | mA |
| | | $T_A$ = −55°C to +125°C | | | | 60 | |

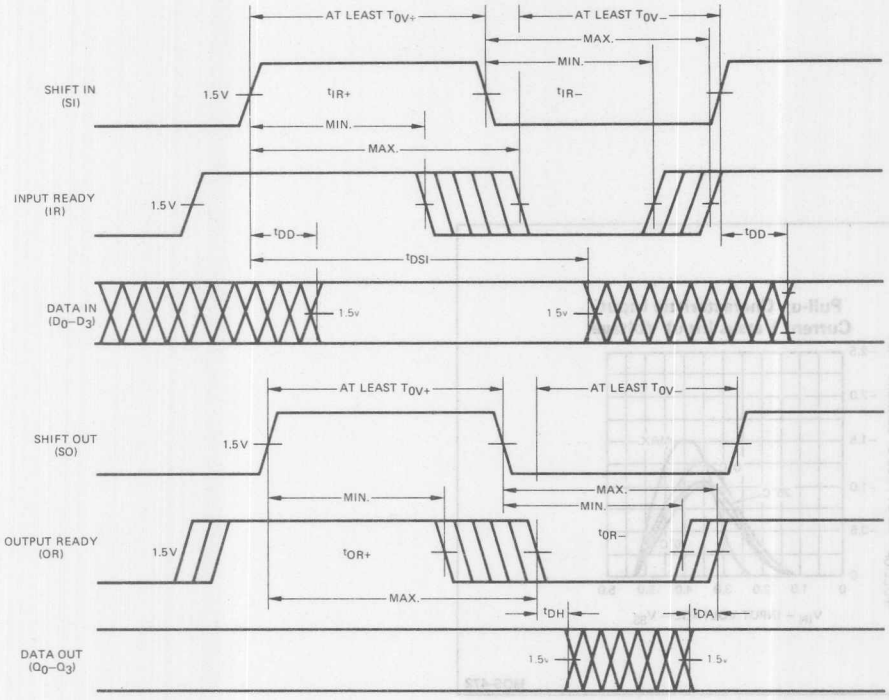
Notes: 1. Typical limits are at $V_{SS}$ = 5.0V, $V_{GG}$ = −12.0V, $T_A$ = 25°C
2. See graph of input V-I characteristics.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

| Parameters | Definition | Test Conditions | Am3341 Min. | Am3341 Typ. | Am3341 Max. | Am2841 Min. | Am2841 Typ. | Am2841 Max. | Am2841A Min. | Am2841A Typ. | Am2841A Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | Maximum SI or SO Frequency | | 0.75 | | | 1.0 | | | 1.2 | | | MHz |
| $t_{IR+}$ | Delay, SI HIGH to IR LOW | | 90 | 250 | 550 | 80 | | 400 | 80 | | 350 | ns |
| $t_{IR-}$ | Delay, SI LOW to IR HIGH | | 138 | 275 | 550 | 100 | | 550 | 100 | | 450 | ns |
| $t_{OV+}$ | Minimum Time SI and IR both HIGH | | 100 | | | 80 | | | 80 | | | ns |
| $t_{OV-}$ | Minimum Time SI and IR both LOW | | 100 | | | 80 | | | 80 | | | ns |
| $t_{DSI}$ | Data Release Time | | 400 | | | 200 | | | 200 | | | ns |
| $t_{DD}$ | Data Set-up Time | | 25 | | | 0 | | | 0 | | | ns |
| $t_{OR+}$ | Delay, SO HIGH to OR LOW | | 90 | 250 | 500 | 70 | 200 | 450 | 80 | 200 | 370 | ns |
| $t_{OR-}$ | Delay, SO LOW to OR HIGH | | 170 | 350 | 850 | 70 | 200 | 550 | 70 | 200 | 450 | ns |
| $t_{PT}$ | Ripple through Time | FIFO Empty | | 10 | 32 | | 8 | 16 | | 8 | 16 | μs |
| $t_{DH}$ | Delay, OR LOW to Data Out | SO = LOW | 75 | | | 75 | | | 75 | | | ns |
| $t_{MRW}$ | Minimum Reset Pulse Width | | | | 400 | | | 400 | | | 400 | ns |
| $t_{DA}$ | Delay, Data Out to OR HIGH | SO = HIGH | 0 | 30 | | 0 | 20 | | 0 | 20 | | ns |
| CI | Input Capacitance (Except $\overline{MR}$) | | | | 7 | | | 7 | | | 7 | pF |
| $C_{MR}$ | Input Capacitance $\overline{MR}$ | | | | 15 | | | 7 | | | 7 | pF |

Note: Switching times over the entire temperature range are such that two devices at approximately the same ambient temperature can drive each other.

## TIMING DIAGRAM

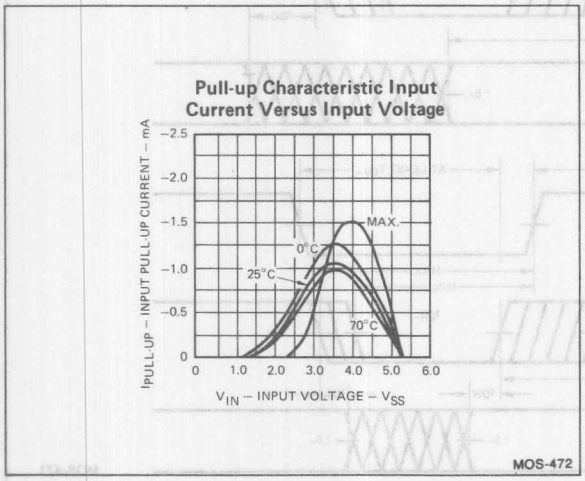



MOS-471

### USER NOTES

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and always stays LOW until after the new data has appeared on the outputs, so anytime OR is HIGH, there is good, stable data on the outputs.
3. If SO is held HIGH while the memory is empty and a word is written into the input, then that word will fall through the memory to the output. OR will go HIGH for one internal cycle (at least $t_{OR+}$) and then will go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the master reset is brought LOW, the control register and the outputs are cleared. IR goes HIGH and OR goes LOW. If SI is HIGH when the master reset goes HIGH then the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the master reset is ended, then IR will go HIGH, but the data on the inputs will not enter the memory until SI goes HIGH.

6




## DESCRIPTION OF THE Am3341 FIFO OPERATION

The Am3341 FIFO consists internally of 64 four-bit data registers and one 64-bit control register, as shown in the logic block diagram. A "1" in a bit of the control register indicates that a four-bit data word is stored in the corresponding data register. A "0" in a bit of the control register indicates that the corresponding data register does not contain valid data. The control register directs the movement of data through the data registers. Whenever the $n^{th}$ bit of the control register contains a "1" and the (n+1)th bit contains a "0", then a strobe is generated causing the (n+1)th data register to read the contents of the $n^{th}$ data register, simultaneously setting the (n+1)th control register bit and clearing the $n^{th}$ control register bit, so that the control flag moves with the data. In this fashion data in the data register moves down the stack of data registers toward the output as long as there are "empty" locations ahead of it. The fall through operation stops when the data reaches a register n with a "1" in the (n+1)th control register bit, or the end of the register.

Data is initially loaded from the four data inputs $D_0$–$D_3$ by applying a LOW-to-HIGH transition on the shift in (SI) input. A "1" is placed in the first control register bit simultaneously. The first control register bit is returned, buffered, to the input ready (IR) output, and this pin goes LOW indicating that data has been entered into the first data register and the input is now "busy", unable to accept more data. When SI next goes LOW, the fall-through process begins (assuming that at least the second location is empty). The data in the first register is copied into the second, and the first control register bit is cleared. This causes IR to go HIGH, indicating the inputs are available for another data word.

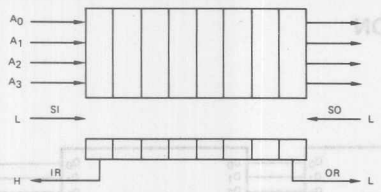
The data falling through the register stacks up at the output end. At the output the last control register bit is buffered and brought out as Output Ready (OR). A HIGH on OR indicates there is a "1" in the last control register bit and therefore there is valid data on the four data outputs $Q_0$–$Q_3$. An input signal, shift out (SO), is used to shift the data out of the FIFO. A LOW-to-HIGH transition on SO clears the last register bit, causing OR to go LOW, indicating that the data on the outputs may no longer be valid. When SO goes LOW, the "0" which is now present at the last control register bit allows the data in the next to the last register to move into the last register position and on to the outputs. The "0" in the control register then "bubbles" back toward the input as the data shifts toward the output.

If the memory is emptied by reading out all the data, then when the last word is being read out and SO goes HIGH, OR will go LOW as before, but when SO next goes LOW, there is no data to move into the last location, so OR remains LOW until more data arrives at the output. Similarly, when the memory is full data written into the first location will not shift into the second when SI goes LOW, and IR will remain LOW instead of returning to a HIGH state.

The pairs of input and output control signals are designed so that the SO input of one FIFO can be driven by the IR output of another, and the OR output of the first FIFO can drive the SI input of the second, allowing simple expansion of the FIFO to any depth. Wider buffers are formed by allowing parallel rows of FIFOs to operate together, as shown in the application on the last page.

An over-riding master reset ($\overline{MR}$) is used to reset all control register bits and remove the data from the output (i.e. reset the outputs to all LOW).

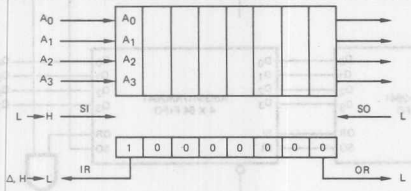
1



**INITIAL CONDITION**

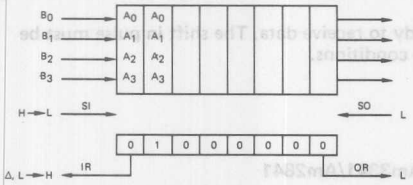
FIFO empty, SI LOW IR HIGH, word "A" on inputs.

2



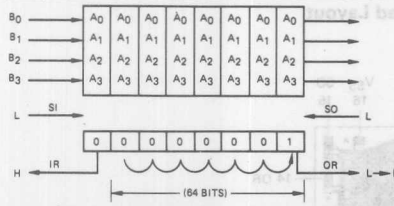
Write input into first stage by raising SI. (Δ = delay) IR goes LOW indicating data has been entered.

3



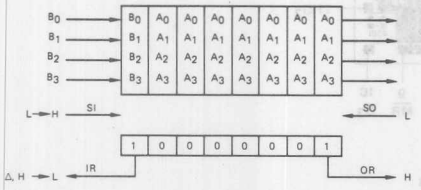
Release data into FIFO by lowering SI. After delay, data moves to second location, and IR goes HIGH indicating input available for new data word.

4



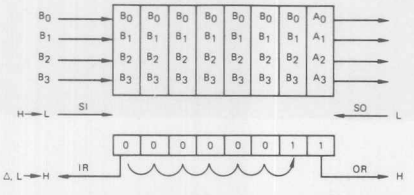
Data spontaneously ripple through registers to end of FIFO, causing OR to go HIGH. The time required for data to fall completely through the FIFO is the "Ripple-through Time".

5



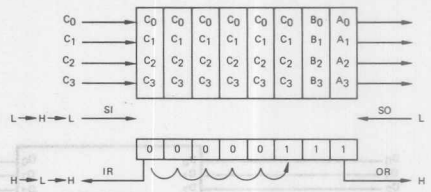
Word "B" written into FIFO

6



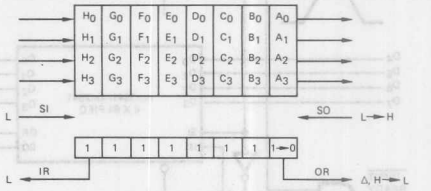
SI goes LOW allowing word "B" to fall through.

7



Word "C" written in same manner, and so on. When buffer is full, all control bits are 1's and IR stays LOW.

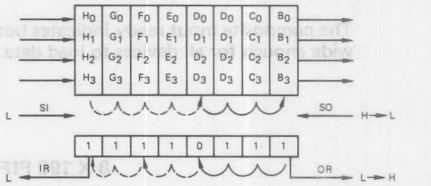
8



**FIRST READ OPERATION**

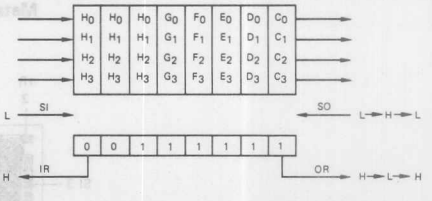
SO goes HIGH, indicating "Ready to Read". OR then goes LOW indicating "Data Read".

9



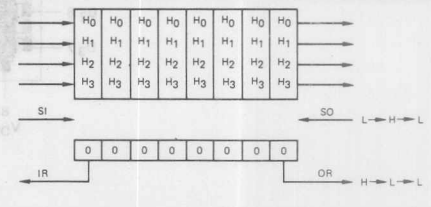
When SO goes LOW, the "0" in the last control bit bubbles toward the memory input. OR goes HIGH as the new word arrives at the output. IR goes HIGH when "0" reaches input.

10



Read word "B" out, word "C" moves to output, and so on.

11

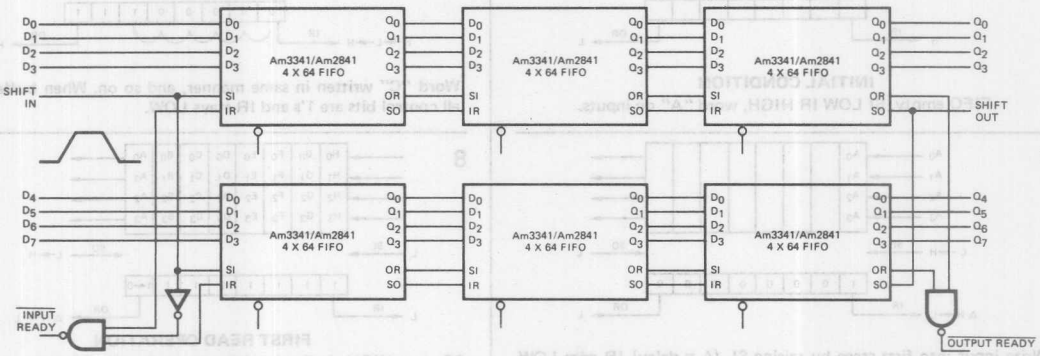


Read word "H". OR stays LOW because FIFO is empty. Word "H" remains in output until new word falls through.

MOS-480

6

## APPLICATION

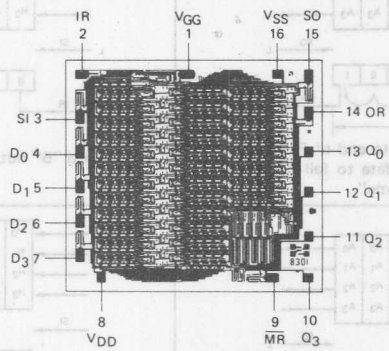



The composite input ready indicates both devices are ready to receive data. The shift in pulse must be wide enough for all devices to load data under worst case conditions.

**8 X 192 FIFO Buffer Using Am3341/Am2841**

MOS-473

**Metallization and Pad Layout**




126 x 138 Mils

# Microprocessors and Peripheral Circuits

## NUMERICAL INDEX


| | | |
|---|---|---|
| Am8035 | Single-Chip 8-Bit Microcomputer | 7-1 |
| Am8048 | Single-Chip 8-Bit Microcomputer | 7-1 |
| Am8080A/9080A | 8-Bit | 7-5 |
| Am8085A/Am8085A-5/ Am9085ADM | Single-Chip 8-Bit N-Channel | 7-13 |
| Am8155 | 2048-Bit Static MOS RAM with I/O Ports and Timer | 7-26 |
| Am8156 | 2048-Bit Static MOS RAM with I/O Ports and Timer | 7-26 |
| Am8251/9551 | Programmable Communications Interface | 7-36 |
| Am8253/8253-5 | Programmable Interval Timer | 7-43 |
| Am8255A | Programmable Peripheral Interface | 7-49 |
| Am8255A-5 | Programmable Peripheral Interface | 7-49 |
| Am8257/9557 | Programmable DMA Controller | 7-54 |
| Am8279 | Programmable Keyboard/Display Interface | 7-62 |
| Am8279-5 | Programmable Keyboard/Display Interface | 7-62 |
| Am9511A | Arithmetic Processor | 7-66 |
| Am9512 | Floating Point Processor | 7-91 |
| Am9513 | System Timing Controller | 7-110 |
| Am9517A | Multimode DMA Controller | 7-135 |
| Am9519A | Universal Interrupt Controller | 7-149 |

# Microprocessors and Peripheral Circuits

## NUMERICAL INDEX


| | | |
|---|---|---|
| Am8035 | Single-Chip 8-Bit Microcomputer | 7-1 |
| Am8048 | Single-Chip 8-Bit Microcomputer | 7-1 |
| Am8080A/9080A | 8-Bit | 7-5 |
| Am8085A/Am8085A-5/ Am9085ADM | Single-Chip 8-Bit N-Channel | 7-13 |
| Am8155 | 2048-Bit Static MOS RAM with I/O Ports and Timer | 7-25 |
| Am8156 | 2048-Bit Static MOS RAM with I/O Ports and Timer | 7-25 |
| Am8251/9551 | Programmable Communications Interface | 7-35 |
| Am8253/8253-5 | Programmable Interval Timer | 7-43 |
| Am8255A | Programmable Peripheral Interface | 7-49 |
| Am8255A-5 | Programmable Peripheral Interface | 7-49 |
| Am8257/9557 | Programmable DMA Controller | 7-54 |
| Am8279 | Programmable Keyboard/Display Interface | 7-62 |
| Am8279-5 | Programmable Keyboard/Display Interface | 7-62 |
| Am9511A | Arithmetic Processor | 7-66 |
| Am9512 | Floating Point Processor | 7-91 |
| Am9513 | System Timing Controller | 7-110 |
| Am9517A | Multimode DMA Controller | 7-135 |
| Am9519A | Universal Interrupt Controller | 7-149 |

# Am8048/8035

## Single Chip 8-Bit Microcomputers

### DISTINCTIVE CHARACTERISTICS

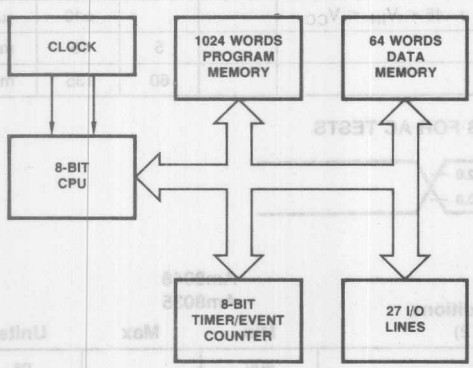
- 8-bit CPU, ROM, RAM, I/O in single package
- Single +5V supply
- All instructions 1 or 2 cycles
- Over 90 instructions: 70% single byte
- 1K x 8 ROM
- 64 x 8 RAM
- 27 I/O lines
- Interval timer/event counter
- Easily expandable memory and I/O
- Single level interrupt
- 100% reliability assurance testing to MIL-STD-883

### GENERAL DESCRIPTION

The Am8048 contains a 1k x 8 program memory, a 64 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on board oscillator and clock circuits. For systems that require extra capability, the Am8048 can be expanded using standard memories and Am9080A peripherals. The Am8035 is the equivalent of an Am8048 without program memory.

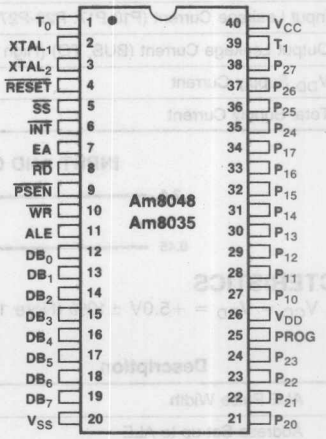
The microprocessor is designed to be an efficient controller. The Am8048 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over two bytes in length.

### BLOCK DIAGRAM




MOS-163

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

MOS-164

### ORDERING INFORMATION

| Package Type | Ambient Temperature Specification | Order Numbers | |
|---|---|---|---|
| Hermetic DIP* | 0°C ≤ $T_A$ ≤ +70°C | AM8048DC<br>AM8048CC | AM8035DC<br>AM8035CC |
| Molded DIP | | AM8048PC | AM8035PC |

*Hermetic = Ceramic = DC = CC = D-40-1.

## MAXIMUM RATINGS (Above which useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | 0°C to +70°C |
| Voltage on Any Pin with Respect to Ground | −0.5V to +7.0V |
| Power Dissipation | 1.5W |

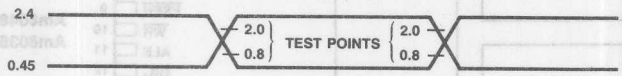
The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## DC AND OPERATING CHARACTERISTICS

$T_A$ = 0 to 70°C, $V_{CC}$ = $V_{DD}$ = +5.0V ±10% (Note 1), $V_{SS}$ = 0V

| Parameters | Description | Test Conditions | Limits Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage (All Except $\overline{RESET}$, X1, X2) | | −.5 | | .8 | Volts |
| $V_{IL1}$ | Input Low Voltage ($\overline{RESET}$, X1, X2) | | −.5 | | .6 | Volts |
| $V_{IH}$ | Input High Voltage (All Except XTAL1, XTAL2, $\overline{RESET}$) | | 2.0 | | $V_{CC}$ | Volts |
| $V_{IH1}$ | Input High Voltage (X1, X2, $\overline{RESET}$) | | 3.8 | | $V_{CC}$ | Volts |
| $V_{OL}$ | Output Low Voltage (BUS) | $V_{OL}$ = 2.0mA | | | .45 | Volts |
| $V_{OL1}$ | Output Low Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE) | $I_{OL}$ = 1.8mA | | | .45 | Volts |
| $V_{OL2}$ | Output Low Voltage (PROG) | $I_{OL}$ = 1.0mA | | | .45 | Volts |
| $V_{OL3}$ | Output Low Voltage (All Other Outputs) | $I_{OL}$ = 1.6mA | | | .45 | Volts |
| $V_{OH}$ | Output High Voltage (BUS) | $I_{OH}$ = −400μA | 2.4 | | | Volts |
| $V_{OH1}$ | Output High Voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE) | $I_{OH}$ = −100μA | 2.4 | | | Volts |
| $V_{OH2}$ | Output High Voltage (All Other Outputs) | $I_{OH}$ = −40μA | 2.4 | | | Volts |
| $I_{LI}$ | Input Leakage Current (T1, $\overline{INT}$) | $V_{SS} \leq V_{IN} \leq V_{CC}$ | | | ±10 | μA |
| $I_{LI1}$ | Input Leakage Current (P10-P17, P20-P27, EA, $\overline{SS}$) | $V_{SS}$ + .45 ≤ $V_{IN} \leq V_{CC}$ | | | −500 | μA |
| $I_{LO}$ | Output Leakage Current (BUS, TO) (High Impedance State) | $V_{SS}$ + .45 ≤ $V_{IN} \leq V_{CC}$ | | | ±10 | μA |
| $I_{DD}$ | $V_{DD}$ Supply Current | | | 5 | 15 | mA |
| $I_{DD}$ + $I_{CC}$ | Total Supply Current | | | 60 | 135 | mA |

### INPUT AND OUTPUT WAVEFORMS FOR AC TESTS




## AC CHARACTERISTICS

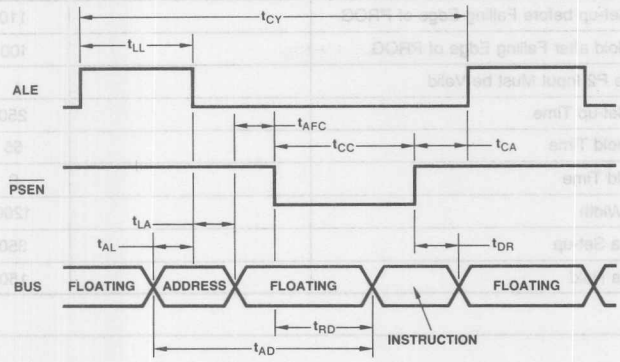
$T_A$ = 0 to 70°C, $V_{CC}$ = $V_{DD}$ = +5.0V ±10% (Note 1), $V_{SS}$ = 0V

| Parameters | Description | Test Conditions (Note 2) | Am8048 Am8035 Min | Max | Units |
|---|---|---|---|---|---|
| $t_{LL}$ | ALE Pulse Width | | 400 | | ns |
| $t_{AL}$ | Address Set-up to ALE | | 120 | | ns |
| $t_{LA}$ | Address Hold from ALE | | 80 | | ns |
| $t_{CC}$ | Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$) | | 700 | | ns |
| $t_{DW}$ | Data Set-up Before $\overline{WR}$ | | 500 | | ns |
| $t_{WD}$ | Data Hold After $\overline{WR}$ | $C_L$ = 20pF | 120 | | ns |
| $t_{CY}$ | Cycle Time | 6MHz XTAL (3.6MHz XTAL for -8) | 2.5 | 15.0 | μs |
| $t_{DR}$ | Data Hold | | 0 | 200 | ns |
| $t_{RD}$ | PSEN, RD to Data In | | | 500 | ns |
| $t_{AW}$ | Address Set-up to $\overline{WR}$ | | 230 | | ns |
| $t_{AD}$ | Address Set-up to Data In | | | 950 | ns |
| $t_{AFC}$ | Address Float to $\overline{RD}$, $\overline{PSEN}$ | | 0 | | ns |
| $t_{CA}$ | Control Pulse to ALE | | 10 | | ns |

Notes: 1. $V_{CC}$ and $V_{DD}$ for Am8035-8 are ±5%.
2. Control Outputs: $C_L$ = 80pF.
Bus Outputs: $C_L$ = 150pF, $t_{CY}$ = 2.5μs.

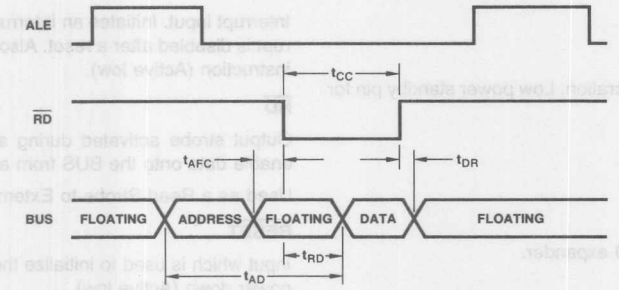
## WAVEFORMS

### INSTRUCTION FETCH FROM EXTERNAL PROGRAM MEMORY



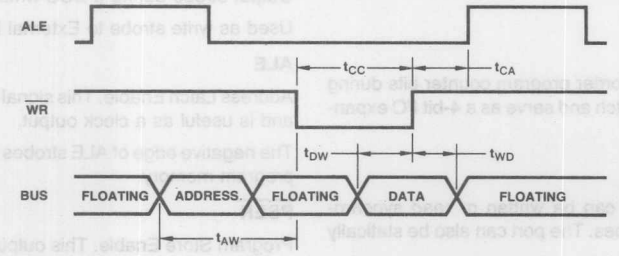

MOS-165

### READ FROM EXTERNAL DATA MEMORY



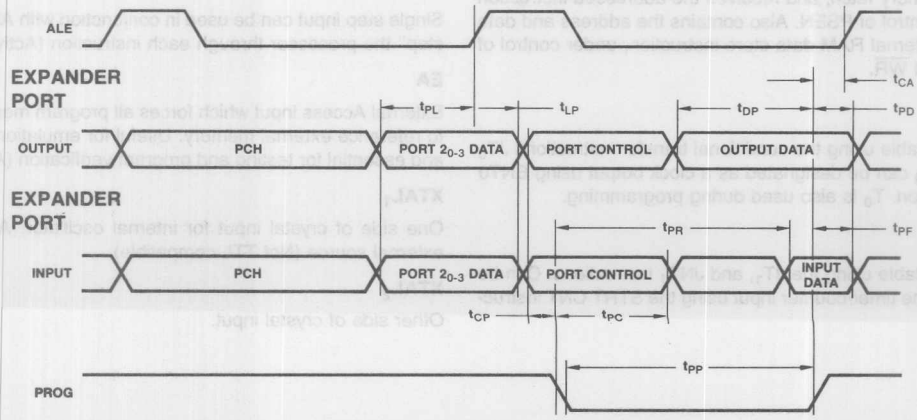

MOS-166

### WRITE TO EXTERNAL DATA MEMORY




MOS-167

### PORT 2 TIMING




MOS-168

7

| Parameters | Description | Test Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|
| $t_{CP}$ | Port Control Set-up before Falling Edge of PROG | | 110 | | ns |
| $t_{PC}$ | Port Control Hold after Falling Edge of PROG | | 100 | | ns |
| $t_{PR}$ | PROG to Time P2 Input Must be Valid | | | 810 | ns |
| $t_{DP}$ | Output Data Set-up Time | | 250 | | ns |
| $t_{PD}$ | Output Data Hold Time | | 65 | | ns |
| $t_{PF}$ | Input Data Hold Time | | 0 | 150 | ns |
| $t_{PP}$ | PROG Pulse Width | | 1200 | | ns |
| $t_{PL}$ | Port 2 I/O Data Set-up | | 350 | | ns |
| $t_{LP}$ | Port 2 I/O Data Hold | | 150 | | ns |

## PIN DESCRIPTION

**$V_{SS}$**

Circuit GND potential.

**$V_{DD}$**

Power supply; +5V during operation. Low power standby pin for Am8048 ROM.

**$V_{CC}$**

Main power supply; +5V.

**PROG**

Output strobe for Am8243 I/O expander.

**$P_{10}$-$P_{17}$ Port 1**

8-bit quasi-bidirectional port.

**$P_{20}$-$P_{27}$ Port 2**

8-bit quasi-bidirectional port.

$P_{20}$-$P_{23}$ contain the four high order program counter bits during an exteral program memory fetch and serve as a 4-bit I/O expander bus for Am8243.

**$D_0$-$D_7$ BUS**

True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched.

Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$ and $\overline{WR}$.

**$T_0$**

Input pin testable using the conditional transfer instructions $JT_0$ and $JNT_0$. $T_0$ can be designated as a clock output using ENT0 CLK instruction. $T_0$ is also used during programming.

**$T_1$**

Input pin testable using the $JT_1$, and $JNT_1$ instructions. Can be designated the timer/counter input using the STRT CNT instruction.

**$\overline{INT}$**

Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction (Active low).

**$\overline{RD}$**

Output strobe activated during a BUS read. Can be used to enable data onto the BUS from an external device.

Used as a Read Strobe to External Data Memory (Active low).

**$\overline{RESET}$**

Input which is used to initialize the processor. Also used during power down (Active low).

**$\overline{WR}$**

Output strobe during a BUS write (Active low) (Non-TTL $V_{IH}$).

Used as write strobe to External Data Memory.

**ALE**

Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output.

The negative edge of ALE strobes address into external data and program memory.

**$\overline{PSEN}$**

Program Store Enable. This output occurs only during a fetch to external program memory (Active low).

**$\overline{SS}$**

Single step input can be used in conjunction with ALE to "single step" the processor through each instruction (Active low).

**EA**

External Access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification (Active high).

**$XTAL_1$**

One side of crystal input for internal oscillator. Also input for external source (Not TTL compatible).

**$XTAL_2$**

Other side of crystal input.

# Am8080A/9080A

## 8-Bit Microprocessor

### Distinctive Characteristics

- Plug-in replacements for 8080A, 8080A-1, 8080A-2
- High-speed version with 1μsec instruction cycle
- Military temperature range operation to 1.5μsec
- Ion-implanted, n-channel, silicon-gate MOS technology
- 3.2mA of output drive at 0.4V (two full TTL loads)
- 700mV of high, 400mV of low level noise immunity
- 820mW maximum power dissipation at ±5% power
- 100% reliability assurance testing to MIL-STD-883

### GENERAL DESCRIPTION

The Am9080A products are complete, general-purpose, single-chip digital processors. They are fixed instruction set, parallel, 8-bit units fabricated with Advanced N-Channel Silicon Gate MOS technology. When combined with external memory and peripheral devices, powerful microcomputer systems are formed. The Am9080A may be used to perform a wide variety of operations, ranging from complex arithmetic calculations to character handling to bit control. Several versions are available offering a range of performance options.

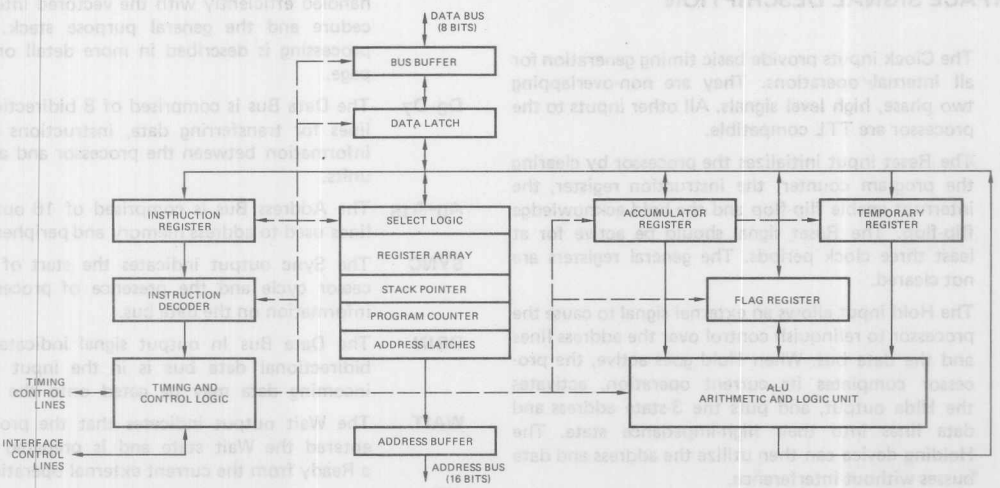
The processor has a 16-bit address bus that may be used to directly address up to 64K bytes of memory. The memory may be any combination of read/write and read-only. Data are transferred into or out of the processor on a bi-directional 8-bit data bus that is separate from the address lines. The data bus transfers instructions, data and status information between system devices. All transfers are handled using asynchronous handshaking controls so that any speed memory or I/O device is easily accommodated.

An accumulator plus six general purpose registers are available to the programmer. The six registers are each 8 bits long and may be used singly or in pairs for both 8 and 16-bit operations. The accumulator forms the primary working register and is the destination for many of the arithmetic and logic operations.

A general purpose push-down stack is an important part of the processor architecture. The contents of the stack reside in R/W memory and the control logic, including a 16-bit stack pointer, is located on the processor chip. Subroutine call and return instructions automatically use the stack to store and retrieve the contents of the program counter. Push and Pop instructions allow direct use of the stack for storing operands, passing parameters and saving the machine state.

An asynchronous vectored interrupt capability is included to allow external signals to modify the instruction stream. The interrupting device may specify an interrupt instruction to be executed and may thus vector the program to a particular service location, or perform some other direct function. Direct memory access (DMA) capability is also included.

### BLOCK DIAGRAM



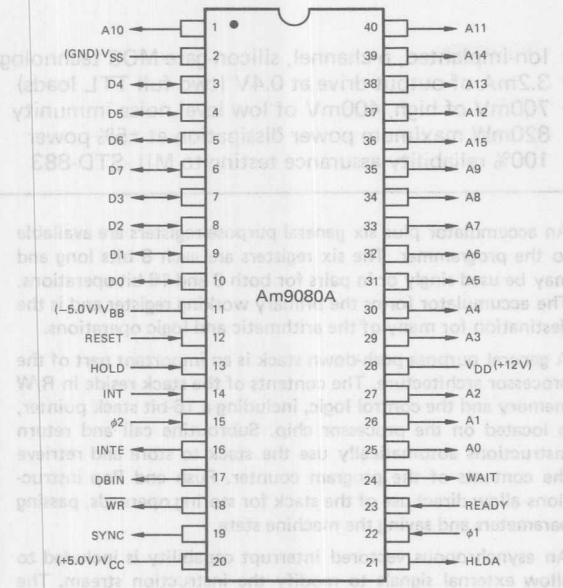

MOS-155

### ORDERING INFORMATION

| Package Type | Ambient Temperature Specification | Minimum Clock Period | | | |
|---|---|---|---|---|---|
| | | 250ns | 320ns | 380ns | 480ns |
| Hermetic DIP* | 0°C ≤ $T_A$ ≤ +70°C | AM9080A-4DC<br>AM9080A-4CC | AM9080A-1DC<br>AM9080A-1CC<br>D8080A-1 | AM9080A-2DC<br>AM9080A-2CC<br>D8080A-2 | AM9080ADC<br>AM9080ACC<br>D8080A |
| Molded DIP | | AM9080A-4PC | AM9080A-1PC<br>P8080A-1 | AM9080A-2PC<br>P8080A-2 | AM9080APC<br>P8080A |
| Hermetic DIP | −55°C ≤ $T_A$ ≤ +125°C | | | AM9080A-2DM | AM9080ADM<br>AM8080A |

*Hermetic = Ceramic = DC = CC = D-40-1.

## CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

MOS-156

## INTERFACE SIGNAL SUMMARY

| TYPE | PINS | ABBREVIATION | SIGNAL |
|---|---|---|---|
| INPUT | 1 | $V_{SS}$ | Ground |
| INPUT | 3 | $V_{DD}$, $V_{CC}$, $V_{BB}$ | +12V, +5V, –5V Supplies |
| INPUT | 2 | $\phi 1$, $\phi 2$ | Clocks |
| INPUT | 1 | RESET | Reset |
| INPUT | 1 | HOLD | Hold |
| INPUT | 1 | INT | Interrupt |
| INPUT | 1 | READY | Ready |
| IN/OUT | 8 | $D_0$–$D_7$ | Data Bus |
| OUTPUT | 16 | $A_0$–$A_{15}$ | Address |
| OUTPUT | 1 | INTE | Interrupt Enable |
| OUTPUT | 1 | DBIN | Data Bus In Control |
| OUTPUT | 1 | $\overline{WR}$ | Write Not |
| OUTPUT | 1 | SYNC | Cycle Synchronization |
| OUTPUT | 1 | HLDA | Hold Acknowledge |
| OUTPUT | 1 | WAIT | Wait |

## INTERFACE SIGNAL DESCRIPTION

**$\phi 1$, $\phi 2$** The Clock inputs provide basic timing generation for all internal operations. They are non-overlapping two phase, high level signals. All other inputs to the processor are TTL compatible.

**RESET** The Reset input initializes the processor by clearing the program counter, the instruction register, the interrupt enable flip-flop and the hold acknowledge flip-flop. The Reset signal should be active for at least three clock periods. The general registers are not cleared.

**HOLD** The Hold input allows an external signal to cause the processor to relinquish control over the address lines and the data bus. When Hold goes active, the processor completes its current operation, activates the Hlda output, and puts the 3-state address and data lines into their high-impedance state. The Holding device can then utilize the address and data busses without interference.

**READY** The Ready input synchronizes the processor with external units. When Ready is absent, indicating the external operation is not complete, the processor will enter the Wait state. It will remain in the Wait state until the clock cycle following the appearance of Ready.

**INT** The Interrupt input signal provides a mechanism for external devices to modify the instruction flow of the program in progress. Interrupt requests are handled efficiently with the vectored interrupt procedure and the general purpose stack. Interrupt processing is described in more detail on the next page.

**$D_0$-$D_7$** The Data Bus is comprised of 8 bidirectional signal lines for transferring data, instructions and status information between the processor and all external units.

**$A_0$-$A_{15}$** The Address Bus is comprised of 16 output signal lines used to address memory and peripheral devices.

**SYNC** The Sync output indicates the start of each processor cycle and the presence of processor status information on the data bus.

**DBIN** The Data Bus In output signal indicates that the bidirectional data bus is in the input mode and incoming data may be gated onto the Data Bus.

**WAIT** The Wait output indicates that the processor has entered the Wait state and is prepared to accept a Ready from the current external operation.

**$\overline{WR}$** The Write output indicates the validity of output on the data bus during a write operation.

**HLDA** The Hold Acknowledge output signal is a response to a Hold input. It indicates that processor activity has been suspended and the Address and Data Bus signals will enter their high impedance state.

**INTE** The Interrupt Enable output signal shows the status of the interrupt enable flip-flop, indicating whether or not the processor will accept interrupts.

## INSTRUCTION SET INTRODUCTION

The instructions executed by the Am9080A are variable length and may be one, two or three bytes long. The length is determined by the nature of the operation being performed and the addressing mode being used.

The instruction summary shows the number of successive memory bytes occupied by each instruction, the number of clock cycles required for the execution of the instruction, the binary coding of the first byte of each instruction, the mnemonic coding used by assemblers and a brief description of each operation. Some branch-type instructions have two execution times depending on whether the conditional branch is taken or not. Some fields in the binary code are labeled with alphabetic abbreviations. That shown as **vvv** is the address pointer used in the one-byte Call instruction (RST). Those shown as **ddd** or **sss** designate destination and source register fields that may be filled as follows:

| | |
|---|---|
| 111 | A register |
| 000 | B register |
| 001 | C register |
| 010 | D register |
| 011 | E register |
| 100 | H register |
| 101 | L register |
| 110 | Memory |

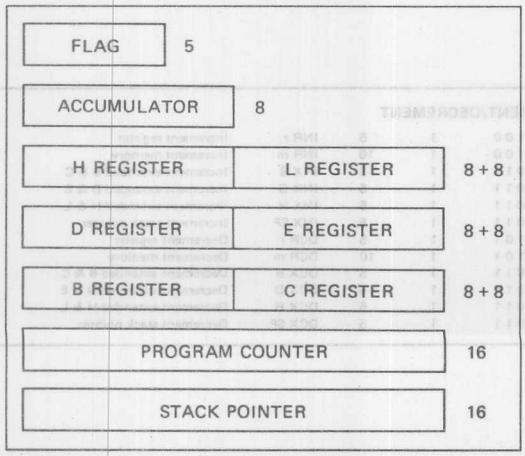
The register diagram shows the internal registers that are directly available to the programmer. The accumulator is the primary working register for the processor and is a specified or implied operand in many instructions. All I/O operations take place via the accumulator. Registers H, L, D, E, B and C may be used singly or in the indicated pairs. The H and L pair is the implied address pointer for many instructions.

The Flag register stores the program status bits used by the conditional branch instructions: carry, zero, sign and parity. The fifth flag bit is the intermediate carry bit. The flags and the accumulator can be stored on or retrieved from the stack with a single instruction. Bit positions in the flag register when pushed onto the stack (PUSH PSW) are:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| S | Z | 0 | CY1 | 0 | P | 1 | CY2 |

where S = sign, Z = zero, CY1 = intermediate carry, P = parity, CY2 = carry.

**REGISTER DIAGRAM**




During Sync time at the beginning of each instruction cycle the data bus contains operation status information that describes the machine cycle being executed. Positions for the status bits are:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MEMR | INP | M1 | OUT | HLTA | STK | $\overline{WO}$ | INTA |

**STATUS DEFINITION:**

**INTA** Interrupt Acknowledge. Occurs in response to an Interrupt input and indicates that the processor will be ready for an interrupt instruction on the data bus when DBIN goes true.

**$\overline{WO}$** Write or Output indicated when signal is low. When high, a Read or Input will occur.

**STK** Stack indicates that the content of the stack pointer is on the address bus.

**HLTA** Halt Acknowledge.

**OUT** Output instruction is being executed.

**M1** First instruction byte is being fetched.

**INP** Input instruction is being executed.

**MEMR** Memory Read operation.

### INTERRUPT PROCESSING

When the processor interrupt mechanism is enabled (INTE=1), interrupt signals from external devices will be recognized unless the processor is in the Hold State. In handling an interrupt, the processor will complete the execution of the current instruction, disable further interrupts and respond with INTA status instead of executing the next sequential instruction in the interrupted program.

The interrupting device should supply an instruction opcode to the processor during the next DBIN time after INTA status appears.

Any opcode may be used except XTHL. If the instruction supplied is a single byte instruction, it will be executed. (The usual single byte instruction utilized is RST.) If the interrupt instruction is two or three bytes long, the next one or two processor cycles, as indicated by the DBIN signal, should be used by the external device to supply the succeeding byte(s) of the interrupt instruction. Note that INTA status from the processor is not present during these operations.

If the interrupt instruction is not some form of CALL, it is executed normally by the processor except that the Program Counter is not incremented. The next instruction in the interrupted program is then fetched and executed. Notice that the interrupt mechanism must be re-enabled by the processor before another interrupt can occur.

If the interrupt instruction is some form of CALL, it is executed normally. The Program Counter is stored and control transferred to the interrupt service subroutine. This routine has responsibility for saving and restoring the machine state and for re-enabling interrupts if desired. When the interrupt service is complete, a RETURN instruction will transfer control back to the interrupted program.

7

# INSTRUCTION SET SUMMARY

## DATA TRANSFER

| Op Code \|7\|6\|5\|4\|3\|2\|1\|0 | No. of Bytes | Clock Cycles | Assembly Mnemonic | Instruction Description |
|---|---|---|---|---|
| 01dddsss | 1 | 5 | MOVr, r | Move register to register |
| 01110sss | 1 | 7 | MOVm, r | Move register to memory |
| 01ddd110 | 1 | 7 | MOVr, m | Move memory to register |
| 00ddd110 | 2 | 7 | MVI, r | Move to register, immediate |
| 00110110 | 2 | 10 | MVI, m | Move to memory, immediate |
| 00111010 | 3 | 13 | LDA | Load Acc, direct |
| 00001010 | 1 | 7 | LDAX B | Load Acc, indirect via B & C |
| 00011010 | 1 | 7 | LDAX D | Load Acc, indirect via D & E |
| C0101010 | 3 | 16 | LHLD | Load H & L, direct |
| 00100001 | 3 | 10 | LXI H | Load H & L, immediate |
| 00010001 | 3 | 10 | LXI D | Load D & E, immediate |
| 00000001 | 3 | 10 | LXI B | Load B & C, immediate |
| 00110001 | 3 | 10 | LXI SP | Load stack pointer, immediate |
| 00100010 | 3 | 16 | SHLD | Store H & L, direct |
| 00110010 | 3 | 13 | STA | Store Acc, direct |
| 00000010 | 1 | 7 | STAX B | Store Acc, indirect via B & C |
| 00010010 | 1 | 7 | STAX D | Store Acc, indirect via D & E |
| 11111001 | 1 | 5 | SPHL | Transfer H & L to stack pointer |
| 11101011 | 1 | 4 | XCHG | Exchange D & E with H & L |
| 11100011 | 1 | 18 | XTHL | Exchange top of stack with H & L |
| 11011011 | 2 | 10 | IN | Input to Acc |
| 11010011 | 2 | 10 | OUT | Output from Acc |

## CONTROL

| | | | | |
|---|---|---|---|---|
| 01110110 | 1 | 7 | HLT | Halt and enter wait state |
| 00110111 | 1 | 4 | STC | Set carry flag |
| 00111111 | 1 | 4 | CMC | Compliment carry flag |
| 11111011 | 1 | 4 | EI | Enable interrupts |
| 11110011 | 1 | 4 | DI | Disable interrupts |
| 00000000 | 1 | 4 | NOP | No operation |

## BRANCH

| | | | | |
|---|---|---|---|---|
| 11000011 | 3 | 10 | JMP | Jump unconditionally |
| 11011010 | 3 | 10 | JC | Jump on carry |
| 11010010 | 3 | 10 | JNC | Jump on no carry |
| 11001010 | 3 | 10 | JZ | Jump on zero |
| 11000010 | 3 | 10 | JNZ | Jump on not zero |
| 11110010 | 3 | 10 | JP | Jump on positive |
| 11111010 | 3 | 10 | JM | Jump on minus |
| 11101010 | 3 | 10 | JPE | Jump on parity even |
| 11100010 | 3 | 10 | JPO | Jump on parity odd |
| 11001101 | 3 | 17 | CALL | Call unconditionally |
| 11011100 | 3 | 17-11 | CC | Call on carry |
| 11010100 | 3 | 17-11 | CNC | Call on no carry |
| 11001100 | 3 | 17-11 | CZ | Call on zero |
| 11000100 | 3 | 17-11 | CNZ | Call on not zero |
| 11110100 | 3 | 17-11 | CP | Call on positive |
| 11111100 | 3 | 17-11 | CM | Call on minus |
| 11101100 | 3 | 17-11 | CPE | Call on parity even |
| 11100100 | 3 | 17-11 | CPO | Call on parity odd |
| 11001001 | 1 | 10 | RET | Return unconditionally |
| 11011000 | 1 | 11-5 | RC | Return on carry |
| 11010000 | 1 | 11-5 | RNC | Return on no carry |
| 11001000 | 1 | 11-5 | RZ | Return on zero |
| 11000000 | 1 | 11-5 | RNZ | Return on not zero |
| 11110000 | 1 | 11-5 | RP | Return on positive |
| 11111000 | 1 | 11-5 | RM | Return on minus |
| 11101000 | 1 | 11-5 | RPE | Return on parity even |
| 11100000 | 1 | 11-5 | RPO | Return on parity odd |
| 11101001 | 1 | 5 | PCHL | Jump unconditionally, indirect via H & L |
| 11VVV111 | 1 | 11 | RST | Restart |

## ARITHMETIC

| | | | | |
|---|---|---|---|---|
| 10000sss | 1 | 4 | ADDr | Add register to Acc |
| 10001sss | 1 | 4 | ADCr | Add with carry register to Acc |
| 10000110 | 1 | 7 | ADDm | Add memory to Acc |
| 10001110 | 1 | 7 | ADCm | Add with carry memory to Acc |
| 11000110 | 2 | 7 | ADI | Add to Acc, immediate |
| 11001110 | 2 | 7 | ACI | Add with carry to Acc, immediate |
| 00001001 | 1 | 10 | DAD B | Double add B & C to H & L |
| 00011001 | 1 | 10 | DAD D | Double add D & E to H & L |
| 00101001 | 1 | 10 | DAD H | Double add H & L to H & L |
| 00111001 | 1 | 10 | DAD SP | Double add stack pointer to H & L |
| 10010sss | 1 | 4 | SUBr | Subtract register from Acc |
| 10011sss | 1 | 4 | SBBr | Subtract with borrow register from Acc |
| 10010110 | 1 | 7 | SUBm | Subtract memory from Acc |
| 10011110 | 1 | 7 | SBBm | Subtract with borrow memory from Acc |
| 11010110 | 2 | 7 | SUI | Subtract from Acc, immediate |
| 11011110 | 2 | 7 | SBI | Subtract with borrow from Acc, immediate |
| 00100111 | 1 | 4 | DAA | Decimal adjust Acc |

## STACK OPERATIONS

| | | | | |
|---|---|---|---|---|
| 11000101 | 1 | 11 | PUSH B | Push registers B & C on stack |
| 11010101 | 1 | 11 | PUSH D | Push registers D & E on stack |
| 11100101 | 1 | 11 | PUSH H | Push registers H & L on stack |
| 11110101 | 1 | 11 | PUSH PSW | Push Acc and flags on stack |
| 11000001 | 1 | 10 | POP B | Pop registers B & C off stack |
| 11010001 | 1 | 10 | POP D | Pop registers D & E off stack |
| 11100001 | 1 | 10 | POP H | Pop registers H & L off stack |
| 11110001 | 1 | 10 | POP PSW | Pop Acc and flags off stack |

## LOGICAL

| | | | | |
|---|---|---|---|---|
| 10100sss | 1 | 4 | ANA r | And register with Acc |
| 10100110 | 1 | 7 | ANA m | And memory with Acc |
| 11100110 | 2 | 7 | ANI | And with Acc, immediate |
| 10101sss | 1 | 4 | XRA r | Exclusive or register with Acc |
| 10101110 | 1 | 7 | XRA m | Exclusive Or memory with Acc |
| 11101110 | 2 | 7 | XRI | Exclusive Or with Acc, immediate |
| 10110sss | 1 | 4 | ORA r | Inclusive Or register with Acc |
| 10110110 | 1 | 7 | ORA m | Inclusive Or memory with Acc |
| 11110110 | 2 | 7 | ORI | Inclusive Or with Acc, immediate |
| 10111sss | 1 | 4 | CMP r | Compare register with Acc |
| 10111110 | 1 | 7 | CMP m | Compare memory with Acc |
| 11111110 | 2 | 7 | CPI | Compare with Acc, immediate |
| 00101111 | 1 | 4 | CMA | Compliment Acc |
| 00000111 | 1 | 4 | RLC | Rotate Acc left |
| 00001111 | 1 | 4 | RRC | Rotate Acc right |
| 00010111 | 1 | 4 | RAL | Rotate Acc left through carry |
| 00011111 | 1 | 4 | RAR | Rotate Acc right through carry |

## INCREMENT/DECREMENT

| | | | | |
|---|---|---|---|---|
| 00ddd100 | 1 | 5 | INR r | Increment register |
| 00110100 | 1 | 10 | INR m | Increment memory |
| 00000011 | 1 | 5 | INX B | Increment extended B & C |
| 00010011 | 1 | 5 | INX D | Increment extended D & E |
| 00100011 | 1 | 5 | INX H | Increment extended H & L |
| 00110011 | 1 | 5 | INX SP | Increment stack pointer |
| 00ddd101 | 1 | 5 | DCR r | Decrement register |
| 00110101 | 1 | 10 | DCR m | Decrement memory |
| 00001011 | 1 | 5 | DCX B | Decrement extended B & C |
| 00011011 | 1 | 5 | DCX D | Decrement extended D & E |
| 00101011 | 1 | 5 | DCX H | Decrement extended H & L |
| 00111011 | 1 | 5 | DCX SP | Decrement stack pointer |

## MAXIMUM RATINGS (Above which useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| All Signal Voltages With Respect to $V_{BB}$ | −0.3V to +20V |
| All Supply Voltages With Respect to $V_{BB}$ | −0.3V to +20V |
| Power Dissipation | 1.5W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGE

| Part Number | $T_A$ | $V_{DD}$ | $V_{CC}$ | $V_{BB}$ | $V_{SS}$ |
|---|---|---|---|---|---|
| Am9080A-XCC<br>Am9080A-XPC<br>D8080A-X<br>P8080A-X | 0°C to +70°C | +12V ±5% | +5.0V ±5% | −5.0V ±5% | 0V |
| Am9080A-XDM<br>M8080A | −55°C to +125°C | +12V ±10% | +5.0V ±10% | −5.0V ±10% | 0V |

No signal or supply voltage should ever be greater than 0.3V more negative than $V_{BB}$.

## ELECTRICAL CHARACTERISTICS

over operating range (note 1)

| Parameters | Description | Test Conditions | | P8080A-X D8080A-X Min. | Typ. | Max. | Am9080A-XPC Am9080A-XCC Min. | Typ. | Max. | Am9080A-XDM M8080A Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW Voltage | | | −1.0 | | 0.8 | −1.0 | | 0.8 | −1.0 | | 0.8 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | | **3.3** | | $V_{CC}$+1 | **3.0** | | $V_{CC}$+1 | **3.0** | | $V_{CC}$+1 | Volts |
| $V_{ILC}$ | Input LOW Voltage, Clock | | | −1.0 | | 0.8 | −1.0 | | 0.8 | −1.0 | | 0.8 | Volts |
| $V_{IHC}$ | Input HIGH Voltage, Clock | A-4 | | | | | $V_{DD}$−2 | | $V_{DD}$+1 | | | | Volts |
| | | A-1 | | 9.0 | | $V_{DD}$+1 | 9.0 | | $V_{DD}$+1 | $V_{DD}$−2 | | $V_{DD}$+1 | |
| | | A-2 | | 9.0 | | $V_{DD}$+1 | 9.0 | | $V_{DD}$+1 | $V_{DD}$−2 | | $V_{DD}$+1 | |
| | | A | | 9.0 | | $V_{DD}$+1 | 9.0 | | $V_{DD}$+1 | $V_{DD}$−2 | | $V_{DD}$+1 | |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = **3.2mA** | | | | | | | **0.40** | | | **0.40** | Volts |
| | | $I_{OL}$ = **1.9mA** | | | | **0.45** | | | | | | | |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = −200μA | | | | | 3.7 | | | 3.7 | | | Volts |
| | | $I_{OH}$ = −150μA | | 3.7 | | | | | | | | | |
| $I_{DD}$(AV) | $V_{DD}$ Supply Current, Average | Operating, Minimum Clock Period | −55°C | | | | | | | | 50 | 80 | mA |
| | | | 0°C | | | 70 | | 40 | 70 | | 45 | 75 | |
| | | | 25°C | | 40 | | | 35 | 65 | | 40 | 70 | |
| | | | 70°C | | | | | 30 | 55 | | 35 | 60 | |
| | | | 125°C | | | | | | | | 30 | 50 | |
| $I_{CC}$(AV) | $V_{CC}$ Supply Current, Average | Operating, Minimum Clock Period | −55°C | | | | | | | | 45 | 60 | mA |
| | | | 0°C | | | 80 | | 35 | 50 | | 40 | 55 | |
| | | | 25°C | | 60 | | | 30 | 45 | | 35 | 50 | |
| | | | 70°C | | | | | 25 | 40 | | 30 | 45 | |
| | | | 125°C | | | | | | | | 25 | 40 | |
| $I_{BB}$(AV) | $V_{BB}$ Supply Current, Average | Operating, Minimum Clock Period | | | | 1.0 | | | 1.0 | | | 1.0 | mA |
| $I_{IL}$ | Input Leakage Current | (Note 4) | | | | ±10 | | | ±10 | | | ±10 | μA |
| $I_{CL}$ | Clock Leakage Current | $V_{SS} \leq V_{\phi} \leq V_{DD}$ | | | | ±10 | | | ±10 | | | ±10 | μA |
| $I_{DL}$ | Data Bus Current, | $V_{IN} \leq V_{SS}$ + 0.8V | | | | −100 | | | −100 | | | −100 | μA |
| | Input Mode (Note 2) | $V_{IN} \geq V_{SS}$ + 0.8V | | | | −2.0 | | | −2.0 | | | −2.0 | mA |
| $I_{FL}$ | Address and Data Bus | $V_{A/D} = V_{CC}$ | | | | 10 | | | 10 | | | 10 | μA |
| | Leakage in OFF State | $V_{A/D} = V_{SS}$ | | | | −100 | | | −100 | | | −100 | μA |

## CAPACITANCE

f = 1.0MHz, Inputs = 0V, $T_A$ = 25°C
$V_{DD} = V_{CC} = V_{SS}$ = 0V, $V_{BB}$ = −5.0V

| Parameters | Description | Typ. | Max. | Units |
|---|---|---|---|---|
| $C_{\phi}$ | Clock Input Capacitance | 12 | 25 | pF |
| $C_I$ | Input Capacitance | 4.0 | 10 | pF |
| $C_O$ | Output Capacitance | 8.0 | 20 | pF |
| $C_{I/O}$ | I/O Capacitance | 10 | 20 | pF |

7

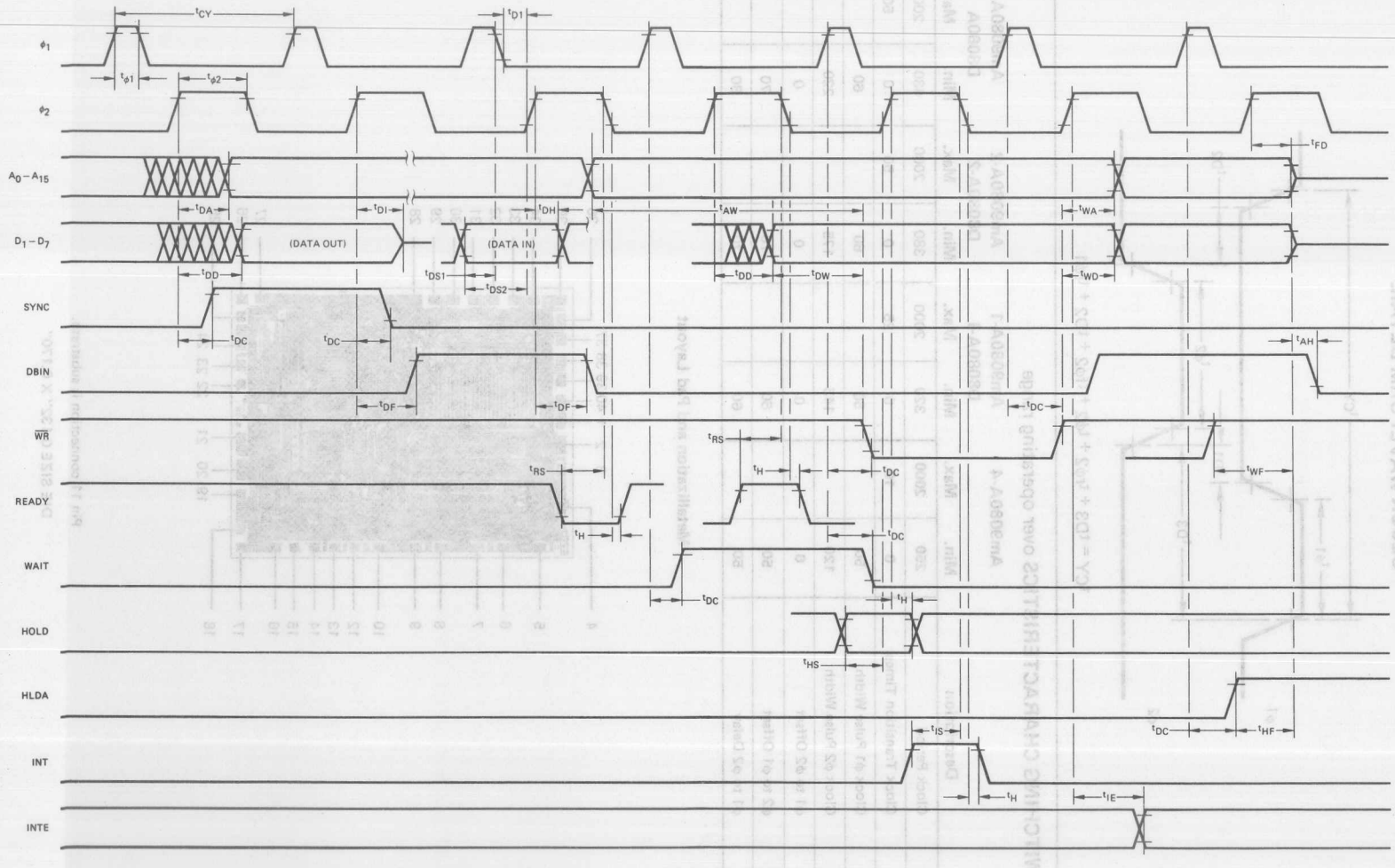
## SWITCHING CHARACTERISTICS over operating range (Note 9)

| Parameters | Description | Test Conditions | Am9080A-4 Min. | Am9080A-4 Max. | Am9080A-1 Min. | Am9080A-1 Max. | Am9080A-2 Min. | Am9080A-2 Max. | Am9080A Min. | Am9080A Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{DA}$ | Clock $\phi 2$ to Address Out Delay | Load Capacitance = 100pF | | 125 | | 150 | | 175 | | 200 | ns |
| $t_{DD}$ | Clock $\phi 2$ to Data Out Delay | | | 140 | | 180 | | 200 | | 220 | ns |
| $t_{DI}$ | Clock $\phi 2$ to Data Bus Input Mode Delay | (Note 5) | | $t_{DF}$ | | $t_{DF}$ | | $t_{DF}$ | | $t_{DF}$ | ns |
| $t_{DS1}$ | Data In to Clock $\phi 1$ Set-up Time | Both $t_{DS1}$ and $t_{DS2}$ must be satisfied | 10 | | 10 | | 20 | | 30 | | ns |
| $t_{DS2}$ | Data In to Clock $\phi 2$ Set-up Time | | 110 | | 120 | | 130 | | 150 | | ns |
| $t_{DC}$ | Clock to Control Output Delay | Load Capacitance = 50pF | | 100 | | 110 | | 120 | | 120 | ns |
| $t_{RS}$ | Ready to Clock $\phi 2$ Set-up Time | | 80 | | 90 | | 90 | | 120 | | ns |
| $t_H$ | Clock $\phi 2$ to Control Signal Hold Time | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{IS}$ | Interrupt to Clock $\phi 2$ Set-up Time | | 90 | | 100 | | 100 | | 120 | | ns |
| $t_{HS}$ | Hold to Clock $\phi 2$ Set-up Time | | 100 | | 120 | | 120 | | 140 | | ns |
| $t_{IE}$ | Clock $\phi 2$ to INTE Delay | Load Capacitance = 50pF | | 100 | | 200 | | 200 | | 200 | ns |
| $t_{FD}$ | Clock $\phi 2$ to Address/Data OFF Delay | | | 100 | | 120 | | 120 | | 120 | ns |
| $t_{DF}$ | Clock $\phi 2$ to DBIN Delay | Load Capacitance = 50pF | 25 | 110 | 25 | 130 | 25 | 140 | 25 | 140 | ns |
| $t_{DH}$ | Clock $\phi 2$ to Data In Hold Time | (Note 5) | – | – | – | – | – | – | – | – | ns |
| $t_{AW}$ | Address Valid to Write Delay | (Note 8) | – | – | – | – | – | – | – | – | ns |
| $t_{DW}$ | Output Data Valid to Write Delay | | – | – | – | – | – | – | – | – | ns |
| $t_{KA}$ | Address Valid to Write Increment | | | 90 | | 110 | | 130 | | 140 | ns |
| $t_{KD}$ | Output Data Valid to Write Increment | | | 130 | | 150 | | 170 | | 170 | ns |
| $t_{WA}$ | Write to Address Invalid Delay | | – | – | – | – | – | – | – | – | ns |
| $t_{WD}$ | Write to Output Data Invalid Delay | | – | – | – | – | – | – | – | – | ns |
| $t_{HF}$ | HLDA to Address/Data OFF Delay | | – | – | – | – | – | – | – | – | ns |
| $t_{WF}$ | Write to Address/Data OFF Delay | | – | – | – | – | – | – | – | – | ns |
| $t_{KH}$ | HLDA to Address/Data OFF Increment | | | 40 | | 50 | | 50 | | 50 | ns |
| $t_{AH}$ | DBIN to Address Hold Time | | 0 | | –20 | | –20 | | –20 | | ns |

**NOTES:**

1. Typical values are at $T_A = 25°C$, nominal supply voltages and nominal processing parameters.
2. Pull-up devices are connected to the Data Bus lines when the input signal is high during DBIN time. When switching the input from HIGH-to-LOW a transient current must be absorbed by the driving device until the input reaches a LOW level.
3. Timing reference levels –
   Clocks: HIGH = 8.0V, LOW = 1.0V
   Inputs: HIGH = 3.3V, LOW = 0.8V
   Outputs: HIGH = 2.0V, LOW = 0.8V
4. Control inputs impress currents on the driving signal during HIGH-to-LOW transitions. Values shown are for logic high or logic low levels. Peak current during transition is as much as 2.0mA.
5. Bus contention cannot occur and data hold times are adequate when DBIN is used to enable Data In. $t_{DH}$ is the smaller of 50ns or $t_{DF}$.
6. RESET should remain active for at least three clock periods.
7. With interrupts enabled, the interrupted instruction will be one with an interrupt input stable during the indicated interval of the last clock period of the preceding instruction. Additional synchronization not necessary.
8. $t_{AW} = 2\,t_{CY} - t_{D3} - t_r - t_{KA}$
   $t_{DW} = t_{CY} - t_{D3} - t_r - t_{KD}$
   For HLDA Off: $t_{WD} = t_{WA} = t_{D3} + t_r + 10ns$
   For HLDA On: $t_{WD} = t_{WA} = t_{WF}$
   $t_{HF} = t_{D3} + t_r - t_{KH}$
   $t_{WF} = t_{D3} + t_r - 10ns$
   $t_r = \phi 2$ rise time
9. The switching specifications listed for the Am9080A, Am9080A-2, Am9080A-1 meet or exceed the corresponding specifications for the C8080A, C8080A-2, C8080A-1.

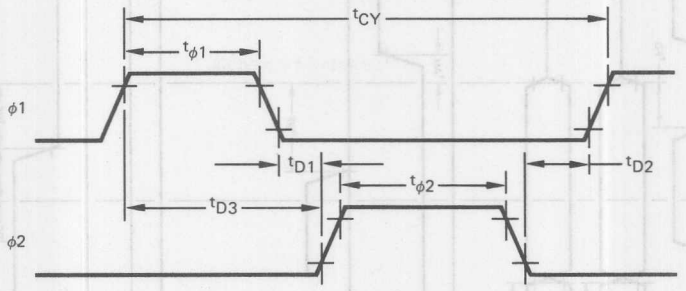
## SWITCHING WAVEFORMS SUMMARY




This chart presents relative timing waveform relationships and does not show actual processor operating cycles.

MOS-157

## CLOCK WAVEFORM DETAIL



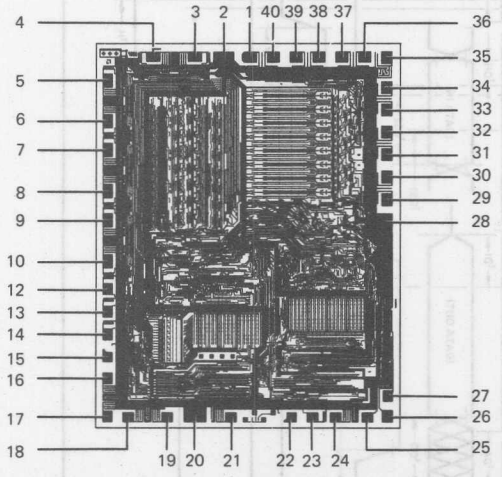

$t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1}$

MOS-158

## CLOCK SWITCHING CHARACTERISTICS over operating range

| Parameters | Description | Am9080A-4 Min. | Am9080A-4 Max. | Am9080A-1 D8080A-1 Min. | Am9080A-1 D8080A-1 Max. | Am9080A-2 D8080A-2 Min. | Am9080A-2 D8080A-2 Max. | Am9080A D8080A Min. | Am9080A D8080A Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{CY}$ | Clock Period | 250 | 2000 | 320 | 2000 | 380 | 2000 | 480 | 2000 | ns |
| $t_r$, $t_f$ | Clock Transition Times | 0 | 15 | 0 | 25 | 0 | 50 | 0 | 50 | ns |
| $t_{\phi1}$ | Clock $\phi1$ Pulse Width | 50 | | 50 | | 60 | | 60 | | ns |
| $t_{\phi2}$ | Clock $\phi2$ Pulse Width | 120 | | 145 | | 175 | | 220 | | ns |
| $t_{D1}$ | $\phi1$ to $\phi2$ Offset | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{D2}$ | $\phi2$ to $\phi1$ Offset | 50 | | 60 | | 70 | | 70 | | ns |
| $t_{D3}$ | $\phi1$ to $\phi2$ Delay | 50 | | 60 | | 70 | | 80 | | ns |

### Metallization and Pad Layout




Pin 11 connection is substrate.

DIE SIZE 0.132" X 0.170"

# Am8085A/Am8085A-2/Am9085ADM

## Single Chip 8-Bit N-Channel Microprocessor

### DISTINCTIVE CHARACTERISTICS

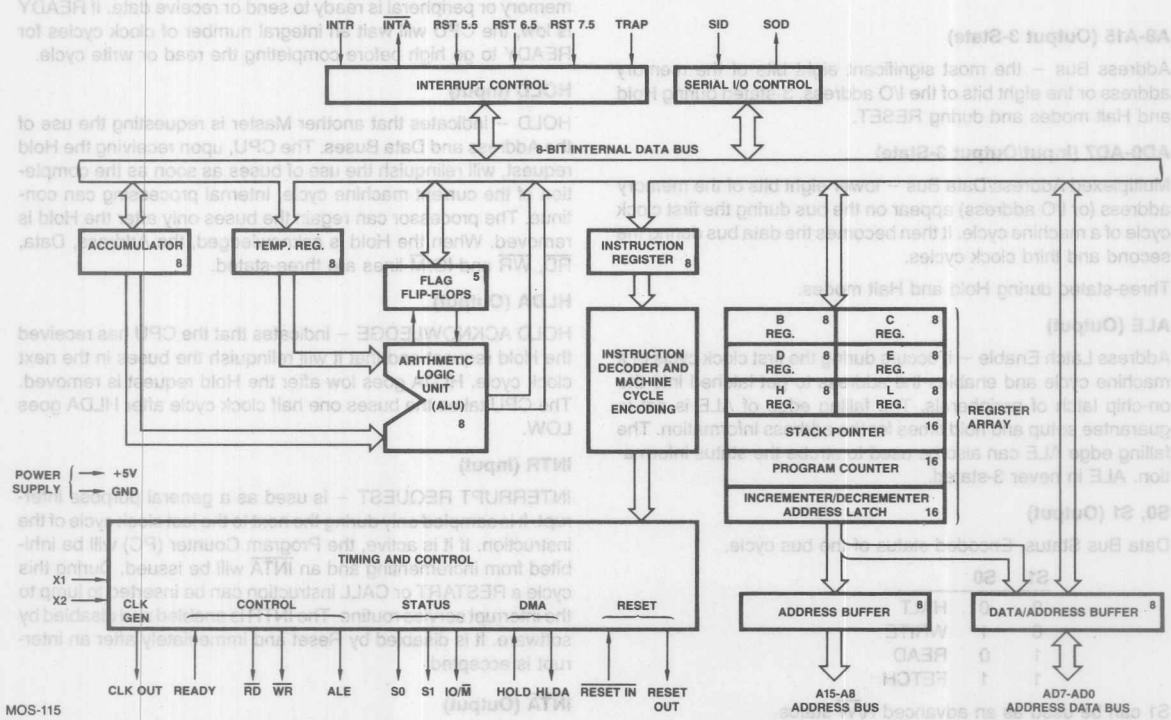
- Complete 8-bit parallel CPU
- On-chip system controller; advanced cycle status information available for large system control
- Four vectored interrupts (one is non-maskable)
- On-chip clock generator (with external crystal, LC or R/C network)
- Serial in/serial out port
- Decimal, binary and double precision arithmetic
- Direct addressing capability to 64K bytes of memory
- 1.3$\mu$s instruction cycle (Am8085A)
- 0.8$\mu$s instruction cycle (Am8085A-2)
- 100% software compatible with Am9080A
- Single +5V power supply
- 100% MIL-STD-883, Level C processing

### GENERAL DESCRIPTION

The Am8085A is a new generation, complete 8-bit parallel central processing unit (CPU). Its instruction set is 100% software compatible with the Am9080A microprocessor. Specifically, the Am8085A incorporates all of the features that the Am8224 (clock generator) and Am8228 (system controller) provided for the Am9080A. The Am8085A-2 is a faster version of the Am8085A.

The Am8085A uses a multiplexed Data Bus. The address is split between the 8-bit address bus and the 8-bit data bus. The on-chip address latches of Am8155/Am8355 memory products allows a direct interface with Am8085A. The Am8085A components, including various timing compatible support chips, allow system speed optimization.

### BLOCK DIAGRAM

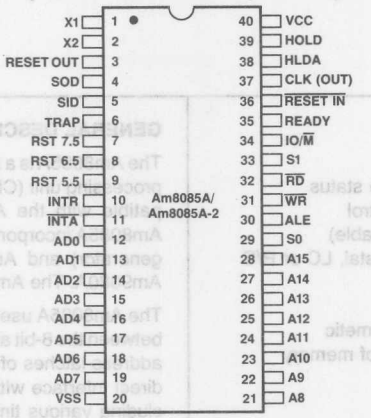



### ORDERING INFORMATION

| Package Type | Temperature Range | Maximum Clock Frequency | |
|---|---|---|---|
| | | 3MHz | 5MHz |
| Molded DIP | 0°C ≤ $T_A$ ≤ 70°C | AM8085APC/P8085A<br>AM8085ADC/D8085A | AM8085A-2PC/P8085A-2<br>AM8085A-2DC/D8085A-2 |
| Hermetic DIP* | | AM8085ACC/C8085A | AM8085A-2CC/C8085A-2 |
| Hermetic DIP | −55°C ≤ $T_A$ ≤ +125°C | AM9085ADM | |

*Hermetic = Ceramic = DC = CC = D-40-1.

**CONNECTION DIAGRAM**
**Top View**




Note: Pin 1 is marked for orientation.

**Figure 1.** MOS-116

## Am8085A FUNCTIONAL PIN DEFINITION

The following describes the function of each pin:

### A8-A15 (Output 3-State)

Address Bus – the most significant eight bits of the memory address or the eight bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.

### AD0-AD7 (Input/Output 3-State)

Multiplexed Address/Data Bus – lower eight bits of the memory address (or I/O address) appear on the bus during the first clock cycle of a machine cycle. It then becomes the data bus during the second and third clock cycles.

Three-stated during Hold and Halt modes.

### ALE (Output)

Address Latch Enable – it occurs during the first clock cycle of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge ALE can also be used to strobe the status information. ALE in never 3-stated.

### S0, S1 (Output)

Data Bus Status. Encoded status of the bus cycle.

| S1 | S0 | |
|---|---|---|
| 0 | 0 | HALT |
| 0 | 1 | WRITE |
| 1 | 0 | READ |
| 1 | 1 | FETCH |

S1 can be used as an advanced R/$\overline{W}$ status.

### $\overline{RD}$ (Output 3-State)

READ – A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer. Three-stated during Hold and Halt and during RESET.

### $\overline{WR}$ (Output 3-State)

WRITE – A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. Three-stated during Hold and Halt modes.

### READY (Input)

If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the CPU will wait an integral number of clock cycles for READY to go high before completing the read or write cycle.

### HOLD (Input)

HOLD – indicates that another Master is requesting the use of the Address and Data Buses. The CPU, upon receiving the Hold request, will relinquish the use of buses as soon as the completion of the current machine cycle. Internal processing can continue. The processor can regain the buses only after the Hold is removed. When the Hold is acknowledged, the Address, Data, $\overline{RD}$, $\overline{WR}$ and IO/$\overline{M}$ lines are three-stated.

### HLDA (Output)

HOLD ACKNOWLEDGE – indicates that the CPU has received the Hold request and that it will relinquish the buses in the next clock cycle. HLDA goes low after the Hold request is removed. The CPU takes the buses one half clock cycle after HLDA goes LOW.

### INTR (Input)

INTERRUPT REQUEST – is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of the instruction. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.

### $\overline{INTA}$ (Output)

INTERRUPT ACKNOWLEDGE – is used instead of (and has the same timing as) $\overline{RD}$ during the Instruction cycle after an INTR is accepted. It can be used to activate the Am9519 Interrupt chip or some other interrupt port.

RST 5.5
RST 6.5
RST 7.5
} (Inputs)

RESTART INTERRUPTS – these three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted.

RST 7.5 → Highest Priority
RST 6.5
RST 5.5 → Lowest Priority

The priority of these interrupts is ordered as shown above. These interrupts have a higher priority than the INTR. However they may be individually masked out using the SIM instructions.

**TRAP (Input)**

Trap interrupt is a non-maskable restart interrupt. It is recognized at the same time as INTR. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt.

**$\overline{\text{RESET IN}}$ (Input)**

Reset sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. None of the other flags or registers (except the instruction register) are affected. The CPU is held in the reset condition as long as RESET is applied.

**RESET OUT (Output)**

Indicates CPU is being reset. Can be used as a system RESET. The signal is synchronized to the processor clock.

**X1, X2 (Input)**

Crystal, LC or R/C network connections to set the internal clock generator. X1 can also be an external clock input instead of a crystal. The input frequency is divided by 2 to give the internal operating frequency.

**CLK (Output)**

Clock Output for use as a system clock when a crystal or R/C network is used as an input to the CPU. The period of CLK is twice the X1, X2 input period.

**IO/$\overline{\text{M}}$ (Output)**

IO/$\overline{\text{M}}$ indicates whether the Read/Write is to memory or I/O. 3-stated during Hold and Halt modes.

**SID (Input)**

Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.

**SOD (Output)**

Serial output data line. The output SOD is set or reset as specified by the SIM instruction.

**VCC**

+5 volt supply.

**VSS**

Ground reference.

## FUNCTIONAL DESCRIPTION

The Am8085A is a complete 8-bit parallel central processor. It is designed with N-channel depletion loads and requires a single +5 volt supply. Its basic clock speed is 3MHz (5MHz: Am8085A-2) thus improving on the present Am9080's performance with higher system speed. Also it is designed to fit into a minimum system of three ICs: The CPU, a RAM/IO, and a ROM or PROM/IO chip.

The Am8085A uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first cycle the address is sent out. The lower eight bits are latched into the peripherals by the Address Latch Enable (ALE). During the rest of the machine cycle the Data Bus is used for memory or I/O data.

The Am8085A provides $\overline{\text{RD}}$, $\overline{\text{WR}}$ and IO/$\overline{\text{Memory}}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{\text{INTA}}$) is also provided. Hold, Ready and all Interrupts are synchronized. The Am8085A also provides serial input data (SID) and serial output data (SOD) lines for simple serial interface.

In addition to these features, the Am8085A has three maskable, restart interrupts and one non-maskable trap interrupt.

**Am8085A vs. Am8080A**

The Am8085A includes the following features on-chip in addition to all of the Am9080A functions.

a. Internal clock generator
b. Clock output
c. Fully synchronized Ready
d. Schmitt action on $\overline{\text{RESET IN}}$
e. RESET OUT pin
f. $\overline{\text{RD}}$, $\overline{\text{WR}}$ and IO/$\overline{\text{M}}$ Bus Control Signals
g. Encoded Status information
h. Multiplexed Address and Data
i. Direct Restarts and non-maskable Interrupt
j. Serial Input/Output lines

The internal clock generator requires an external crystal or R/C network. It will oscillate at twice the basic CPU operating frequency. A 50% duty cycle, two phase, non-overlapping clock is generated from this oscillator internally and one phase of the clock ($\phi$2) is available as an external clock. The Am8085A directly provides the external RDY synchronization previously provided by the Am8224. The $\overline{\text{RESET IN}}$ input is provided with a Schmitt action input so that power-on reset only requires a resistor and capacitor. RESET OUT is provided for System RESET.

The Am8085A provides $\overline{\text{RD}}$, $\overline{\text{WR}}$ and IO/$\overline{\text{M}}$ signals for Bus control. An $\overline{\text{INTA}}$ which was previously provided by the Am8228 in Am9080A systems is also included in Am8085A.

## STATUS INFORMATION

Status information is directly available from the Am8085A. ALE serves as a status strobe. The status is partially encoded and provides the user with advanced timing of the type of bus transfer being done. IO/$\overline{\text{M}}$ cycle status signal is provided directly also. Decoded S0, S1 carries the following status information:

**MACHINE CYCLE STATUS**

| IO/$\overline{\text{M}}$ | S1 | S0 | Status |
|---|---|---|---|
| 0 | 0 | 1 | Memory write |
| 0 | 1 | 0 | Memory read |
| 1 | 0 | 1 | I/O write |
| 1 | 1 | 0 | I/O read |
| 0 | 1 | 1 | Opcode fetch |
| 1 | 1 | 1 | Interrupt Acknowledge |
| • | 0 | 0 | Halt |
| • | X | X | Hold |
| • | X | X | Reset |

• = 3-state (high impedance)
X = unspecified

S1 can be interpreted as R/$\overline{\text{W}}$ in all bus transfers.

In the Am8085A the eight LSB of address are multiplexed with the data instead of status. The ALE line is used as a strobe to enter the lower half of the address into the memory or peripheral address latch. This also frees extra pins for expanded interrupt capability.

7

The Am8085A/Am8085A-2 has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5 and TRAP. INTR is identical in function to the Am8080A INT. Each of three RESTART inputs, 5.5, 6.5, 7.5, has programmable mask. TRAP is also a RESTART interrupt except it is non-maskable.

The three RESTART interrupts cause the internal execution of RST (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The nonmaskable TRAP causes the internal execution of a RST independent of the state of the interrupt enable or masks.

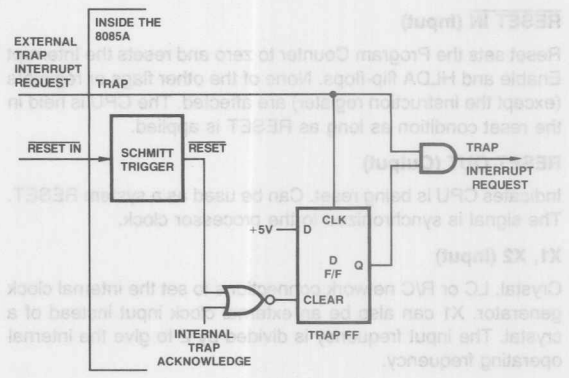
| Name | RESTART Address (Hex) |
|---|---|
| TRAP | $24_{16}$ |
| RST 5.5 | $2C_{16}$ |
| RST 6.5 | $34_{16}$ |
| RST 7.5 | $3C_{16}$ |

There are two different types of inputs in the restart interrupts. RST 5.5 and RST 6.5 are high level-sensitive like INTR (and INT on the Am8080A) and are recognized with the same timing as INTR. RST 7.5 is rising edge-sensitive. For RST 7.5, only a pulse is required to set an internal flip-flop which generates the internal interrupt request. The RST 7.5 request flip-flop remains set until the request is serviced. Then it is reset automatically. This flip-flop may also be reset by using the SIM instruction or by issuing a RESET IN to the Am8085A. The RST 7.5 internal flip-flop will be set by a pulse on the RST 7.5 pin even when the RST 7.5 interrupt is masked out.

The status of the three RST interrupt masks can only be affected by the SIM instruction and RESET IN.

The interrupts are arranged in a fixed priority that determines which interrupt is to be recognized if more than one is pending as follows: TRAP – highest priority, RST 7.5, RST 6.5, RST 5.5, INTR – lowest priority. This priority scheme does not take into account the priority of a routine that was started by a higher priority interrupt. RST 5.5 can interrupt a RST 7.5 routine if the interrupts were re-enabled before the end of the RST 7.5 routine.

as any other interrupt but has the highest priority. It is not affected by any flag or mask. The TRAP input is both edge and level sensitive. The TRAP input must go high and remain high to be acknowledged, but will not be recognized again until it goes low, then high again. This avoids any false triggering due to noise or logic glitches. The following diagram illustrates the TRAP interrupt request circuitry within the Am8085A.




MOS-117

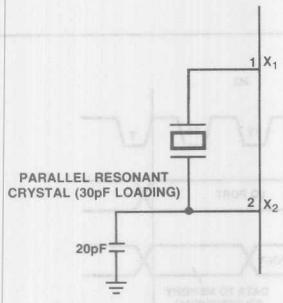
Note that the servicing of any interrupt (TRAP, RST 7.5, RST 6.5, RST 5.5, INTR) disables all future interrupts (except TRAPs) until an EI instruction is executed.

The TRAP interrupt is special in that it preserves the previous interrupt enable status. Performing the first RIM instruction following a TRAP interrupt allows you to determine whether interrupts were enabled or disabled prior to the TRAP. All subsequent RIM instructions provide current interrupt enable status.

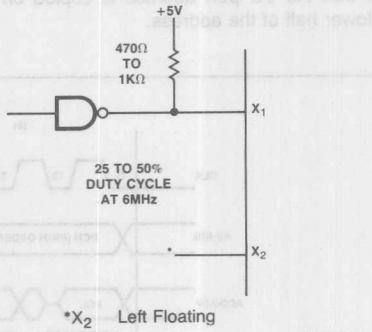
The serial I/O system is also controlled by the RIM and SIM instructions. SID is read by RIM, and SIM sets the SOD data.

## DRIVING THE X1 an X2 INPUTS

The user may drive the X1 and X2 inputs of the Am8085A or Am8085A-2 with a crystal, an external clock source or an R/C network as shown below. The driving frequency must be twice the desired internal operating frequency (the Am8085A would require a 6MHz crystal for 3MHz internal operation).

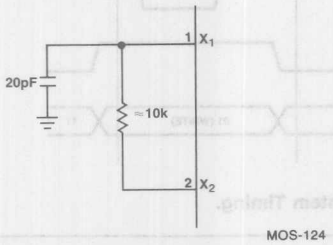



**1-6 MHz Input Frequency**

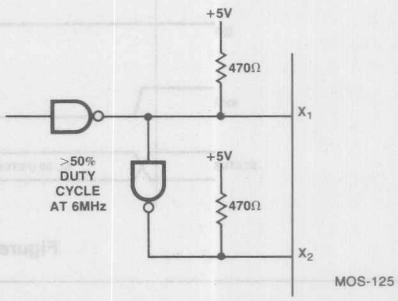



**1-6 MHz Input Frequency**

The 20pF capacitor is required to guarantee oscillation at the proper frequency during system startup.




**≈3 MHz Input Frequency**




**≈6 MHz Input Frequency**

RC Mode causes a large drift in clock frequency because of the variation in on-chip timing generation parameters. Use of RC Mode should be limited to an application which can tolerate a wide frequency variation.

Note: Duty cycle refers to the percentage of the clock input cycle when $X_1$ is high.

**Figure 2. Driving the Clock Inputs (X1 and X2) of Am8085A.**

## GENERATING Am8085A WAIT STATE

The following circuit may be used to insert one WAIT state in each Am8085A machine cycle.

The D flip-flops should be chosen such that

- CLK is rising edge triggered
- CLEAR is low-level active.

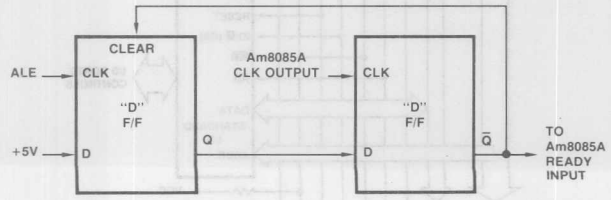



**Figure 3. Generation of a Wait State for Am8085A CPU.**

MOS-126

7

## BASIC SYSTEM TIMING

The Am8085A has a multiplexed Data Bus. ALE is used as a strobe to sample the lower 8 bits of address on the Data Bus. Figure 2 shows an instruction fetch, memory read and I/O write cycle (OUT). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address.

As in the Am9080A, the READY line is used to extend the read and write pulse lengths so that the Am8085A can be used with slow memory. Hold causes the CPU to relinquish the bus when it is through with it by floating the Address and Data Buses.

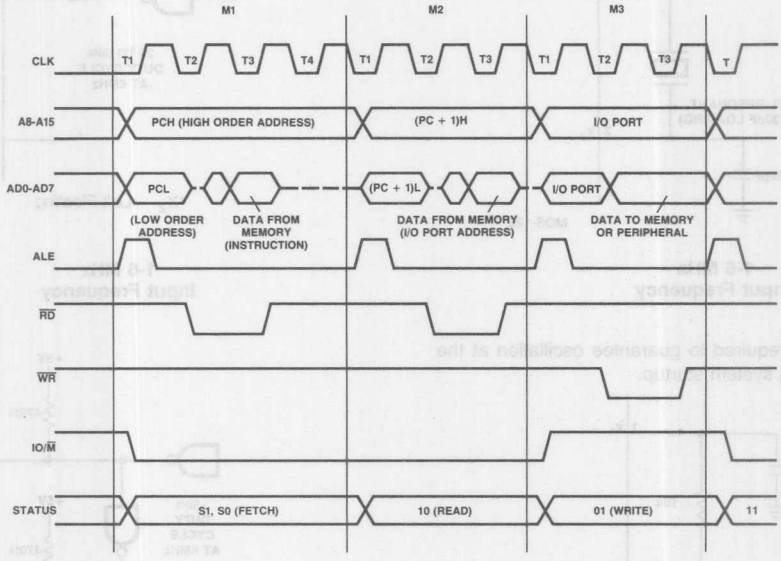



**Figure 4. Am8085A Basic System Timing.** MOS-118

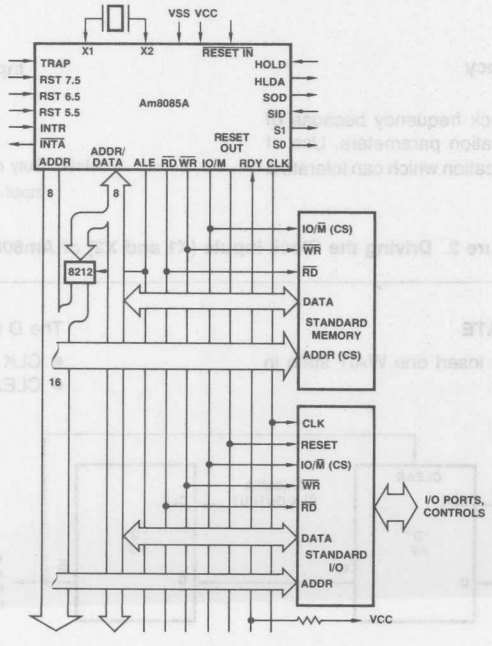



**Figure 5. System Using Standard Memories.** MOS-121

## MAXIMUM RATINGS above which useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| $V_{CC}$ with Respect to $V_{SS}$ | −0.5V to +7.0V |
| All Signal Voltages with Respect to $V_{SS}$ | −0.5V to +7.0V |
| Power Dissipation | 1.5W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGE

| Part Number | $T_A$ | VCC | VSS |
|---|---|---|---|
| Am8085A/Am8085A-2 | 0 to 70°C | +5.0V ±5% | 0V |
| Am9085ADM | −55 to +125°C | +5.0V ±10% | 0V |

## DC CHARACTERISTICS

| | | | Am8085A/Am8085A-2 | | Am9085ADM | | |
|---|---|---|---|---|---|---|---|
| Parameter | Description | Test Conditions | Min | Max | Min | Max | Units |
| VIL | Input Low Voltage | | −0.5 | +0.8 | −0.5 | +0.8 | Volts |
| VIH | Input High Voltage | | 2.0 | VCC+0.5 | 2.2 | VCC+0.5 | Volts |
| VOL | Output Low Voltage | IOL = 2.0mA | | 0.45 | | 0.45* | Volts |
| VOH | Output High Voltage | IOH = −400μA | 2.4 | | 2.4 | | Volts |
| ICC | Power Supply Current | | | 170 | | 200 | mA |
| IIL† | Input Leakage | VIN = VCC | | ±10 | | ±10 | μA |
| ILO | Output Leakage | 0.45V ≤ VOUT ≤ VCC | | ±10 | | ±10 | μA |
| VILR | Input Low Level, RESET | | −0.5 | +0.8 | −0.5 | +0.8 | Volts |
| VIHR | Input High Level, RESET | | 2.4 | VCC+0.5 | 2.4 | VCC+0.5 | Volts |
| VHY | Hysteresis, RESET | | 0.25 | | 0.25 | | Volts |

*IOL = 1.6mA

†Except Pin 1 and Pin 2.

7

## AC CHARACTERISTICS

| Parameters | Description | | Am8085A Min | Am8085A Max | Am8085A-2 Min | Am8085A-2 Max | Am9085ADM Min | Am9085ADM Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| tCYC | CLK Cycle Period | | 320 | 2000 | 200 | 2000 | 320 | 2000 | ns |
| tr, tf | CLK Rise and Fall Time | | | 30 | | 30 | | 30 | ns |
| tAL | A8-A15 Valid before Trailing Edge of ALE (Note 1) | | 115 | | 50 | | 115 | | ns |
| tACL | A0-A7 Valid to Leading Edge of Control | | 240 | | 115 | | 240 | | ns |
| tXKR | X1 Rising to CLK Rising | | 30 | 120 | 30 | 100 | 30 | 120 | ns |
| tXKF | X1 Rising to CLK Falling | | 30 | 150 | 30 | 110 | 30 | 150 | ns |
| t1 | CLK Low Time | Standard 150pF Loading | 80 | | 40 | | 80 | | ns |
| | | Lightly Loaded (Note 8) | 100 | | | | 100 | | |
| t2 | CLK High Time | Standard 150pF Loading | 120 | | 70 | | 120 | | ns |
| | | Lightly Loaded (Note 8) | 150 | | | | 150 | | |
| tALL | A0-A7 Valid to Leading Edge of Control | | 90 | | 50 | | 90 | | ns |
| tLRY | ALE to READY Stable | | | 110 | | 30 | | 110 | ns |
| tLA | Address Hold Time after ALE | | 100 | | 50 | | 100 | | ns |
| tLL | ALE Width | | 140 | | 80 | | 140 | | ns |
| tLCK | ALE Low During CLK High | | 100 | | 50 | | 100 | | ns |
| tLC | Trailing Edge of ALE to Leading Edge of Control | | 130 | | 60 | | 130 | | ns |
| tAFR | Address Float after Leading Edge of $\overline{READ}$ ($\overline{INTA}$) | | | 0 | | 0 | | 0 | ns |
| tAD | Valid Address to Valid Data In | | | 575 | | 350 | | 575 | ns |
| tRD | $\overline{READ}$ (or $\overline{INTA}$) to Valid Data | | | 300 | | 150 | | 300 | ns |
| tRDH | Data Hold Time after $\overline{READ}$ ($\overline{INTA}$) (Note 7) | | 0 | | 0 | | 0 | | ns |
| tRAE | Trailing Edge of $\overline{READ}$ to Re-Enabling of Address | | 150 | | 90 | | 150 | | ns |
| tCA | Address (A8-A15) Valid after Control | | 120 | | 60 | | 120 | | ns |
| tDW | Data Valid to Trailing Edge of $\overline{WRITE}$ | | 420 | | 230 | | 420 | | ns |
| tWD | Data Valid after Trailing Edge of $\overline{WRITE}$ | | 100 | | 60 | | 100 | | ns |
| tCC | Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$) | | 400 | | 230 | | 400 | | ns |
| tCL | Trailing Edge of Control to Leading Edge of ALE | | 50 | | 25 | | 50 | | ns |
| tARY | READY Valid from Address Valid | | | 220 | | 100 | | 220 | ns |
| tRYS | READY Setup Time to Leading Edge of CLK | | 110 | | 100 | | 110 | | ns |
| tRYH | READY Hold Time | | 0 | | 0 | | 0 | | ns |
| tHACK | HLDA Valid to Trailing Edge of CLK | | 110 | | 40 | | 110 | | ns |
| tHABF | Bus Float after HLDA | | | 210 | | 150 | | 210 | ns |
| tHABE | HLDA to Bus Enable | | | 210 | | 150 | | 210 | ns |
| tLDR | ALE to Valid Data In | | | 460 | | 270 | | 460 | ns |
| tRV | Control Trailing Edge to Leading Edge of Next Control | | 400 | | 220 | | 400 | | ns |
| tAC | A8-A15 Valid to Leading Edge of Control (Note 1) | | 270 | | 115 | | 270 | | ns |
| tHDS | HOLD Setup Time to Trailing Edge of CLK | | 170 | | 120 | | 170 | | ns |
| tHDH | HOLD Hold Time | | 0 | | 0 | | 0 | | ns |
| tINS | INTR Setup Time to Falling Edge of CLK, also RST and TRAP | | 160 | | 150 | | 160 | | ns |
| tINH | INTR Hold Time | | 0 | | 0 | | 0 | | ns |

Notes:
1. A8-A15 Address Specs apply to IO/$\overline{M}$, S0 and S1. Except A8-A15 are undefined during T4-T6 of OF cycle whereas IO/$\overline{M}$, S0 and S1 are stable.
2. Test Conditions: tCYC = 320ns (Am8085A)/200ns (Am8085A-2); CL = 150pF.
3. For all output timing where CL = 150pF use the following correction factors.
   25pF ≤ CL < 150pF: −.10ns/pF
   150pF < CL ≤ 300pF: +.30ns/pF
4. Output timings are measured with purely capacitive load.
5. All timings are measured at output voltage VL = 0.8V, VH = 2.0V and 1.5V with 20ns rise and fall time on inputs.
6. To calculate timing specifications at other values of tCYC use the table on Page 7-21.
7. Data Hold Time is guaranteed under all loading conditions.
8. Loading equivalent to 50pF +1 TTL input.

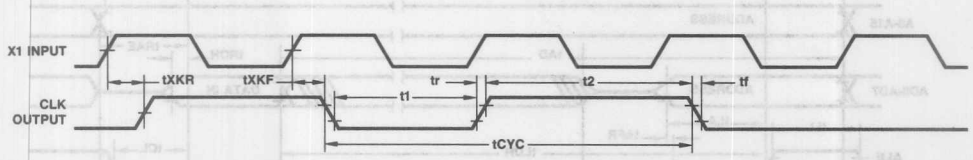
## BUS TIMING SPECIFICATION AS A TCYC DEPENDENT

| Parameters | Description | Am8085A/Am9085ADM Min | Am8085A/Am9085ADM Max | Am8085A-2 Min | Am8085A-2 Max | Units |
|---|---|---|---|---|---|---|
| tAL | Address Valid before Trailing Edge of ALE | (1/2)T−45 | | (1/2)T−50 | | ns |
| tLA | Address Hold Time after ALE | (1/2)T−60 | | (1/2)T−50 | | ns |
| tLL | ALE Width | (1/2)T−20 | | (1/2)T−20 | | ns |
| tLCK | ALE Low During CLK High | (1/2)T−60 | | (1/2)T−50 | | ns |
| tLC | Trailing Edge of ALE to Leading Edge of Control | (1/2)T−30 | | (1/2)T−40 | | ns |
| tAD | Valid Address to Valid Data In | | (5/2+N)T−225 | | (5/2+N)T−150 | ns |
| tRD | READ (or INTA) to Valid Data | | (3/2+N)T−180 | | (3/2+N)T−150 | ns |
| tRAE | Trailing Edge of READ to Re-Enabling of Address | (1/2)T−10 | | (1/2)T−10 | | ns |
| tCA | Address (A8-A15) Valid after Control | (1/2)T−40 | | (1/2)T−40 | | ns |
| tDW | Data Valid to Trailing Edge of WRITE | (3/2+N)T−60 | | (3/2+N)T−70 | | ns |
| tWD | Data Valid after Trailing Edge of WRITE | (1/2)T−60 | | (1/2)T−40 | | ns |
| tWDL | Leading Edge of WRITE to Data Valid | | 40 | | 40 | ns |
| tCC | Width of Control LOW (RD, WR, INTA) | (3/2+N)T−80 | | (3/2+N)T−70 | | ns |
| tCL | Trailing Edge of Control to Leading Edge of ALE | (1/2)T−110 | | (1/2)T−75 | | ns |
| tARY | READY Valid from Address Valid | | (3/2)T−260 | | (3/2)T−200 | ns |
| tHACK | HLDA Valid to Trailing Edge of CLK | (1/2)T−50 | | (1/2)T−60 | | ns |
| tHABF | Bus Float after HLDA | | (1/2)T+50 | | (1/2)T+50 | ns |
| tHABE | HLDA to Bus Enable | | (1/2)T+50 | | (1/2)T+50 | ns |
| tAC | Address Valid to Leading Edge of Control | (2/2)T−50 | | (2/2)T−85 | | ns |
| t1 | CLK Low Time | (1/2)T−80 | | (1/2)T−60 | | ns |
| t2 | CLK High Time | (1/2)T−40 | | (1/2)T−30 | | ns |
| tRV | Control Trailing Edge to Leading Edge of Next Control | (3/2)T−80 | | (3/2)T−80 | | ns |
| tLDR | | | (4/2)T−180 | | (4/2)T−130 | ns |
| tLDW | Trailing Edge of ALE to Valid Data During WRITE | | 200 | | 200 | ns |

Note: N is equal to the total WAIT states.
T = tCYC.

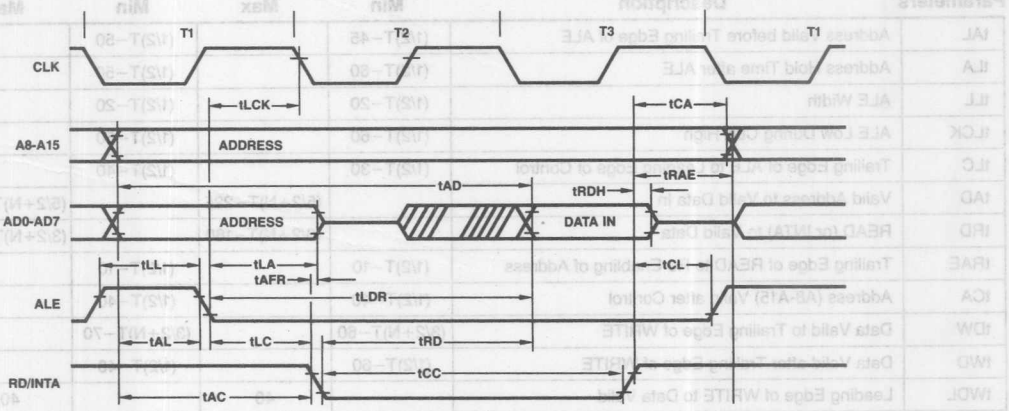
7

### CLOCK TIMING WAVEFORM

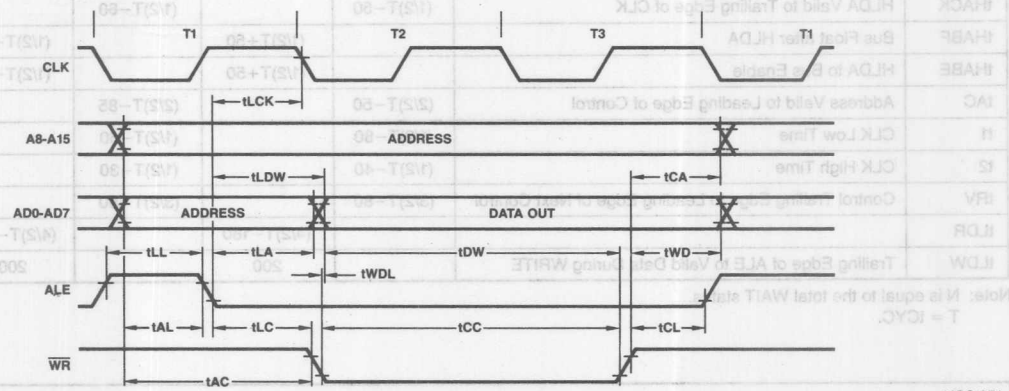



MOS-269

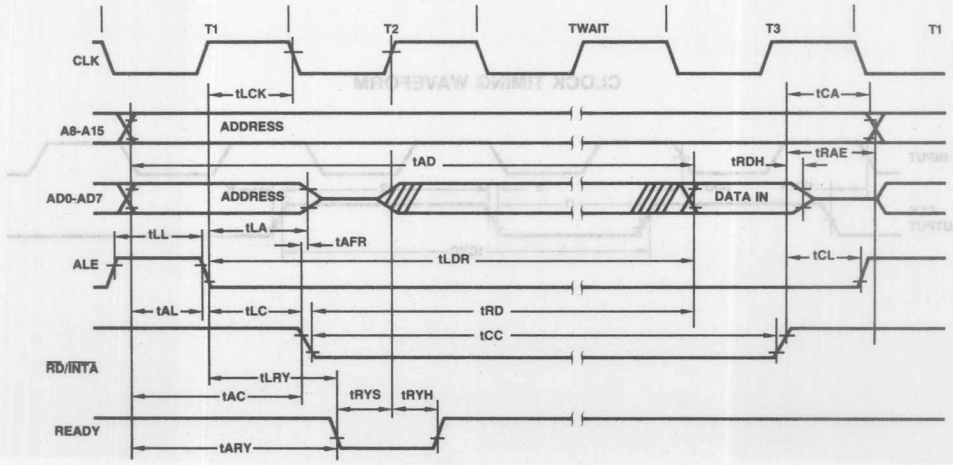
## READ OPERATION




## WRITE OPERATION




## TYPICAL READ OPERATION WITH WAIT CYCLE




Same READY timing applies to WRITE operation.

MOS-272

**Figure 6. Am8085A/Am8085A-2 Bus Timing**

## HOLD OPERATION

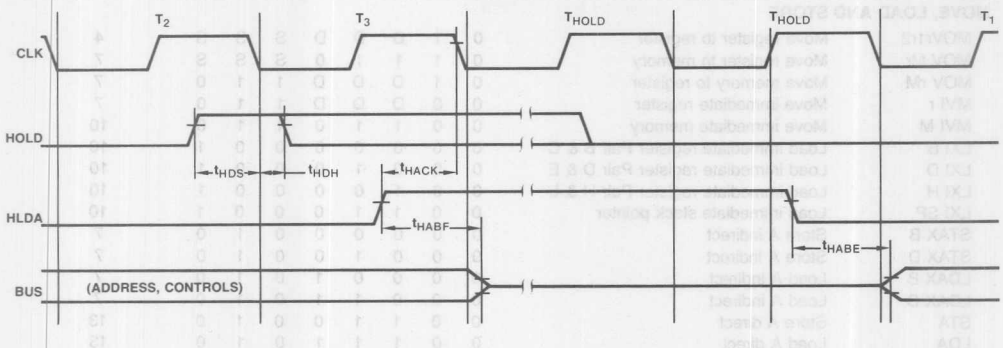



Figure 7. Am8085A Hold Timing.

MOS-130

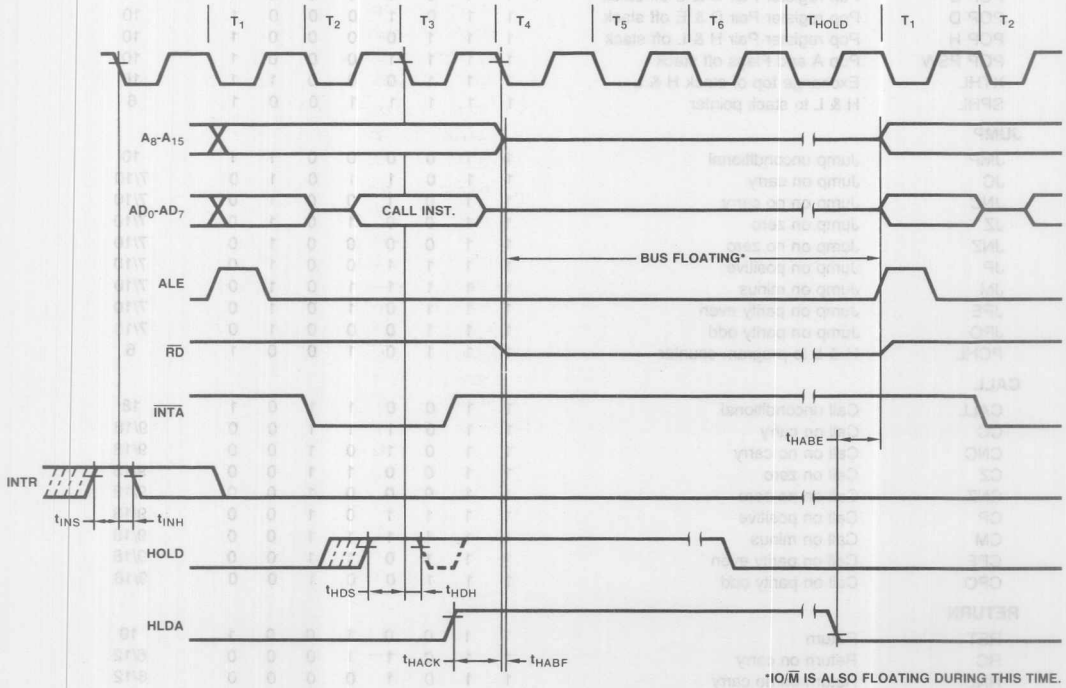



Figure 8. Am8085A Interrupt and Hold Timing.

MOS-131

7

| Mnemonic* | Description | Instruction Code (Note 1) D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Clock Cycles (Note 2) |
|---|---|---|---|---|---|---|---|---|---|---|
| **MOVE, LOAD AND STORE** | | | | | | | | | | |
| MOVr1r2 | Move register to register | 0 | 1 | D | D | D | S | S | S | 4 |
| MOV Mr | Move register to memory | 0 | 1 | 1 | 1 | 0 | S | S | S | 7 |
| MOV rM | Move memory to register | 0 | 1 | D | D | D | 1 | 1 | 0 | 7 |
| MVI r | Move immediate register | 0 | 0 | D | D | D | 1 | 1 | 0 | 7 |
| MVI M | Move immediate memory | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 10 |
| LXI B | Load immediate register Pair B & C | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 10 |
| LXI D | Load immediate register Pair D & E | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 10 |
| LXI H | Load immediate register Pair H & L | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 10 |
| LXI SP | Load immediate stack pointer | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 10 |
| STAX B | Store A indirect | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 7 |
| STAX D | Store A indirect | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 7 |
| LDAX B | Load A indirect | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 7 |
| LDAX D | Load A indirect | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 7 |
| STA | Store A direct | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 13 |
| LDA | Load A direct | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 13 |
| SHLD | Store H & L direct | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 16 |
| LHLD | Load H & L direct | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 16 |
| XCHG | Exchange D & E, H & L Registers | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 4 |
| **STACK OPS** | | | | | | | | | | |
| PUSH B | Push register Pair B & C on stack | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 12 |
| PUSH D | Push register Pair D & E on stack | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 12 |
| PUSH H | Push register Pair H & L on stack | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 12 |
| PUSH PSW | Push A and Flags on stack | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 12 |
| POP B | Pop register Pair B & C off stack | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 10 |
| POP D | Pop register Pair D & E off stack | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 10 |
| POP H | Pop register Pair H & L off stack | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 10 |
| POP PSW | Pop A and Flags off stack | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 10 |
| XTHL | Exchange top of stack H & L | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 16 |
| SPHL | H & L to stack pointer | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 6 |
| **JUMP** | | | | | | | | | | |
| JMP | Jump unconditional | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 10 |
| JC | Jump on carry | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 7/10 |
| JNC | Jump on no carry | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 7/10 |
| JZ | Jump on zero | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 7/10 |
| JNZ | Jump on no zero | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 7/10 |
| JP | Jump on positive | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 7/10 |
| JM | Jump on minus | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 7/10 |
| JPE | Jump on parity even | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 7/10 |
| JPO | Jump on parity odd | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 7/10 |
| PCHL | H & L to program counter | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 6 |
| **CALL** | | | | | | | | | | |
| CALL | Call unconditional | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 18 |
| CC | Call on carry | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 9/18 |
| CNC | Call on no carry | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 9/18 |
| CZ | Call on zero | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 9/18 |
| CNZ | Call on no zero | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 9/18 |
| CP | Call on positive | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 9/18 |
| CM | Call on minus | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 9/18 |
| CPE | Call on parity even | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 9/18 |
| CPO | Call on parity odd | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 9/18 |
| **RETURN** | | | | | | | | | | |
| RET | Return | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 10 |
| RC | Return on carry | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 6/12 |
| RNC | Return on no carry | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 6/12 |
| RZ | Return on zero | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 6/12 |
| RNZ | Return on no zero | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 6/12 |
| RP | Return on positive | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 6/12 |
| RM | Return on minus | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6/12 |
| RPE | Return on parity even | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 6/12 |
| RPO | Return on parity odd | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 6/12 |
| **RESTART** | | | | | | | | | | |
| RST | Restart | 1 | 1 | A | A | A | 1 | 1 | 1 | 12 |
| **INPUT/OUTPUT** | | | | | | | | | | |
| IN | Input | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 10 |
| OUT | Output | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 10 |

## INSTRUCTION SET SUMMARY (Cont.)

| Mnemonic* | Description | Instruction Code (Note 1) D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Clock Cycles (Note 2) |
|---|---|---|---|---|---|---|---|---|---|---|
| **INCREMENT AND DECREMENT** | | | | | | | | | | |
| INR r | Increment register | 0 | 0 | D | D | D | 1 | 0 | 0 | 4 |
| DCR r | Decrement register | 0 | 0 | D | D | D | 1 | 0 | 1 | 4 |
| INR M | Increment memory | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 10 |
| DCR M | Decrement memory | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 10 |
| INX B | Increment B & C registers | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 6 |
| INX D | Increment D & E registers | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 6 |
| INX H | Increment H & L registers | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 6 |
| INX SP | Increment stack pointer | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 6 |
| DCX B | Decrement B & C | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 6 |
| DCX D | Decrement D & E | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 6 |
| DCX H | Decrement H & L | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 6 |
| DCX SP | Decrement stack pointer | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 6 |
| **ADD** | | | | | | | | | | |
| ADD r | Add register to A | 1 | 0 | 0 | 0 | 0 | S | S | S | 4 |
| ADC r | Add register to A with carry | 1 | 0 | 0 | 0 | 1 | S | S | S | 4 |
| ADD M | Add memory to A | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 7 |
| ADC M | Add memory to A with carry | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 7 |
| ADI | Add immediate to A | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 7 |
| ACI | Add immediate to A with carry | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 7 |
| DAD B | Add B & C to H & L | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 10 |
| DAD D | Add D & E to H & L | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 10 |
| DAD H | Add H & L to H & L | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 10 |
| DAD SP | Add stack pointer to H & L | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 10 |
| **SUBTRACT** | | | | | | | | | | |
| SUB r | Subtract register from A | 1 | 0 | 0 | 1 | 0 | S | S | S | 4 |
| SBB r | Subtract register from A with borrow | 1 | 0 | 0 | 1 | 1 | S | S | S | 4 |
| SUB M | Subtract memory from A | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 7 |
| SBB M | Subtract memory from A with borrow | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 7 |
| SUI | Subtract immediate from A | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 7 |
| SBI | Subtract immediate from A with borrow | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 7 |
| **LOGICAL** | | | | | | | | | | |
| ANA r | And register with A | 1 | 0 | 1 | 0 | 0 | S | S | S | 4 |
| XRA r | Exclusive Or register with A | 1 | 0 | 1 | 0 | 1 | S | S | S | 4 |
| ORA r | Or register with A | 1 | 0 | 1 | 1 | 0 | S | S | S | 4 |
| CMP r | Compare register with A | 1 | 0 | 1 | 1 | 1 | S | S | S | 4 |
| ANA M | And memory with A | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 7 |
| XRA M | Exclusive Or memory with A | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 7 |
| ORA M | Or memory with A | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 7 |
| CMP M | Compare memory with A | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 7 |
| ANI | And immediate with A | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 7 |
| XRI | Exclusive Or immediate with A | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 7 |
| ORI | Or immediate with A | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 7 |
| CPI | Compare immediate with A | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 7 |
| **ROTATE** | | | | | | | | | | |
| RLC | Rotate A left | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 4 |
| RRC | Rotate A right | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 4 |
| RAL | Rotate A left through carry | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 4 |
| RAR | Rotate A right through carry | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 4 |
| **SPECIALS** | | | | | | | | | | |
| CMA | Complement A | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 4 |
| STC | Set carry | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 4 |
| CMC | Complement carry | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 4 |
| DAA | Decimal adjust A | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 4 |
| **CONTROL** | | | | | | | | | | |
| EI | Enable Interrupts | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 4 |
| DI | Disable Interrupts | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 4 |
| NOP | No operation | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4 |
| HLT | Halt | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 5 |
| **NEW Am8085A INSTRUCTIONS** | | | | | | | | | | |
| RIM | Read Interrupt Mask | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| SIM | Set Interrupt Mask | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 4 |

Notes: 1. DOD or SSS: 8=000, C=001, D=010, E=011, H=100, L=101, Memory=110, A=111.
2. Two possible cycle times (6/12) indicate instruction cycles dependent on condition flags.

*All mnemonics copyright © Intel Corporation 1977

# Am8155/Am8156

## 2048-Bit Static MOS RAM With I/O Ports and Timer

### ADVANCE INFORMATION

#### DISTINCTIVE CHARACTERISTICS

- 256 word x 8-bits
- Single +5V power supply
- Completely static operation
- Internal address latch
- 2 programmable 8-bit I/O ports
- 1 programmable 6-bit I/O port
- Programmable 14-bit binary counter/timer
- Multiplexed address and data bus

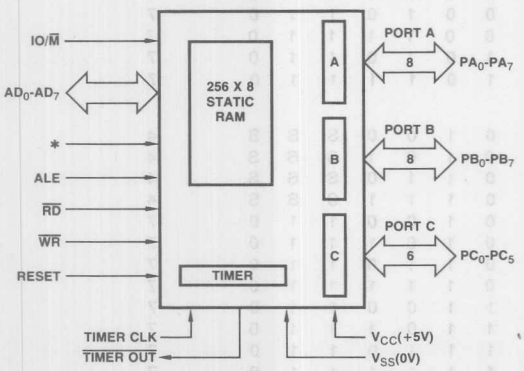
#### GENERAL DESCRIPTION

The Am8155 and Am8156 are RAM and I/O chips to be used in the Am8085A MPU system. The RAM portion is designed with 2K bit static cells organized as 256 x 8. They have a maximum access time of 400ns to permit use with no wait states in Am8085A CPU.

The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.

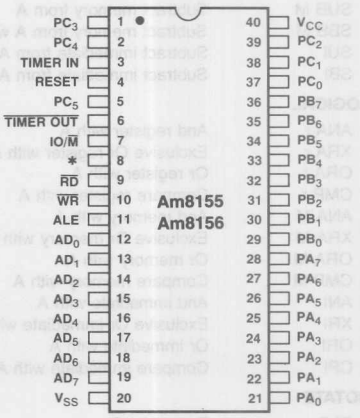
#### BLOCK DIAGRAM




*Am8155 = $\overline{CE}$, Am8156 = CE

MOS-070

#### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

MOS-071

### ORDERING INFORMATION

| Package Type | Temperature Range | Order Numbers | |
|---|---|---|---|
| Hermetic DIP* | 0°C ≤ $T_A$ ≤ +70°C | AM8155DC or AM8155CC | AM8156DC or AM8156CC |
| Molded DIP | | AM8155PC | AM8156PC |

*Hermetic = Ceramic = DC = CC = D-40-1.

## FUNCTIONAL PIN DEFINITION

The following describes the functions of all of the Am8155/Am8156 pins.

**RESET**

The Reset signal is a pulse provided by the Am8085 to initialize the system. Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be 600ns. (Two Am8085A clock cycle times).

**$AD_0$-$AD_7$**

These are 3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch on the falling edge of the ALE. The address can be either for the memory section or the I/O section depending on the polarity of the IO/M input signal. The 8-bit data is either written into the chip or read from the chip depending on the status of $\overline{WRITE}$ or $\overline{READ}$ input signal.

**CE OR $\overline{CE}$**

Chip Enable: On the Am8155, this pin is $\overline{CE}$ and is ACTIVE LOW. On the Am8156, this pin is CE and is ACTIVE HIGH.

**$\overline{RD}$**

Input low on this line with the Chip Enable active enables the $AD_{0-7}$ buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port will be read to the AD bus.

**$\overline{WR}$**

Input low on this line with the Chip Enable active causes the data on the AD lines to be written to the RAM or I/O ports depending on the polarity of IO/$\overline{M}$.

**ALE**

Address Latch Enable: This control signal latches both the address on the $AD_{0-7}$ lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.

**IO/$\overline{M}$**

IO/$\overline{Memory}$ Select: This line selects the memory if low and selects the IO if high.

**$PA_0$-$PA_7$**

These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the Command/Status Register.

**$PB_0$-$PB_7$**

These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the Command/Status Register.

**$PC_0$-$PC_5$**

These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the C/S Register. When $PC_{0-5}$ are used as control signals, they will provide the following:

- $PC_0$ – A INTR (Port A Interrupt)
- $PC_1$ – A BF (Port A Buffer full)
- $PC_2$ – $\overline{A\ STB}$ (Port A Strobe)
- $PC_3$ – B INTR (Port B Interrupt)
- $PC_4$ – B BF (Port B Buffer Full)
- $PC_5$ – $\overline{B\ STB}$ (Port B Strobe)

**TIMER IN**

This is the input to the counter timer.

**$\overline{TIMER\ OUT}$**

This pin is the timer output. This output can be either a square wave or a pulse depending on the timer mode.

**$V_{CC}$**

+5 volt supply.

**$V_{SS}$**

Ground reference.

7

## MAXIMUM RATINGS above which useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| $V_{CC}$ with Respect to $V_{SS}$ | −0.5V to +7.0V |
| All Signal Voltages with Respect to $V_{SS}$ | −0.5V to +7.0V |
| Power Dissipation | 1.5W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## DC CHARACTERISTICS ($T_A$ = 0°C to +70°C; $V_{CC}$ = 5V ± 5%)

| Parameters | Description | | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | | | −0.5 | | 0.8 | Volts |
| $V_{IH}$ | Input High Voltage | | | 2.0 | | $V_{CC}$+0.5 | Volts |
| $V_{OL}$ | Output Low Voltage | | $I_{OL}$ = 2mA | | | 0.45 | |
| $V_{OH}$ | Output High Voltage | | $I_{OH}$ = −400μA | 2.4 | | | Volts |
| $I_{IL}$ | Input Leakage | | $V_{IN}$ = $V_{CC}$ to 0V | | | ±10 | μA |
| $I_{LO}$ | Output Leakage Current | | 0.45V ≤ $V_{OUT}$ ≤ $V_{CC}$ | | | ±10 | μA |
| $I_{CC}$ | $V_{CC}$ Supply Current | | | | | 180 | mA |
| $I_{IL}$(CE) | Chip Enable Leakage | Am8155<br>Am8156 | $V_{IN}$ = $V_{CC}$ to 0V | | +100<br>−100 | | μA |

| | | | | | |
|---|---|---|---|---|---|
| $t_{LA}$ | Address Hold Time After Latch | | 80 | | ns |
| $t_{LC}$ | Latch to READ/WRITE Control | | 100 | | ns |
| $t_{RD}$ | Valid Data Out Delay from READ Control | | | 170 | ns |
| $t_{AD}$ | Address Stable to Data Out Valid | | | 400 | ns |
| $t_{LL}$ | Latch Enable Width | | 100 | | ns |
| $t_{RDF}$ | Data Bus Float After Read | | 0 | 100 | ns |
| $t_{CL}$ | READ/WRITE Control to Latch Enable | | 20 | | ns |
| $t_{CC}$ | READ/WRITE Control Width | | 250 | | ns |
| $t_{DW}$ | Data In to WRITE Set-up Time | | 150 | | ns |
| $t_{WD}$ | Data In Hold Time After WRITE | | 0 | | ns |
| $t_{RV}$ | Recovery Time Between Controls | | 300 | | ns |
| $t_{WP}$ | WRITE to Port Output | | | 400 | ns |
| $t_{PR}$ | Port Input Set-up Time | 150pF Load | 70 | | ns |
| $t_{RP}$ | Port Input Hold Time | | 50 | | ns |
| $t_{SBF}$ | Strobe to Buffer Full | | | 400 | ns |
| $t_{SS}$ | Strobe Width | | 200 | | ns |
| $t_{RBE}$ | READ to Buffer Empty | | | 400 | ns |
| $t_{SI}$ | Strobe to INTR On | | | 400 | ns |
| $t_{RDI}$ | READ to INTR Off | | | 400 | ns |
| $t_{PSS}$ | Port Set-up Time to Strobe | | 50 | | ns |
| $t_{PHS}$ | Port Hold Time After Strobe | | 120 | | ns |
| $t_{SBE}$ | Strobe to Buffer Empty | | | 400 | ns |
| $t_{WBF}$ | WRITE to Buffer Full | | | 400 | ns |
| $t_{WI}$ | WRITE to INTR Off | | | 400 | ns |
| $t_{TL}$ | TIMER-IN to $\overline{\text{TIMER-OUT}}$ Low | | | 400 | ns |
| $t_{TH}$ | TIMER-IN to $\overline{\text{TIMER-OUT}}$ High | | | 400 | ns |
| $t_{RDE}$ | Data Bus Enable from READ Control | | 10 | | ns |

Note: For Timer Input Specification, see Figure 10.

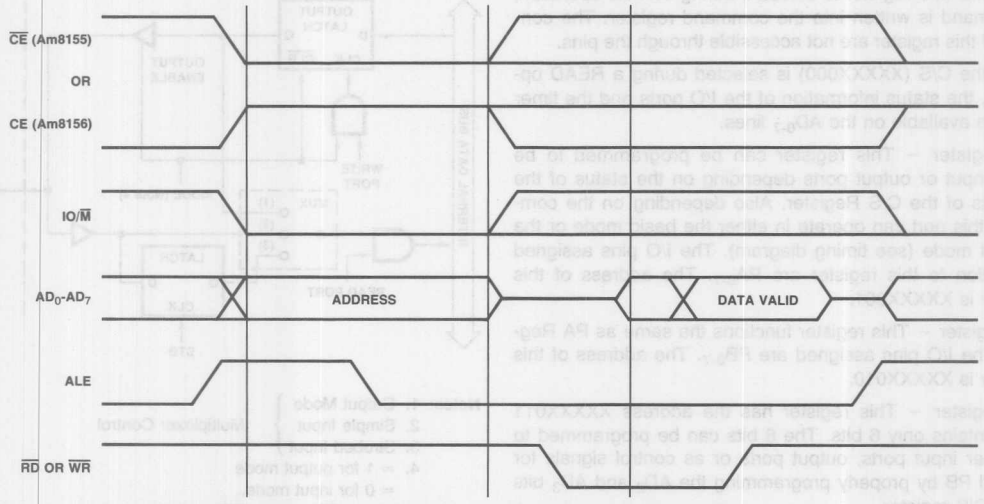
## OPERATIONAL DESCRIPTION

The Am8155/8156 includes the following operational features:

- 2K Bit Static RAM organized as 256 x 8
- Two 8-bit I/O ports (PA and PB) and one 6-bit I/O port (PC)
- 14-bit down counter

The I/O portion contains four registers (Command/Status, $PA_{0-7}$, $PB_{0-7}$, $PC_{0-5}$). The IO/$\overline{M}$ (IO/$\overline{\text{Memory}}$ Select) pin selects the I/O or the memory (RAM) portion. Detailed descriptions of memory, I/O ports and timer functions will follow.

The 8-bit address on the AD lines, the Chip Enable input, and IO/$\overline{M}$ are all latched on chip at the falling edge of ALE. A low on the IO/$\overline{M}$ must be provided to select the memory section.




Note: For detailed timing diagram information, see Figure 7 and AC Characteristics.

**Figure 1. Memory Read/Write Cycle.**

MOS-072

## PROGRAMMING OF THE COMMAND/STATUS REGISTER

The command register consists of eight latches, one for each bit. Four bits (0-3) define the mode of the ports. Two bits (4-5) enable or disable the interrupt from port C when it acts as control port, and the last two bits (6-7) are for the timer.

The C/S register contents can be altered at any time by using the I/O address XXXXX000 during a WRITE operation. The meaning of each bit of the command byte is defined as follows:

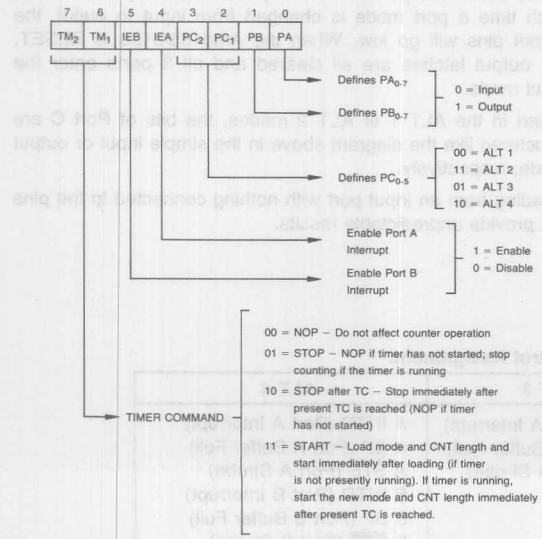



**Figure 2. Command/Status Register Bit Assignment.**

## READING THE COMMAND/STATUS REGISTER

The status register consists of seven latches, one for each bit: six (0-5) for the status of the ports and one (6) for the status of the timer.

The status of the timer and the I/O section can be polled by reading the C/S Register (Address XXXXX000). Status word format is shown below:

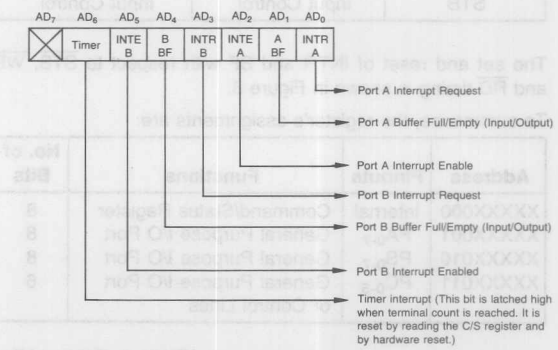



**Figure 3. Command/Status Register Status Word Format.**

## INPUT/OUTPUT SECTION

The I/O section of the Am8155/8156 consists of four registers as described below.

- Command/Status Register (C/S) – This register is assigned the address XXXXX000. The C/S address serves the dual purpose.

  When the C/S register is selected during WRITE operation, a command is written into the command register. The contents of this register are not accessible through the pins.

  When the C/S (XXXXX000) is selected during a READ operation, the status information of the I/O ports and the timer become available on the $AD_{0-7}$ lines.

- PA Register – This register can be programmed to be either input or output ports depending on the status of the contents of the C/S Register. Also depending on the command, this port can operate in either the basic mode or the strobed mode (see timing diagram). The I/O pins assigned in relation to this register are $PA_{0-7}$. The address of this register is XXXXX001.

- PB Register – This register functions the same as PA Register. The I/O pins assigned are $PB_{0-7}$. The address of this register is XXXXX010.

- PC Register – This register has the address XXXXX011 and contains only 6 bits. The 6 bits can be programmed to be either input ports, output ports or as control signals for PA and PB by properly programming the $AD_2$ and $AD_3$ bits of the C/S register.

  When $PC_{0-5}$ is used as a control port, 3 bits are assigned for Port A and 3 for Port B. The first bit is an interrupt that the Am8155 sends out. The second is an output signal indicating whether the buffer is full or empty, and the third is an input pin to accept a strobe for the strobed input mode. See Table 1.

When the 'C' port is programmed to either ALT3 or ALT4, the control signals for PA and PB are initialized as follows:

| Control | Input Mode | Output Mode |
|---|---|---|
| BF | Low | Low |
| INTR | Low | High |
| $\overline{STB}$ | Input Control | Input Control |

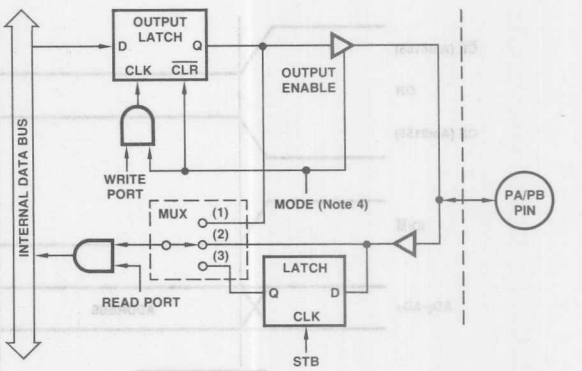
The set and reset of INTR and BF with respect to $\overline{STB}$, $\overline{WR}$ and $\overline{RD}$ timing is shown in Figure 8.

To summarize, the register's assignments are:

| Address | Pinouts | Functions | No. of Bits |
|---|---|---|---|
| XXXXX000 | Internal | Command/Status Register | 8 |
| XXXXX001 | $PA_{0-7}$ | General Purpose I/O Port | 8 |
| XXXXX010 | $PB_{0-7}$ | General Purpose I/O Port | 8 |
| XXXXX011 | $PC_{0-5}$ | General Purpose I/O Port or Control Lines | 6 |

The following diagram shows how I/O Ports A and B are structured within the Am8155 and Am8156:

**Am8155/Am8156**
**One Bit of Port A or Port B**




MOS-073

Notes: 1. Output Mode
2. Simple Input
3. Strobed Input
} Multiplexer Control
4. = 1 for output mode
= 0 for input mode.

Read Port = (IO/$\overline{M}$ = 1) • ($\overline{RD}$ = 0) • (CE active) • (Port address selected)

Write Port = (IO/$\overline{M}$ = 1) • ($\overline{WR}$ = 0) • (CE active) • (Port address selected)

Note in the diagram that when the I/O ports are programmed to be output ports, the contents of the output ports can still be read by a READ operation when appropriately addressed.

Note also that the output latch is cleared when the port enters the input mode. The output latch cannot be loaded by writing to the port if the port is in the input mode. The result is that each time a port mode is changed from input to ouput, the output pins will go low. When the Am8155/8156 is RESET, the output latches are all cleared and all 3 ports enter the input mode.

When in the ALT 1 or ALT 2 modes, the bits of Port C are structured like the diagram above in the simple input or output mode, respectively.

Reading from an input port with nothing connected to the pins will provide unpredictable results.

**Table 1. Table of Port Control Assignment.**

| Pin | ALT 1 | ALT 2 | ALT 3 | ALT 4 |
|---|---|---|---|---|
| PC0 | Input Port | Output Port | A INTR (Port A Interrupt) | A INTR (Port A Interrupt) |
| PC1 | Input Port | Output Port | A BF (Port A Buffer Full) | A BF (Port A Buffer Full) |
| PC2 | Input Port | Output Port | A $\overline{STB}$ (Port A Strobe) | A $\overline{STB}$ (Port A Strobe) |
| PC3 | Input Port | Output Port | Output Port | B INTR (Port B Interrupt) |
| PC4 | Input Port | Output Port | Output Port | B BF (Port B Buffer Full) |
| PC5 | Input Port | Output Port | Output Port | B $\overline{STB}$ (Port B Strobe) |

## TIMER SECTION

The timer is a 14-bit down counter that counts the 'timer input' pulses and provides either a square wave or pulse when terminal count (TC) is reached.

The timer has the I/O address XXXXX100 for the low order byte of the register and the I/O address XXXXX101 for the high order byte of the register.

To program the timer, the COUNT LENGTH REG is loaded first, one byte at a time, by selecting the timer addresses. Bits 0-13 will specify the length of the next count and bits 14-15 will specify the timer output mode. The value loaded into the count length register can have any value from $2_H$ through $3FFF_H$ in bits 0-13.

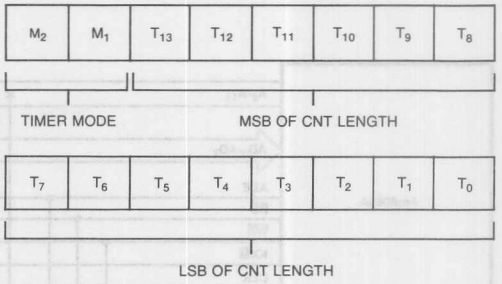



**Figure 4. Timer Format.**

There are four modes to choose from:

0 – Puts out low during second half of count
1 – Square wave
2 – Single pulse upon TC being reached
3 – Repetitive single pulse everytime TC is readied and automatic reload of counter upon TC being reached, until instructed to stop by a new command loaded into C/S.

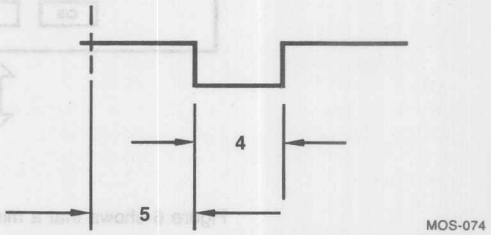
Bits 6-7 of Command/Status Register Contents are used to start and stop the counter. There are four commands to choose from (See the further description on Command/Status Register.).

| C/S7 | C/S6 | |
|---|---|---|
| 0 | 0 | NOP – Do not affect counter operation. |
| 0 | 1 | STOP – NOP if timer has not started; stop counting if the timer is running. |
| 1 | 0 | STOP AFTER TC – Stop immediately after present TC is reached (NOP if timer has not started). |
| 1 | 1 | START – Load mode and CNT length and start immediately after loading (if timer is not presently running). If timer is running, start the new mode and CNT length immediately after present TC is reached. |

M2 and M1 define the timer mode as follows:

| M2 | M1 | |
|---|---|---|
| 0 | 0 | Puts out low during second half of count. |
| 0 | 1 | Square wave, i.e., the period of the square wave equals the count length programmed with automatic reload at terminal count. |
| 1 | 0 | Single pulse upon TC being reached. |
| 1 | 1 | Automatic reload, i.e., single pulse everytime TC is reached. |

Note: In case of an asymmetric count, i.e., 9, larger half of the count will be high, the larger count will stay active as shown in Figure 5.




Note: 5 and 4 refer to the number of clock cycles in that time period.

**Figure 5. Asymmetric Count.**

The counter in the Am8155 is not initialized to any particular mode or count when hardware RESET occurs, but RESET does stop the counting. Therefore, counting cannot begin following RESET until a START command is issued via the C/S register.

7

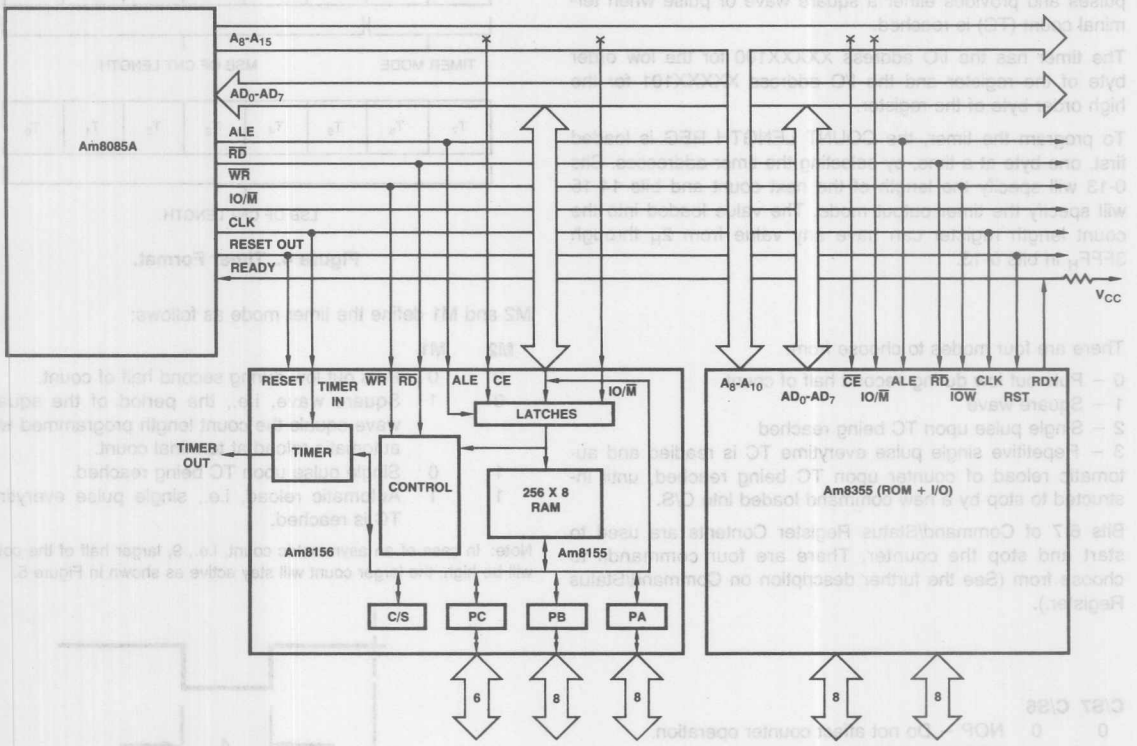


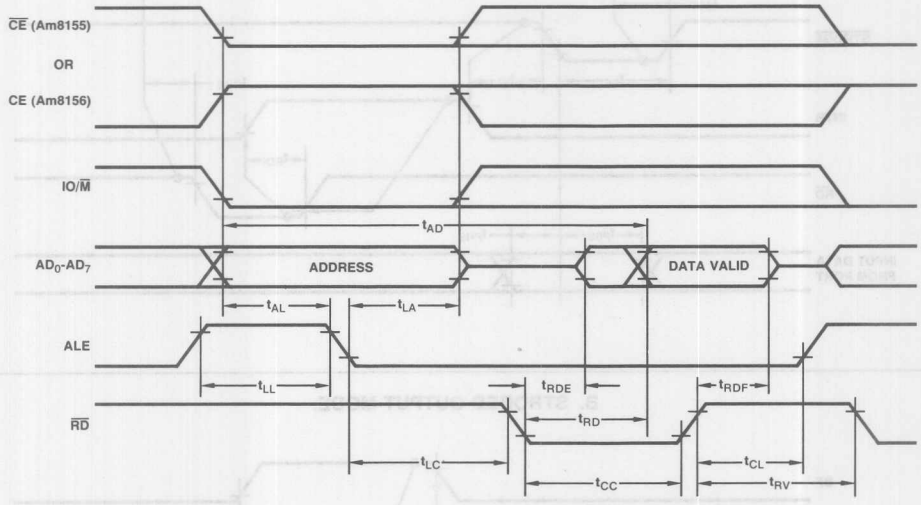

Figure 6 shows that a minimum system is possible using only three chips:

- 256 Bytes RAM
- 2K Bytes ROM
- 38 I/O Pins
- 1 Interval Timer
- 4 Interrupt Levels

**Figure 6. Am8085A Minimum System Configuration.**

## WAVEFORMS

### A. READ CYCLE.




MOS-076

### B. WRITE CYCLE.

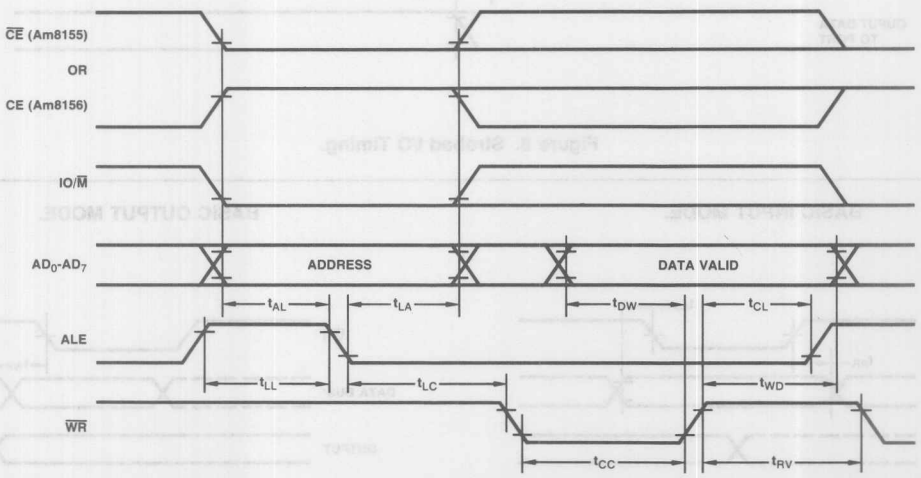


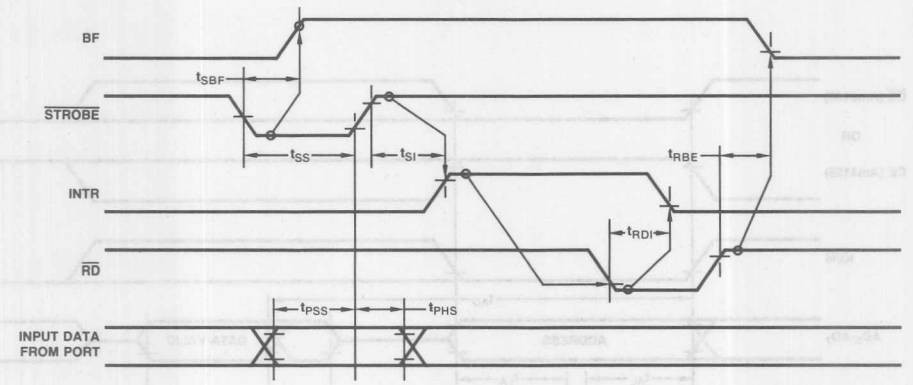

**Figure 7. Am8155/8156 Read/Write Timing Diagrams.**

MOS-077

7

## WAVEFORMS (Cont.)

### A. STROBED INPUT MODE.




MOS-078

### B. STROBED OUTPUT MODE.

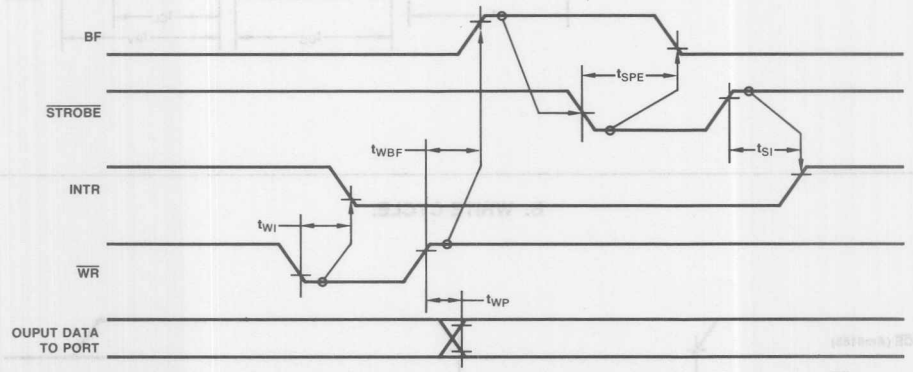
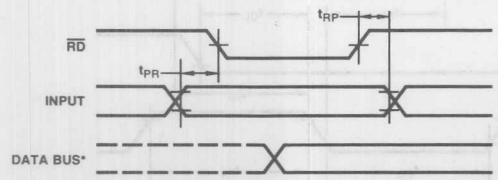



**Figure 8. Strobed I/O Timing.**

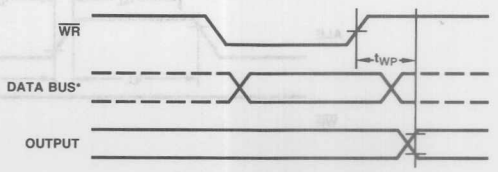
MOS-079

### BASIC INPUT MODE.




MOS-080

### BASIC OUTPUT MODE.

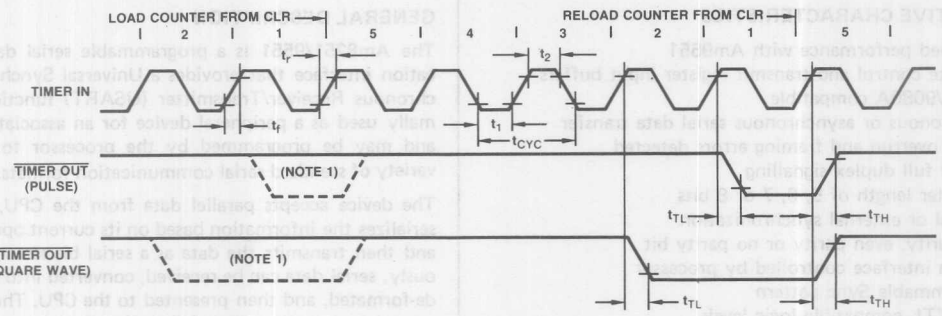



MOS-081

*Data bus timing is shown in Figure 7.

**Figure 9. Basic I/O Timing Waveform.**

## WAVEFORMS (Cont.)




Note 1: The timer output is periodic if in an automatic reload mode ($M_1$ mode bit = 1).

**Countdown from 5 to 1**

| | | |
|---|---|---|
| $t_{CYC}$ | 320ns | MIN. |
| $t_r$ and $t_f$ | 30ns | MAX. |
| $t_1$ | 80ns | MIN. |
| $t_2$ | 120ns | MIN. |
| $t_{TL}$ and $t_{TH}$ | 400ns | MAX. |

**Figure 10. Timer Output Waveform.**

MOS-082

7

## DISTINCTIVE CHARACTERISTICS

- Improved performance with Am9551
- Separate control and transmit register input buffers
- 8080A/9080A compatible
- Synchronous or asynchronous serial data transfer
- Parity, overrun and framing errors detected
- Half or full duplex signalling
- Character length of 5, 6, 7 or 8 bits
- Internal or external synchronization
- Odd parity, even parity or no parity bit
- Modem interface controlled by processor
- Programmable Sync pattern
- Fully TTL compatible logic levels
- +5 only power supply
- Commercial and military temperature range operation
- Ion-implanted N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

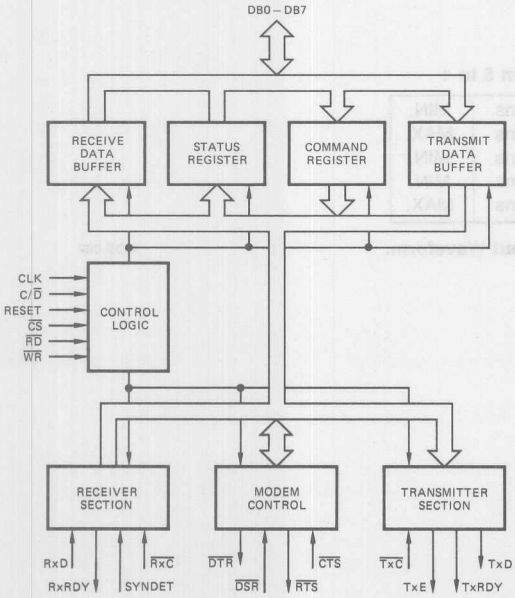
## GENERAL DESCRIPTION

The Am8251/9551 is a programmable serial data communication interface that provides a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) function. It is normally used as a peripheral device for an associated processor, and may be programmed by the processor to operate in a variety of standard serial communication formats.

The device accepts parallel data from the CPU, formats and serializes the information based on its current operating mode, and then transmits the data as a serial bit stream. Simultaneously, serial data can be received, converted into parallel form, de-formated, and then presented to the CPU. The USART can operate in an independent full duplex mode.

Data, Control, operation and format options are all selected by commands from an associated processor. This provides an unusual degree of flexibility and allows the Am8251/9551 to service a wide range of communication disciplines and applications.

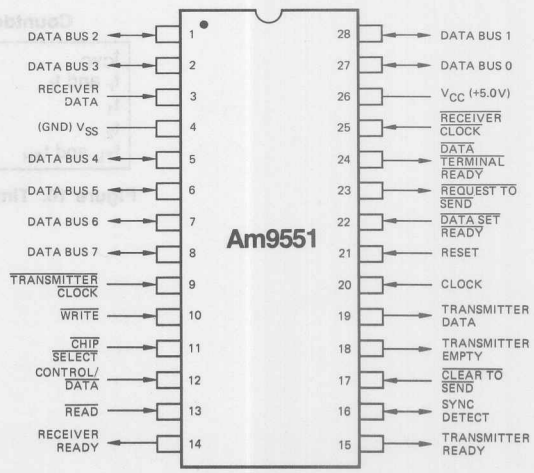
## BLOCK DIAGRAM




MOS-214

## CONNECTION DIAGRAM

Top View




Pin 1 is marked for orientation.

MOS-215

## ORDERING INFORMATION

| Package Type | Ambient Temperature Specification | 8251 Specifications | 9551 Specifications | |
|---|---|---|---|---|
| | | | Standard | Upgraded |
| Hermetic DIP* | $0°C \leq T_A \leq +70°C$ | AM8251DC/D8251<br>AM8251CC/C8251 | AM9551DC<br>AM9551CC | AM9551-4DC<br>AM9551-4CC |
| Molded DIP | | AM8251PC/P8251 | AM9551PC | AM9551-4PC |
| Hermetic DIP | $-55°C \leq T_A \leq +125°C$ | AM8251DM/M8251 | AM9551DM | |

*Hermetic = Ceramic = DC = CC = D-28-1.

## INTERFACE SIGNAL DESCRIPTION

**Data Bus**

The Am9551 uses an 8 bit bi-directional data bus to exchange information with an associated processor. Internally, data is routed between the data bus buffers and the transmitter section or receiver section as selected by the Read ($\overline{RD}$) or Write ($\overline{WR}$) control inputs.

**Chip Select ($\overline{CS}$)**

The active low Chip Select input allows the Am9551 to be individually selected from other devices within its address range. When Chip Select is high, reading or writing is inhibited, and the data bus output is in it's high impedance state.

**Reset**

The Am9551 will assume an idle state when a high level is applied to the Reset input. When the Reset is returned Low, the Am9551 will remain in the idle state until it receives a new mode control instruction.

**Read ($\overline{RD}$)**

The active low Read input enables data to be transferred from the Am9551 to the processor.

**Write ($\overline{WR}$)**

The active low Write input enables data to be transferred from the processor to the Am9551.

**Control/Data (C/$\overline{D}$)**

During a Read operation, if this input is at a high level the status byte will be read, and if it is at a low level the receive data will be read by the processor. When a Write operation is being performed, this input will indicate to the Am9551 that the bus information being written is a command if C/$\overline{D}$ is high and data if C/$\overline{D}$ is low.

| C/$\overline{D}$ | $\overline{RD}$ | $\overline{WR}$ | $\overline{CS}$ | |
|---|---|---|---|---|
| 0 | 0 | 1 | 0 | Am9551 DATA → DATA BUS |
| 0 | 1 | 0 | 0 | DATA BUS → Am9551 DATA |
| 1 | 0 | 1 | 0 | Am9551 STATUS → DATA BUS |
| 1 | 1 | 0 | 0 | DATA BUS → Am9551 COMMAND |
| X | X | X | 1 | DATA BUS → 3-STATE |

**Clock (CLK)**

This input is used for internal timing within the Am9551. It does not control the transmit or receive rate. However, it should be at least 30 times the receive or transmit rate in the synchronous mode and 4.5 times the receive or transmit rate in the asynchronous mode. The CLK frequency is also restricted by both an upper and a lower bound. This input is often connected to a clock from the associated processor.

**Receiver Data (RxD)**

Serial data is received from the communication line on this input.

**Receiver Clock ($\overline{RxC}$)**

The serial data on input RxD is clocked into the Am9551 by the $\overline{RxC}$ clock signal. In the synchronous mode, $\overline{RxC}$ is determined by the baud rate and supplied by the modem. In the asynchronous mode, $\overline{RxC}$ is 1, 16, or 64 times the baud rate as selected in the mode control instruction. Data is sampled by the Am9551 on the rising edge of $\overline{RxC}$.

**Receiver Ready (RxRDY)**

The RxRDY output signal indicates to the processor that data has been shifted into the receiver buffer from the receiver section and may be read. The signal is active high and will be reset when the buffer is read by the processor. RxRDY can be activated only if the receiver enable (RxE) has been set in the command register, even though the receiver may be running. If the processor does not read the receiver buffer before the next character is shifted from the receiver section then an overrun error will be indicated in the status buffer.

**Sync Detect (SYNDET)**

This signal is used only in the synchronous mode. It can be either an output or input depending on whether the program is set for internal or external synchronization. As an output, a high level indicates when the sync character has been detected in the received data stream after the Internal Synchronization mode has been programmed. If the Am9551 is programmed to utilize two sync characters, then SYNDET will go to a high level when the last bit of the second sync character is received. SYNDET is reset when the status buffer is read or when a Reset signal is activated. SYNDET will perform as an input when the External Synchronization mode is programmed. External logic can supply a positive-going signal to indicate to the Am9551 that synchronization has been attained. This will cause it to initialize the assembly of characters on the next falling edge of $\overline{RxC}$. To successfully achieve synchronization the SYNDET signal should be maintained in a high condition for at least one full period of $\overline{RxC}$.

**Transmit Data (TxD)**

Serial data is transmitted to the communication line on this output.

**Transmitter Clock ($\overline{TxC}$)**

The serial data on TxD is clocked out with the $\overline{TxC}$ signal. The relationship between clock rate and baud rate is similar to that for $\overline{RxC}$. Data is shifted out of the Am9551 on the falling edge of $\overline{TxC}$.

**Transmitter Ready (TxRDY)**

The TxRDY output signal goes high when data in the Transmit Data Buffer has been shifted into the transmitter section allowing the Transmit Data Buffer to accept the next byte from the processor. TxRDY will be reset when information is written into the Transmit Data Buffer. Loading command register also resets TxRDY. TxRDY will be available on this output pin only when the Am9551 is enable to transmit (CTS = 0, TxEN = 1). However, the TxRDY bit in the status Buffer will always be set when the Transmit Data Buffer is empty regardless of the state of TxEN and $\overline{CTS}$.

**Transmitter Empty (TxE)**

The TxE output signal goes high when the Transmitter section has transmitted its data and is empty. The signal will remain high until a new data byte is shifted from the Transmit Data Buffer to the Transmitter section. In the synchronous mode if the processor does not load a new byte into the buffer in time, TxE will, independent of the status of the TxEN bit in the command register, momentarily go to a high level as SYNC characters are loaded into the Transmitter Section.

**Data Terminal Ready ($\overline{DTR}$)**

This signal is a general purpose output which reflects the state of bit 1 in the Command instruction. It is commonly connected to an associated modem to indicate that the Am9551 is ready.

**Data Set Ready ($\overline{DSR}$)**

This is a general purpose input signal and forms part of the status byte that may be read by the processor. $\overline{DSR}$ is generally used as a response to $\overline{DTR}$, by the Modem, to indicate that it is ready. The signal acts only as a flag and does not control any internal logic.

7

## INTERFACE SIGNAL DESCRIPTION (Cont.)

**Request to Send ($\overline{RTS}$)**

This is a general purpose output, similar to $\overline{DTR}$, and reflects the state of bit 5 in Command Instruction. It is normally used to initiate a data transmission by requesting the modem to prepare to send.

**Clear to Send ($\overline{CTS}$)**

This is a general purpose input signal used to enable the 8251/9551 to transmit data if the TxEN bit in the Command byte is a one. $\overline{CTS}$ is generally used as a response to $\overline{RTS}$ by a modem to indicate that transmission may begin. Designers not using $\overline{CTS}$ in their systems should remember to tie it low so that 8251/9551 data transmission will not be disabled.

## OPERATION AND PROGRAMMING

The microcomputer program controlling the Am9551 performs these tasks:

- Outputs control codes
- Inputs status
- Outputs data to be transmitted
- Inputs data which have been received

Control codes determine the mode in which the Am9551 will operate and are used to set or reset control signals output by the Am9551.

The Status register contents will be read by the program monitoring this device's operation in order to determine error conditions, when and how to read data, write data or output control codes. Program logic may be based on reading status bit levels, or control signals may be used to request interrupts.

### INITIALIZING THE Am9551

The Am9551 may be initialized following a system reset or prior to starting a new serial I/O sequence. The USART must be reset following power up and subsequently may be reset at any time following completion of one activity and preceeding a new set of operations. Following a reset, the Am9551 enters an idle state in which it can neither transmit nor receive data.

The Am9551 is initialized with two, three or four control words from the processor. Figure 1 shows the sequence of control words needed to initialize the Am9551, for synchronous or for asynchronous operation. Note that in asynchronous operation a mode control is output to the device followed by a command. For synchronous operation, the mode control is followed by one or two SYNC characters, and then a command.

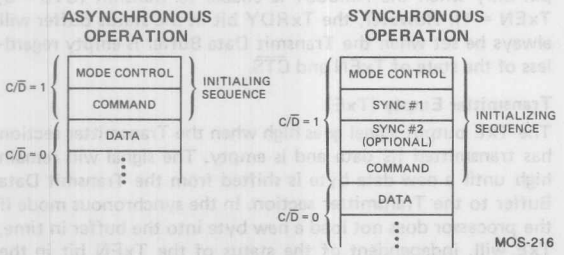



**Figure 1. Control Word Sequence for Initialization.**

Only a single address is set aside for mode control bytes, command bytes and SYNC character bytes. For this to be possible, logic internal to the chip directs control information to its proper destination based on the sequence in which it is received. Following a reset, the first control code output is interpreted as a mode control. If the mode control specifies synchronous operation, then the next one or two bytes (as determined by the mode byte) output as control codes will be interpreted as SYNC characters. For either asynchronous or synchronous operation, the next byte output as a control code is interpreted as a command. All subsequent bytes output as control codes are interpreted as commands. There are two ways in which control logic may return to anticipating a mode control input; following an external Reset signal or following an internal Reset command.

### MODE CONTROL CODES

The Am9551 interprets mode control codes as illustrated in Figures 2 and 3.

Control code bits 0 and 1 determine whether synchronous or asynchronous operation is specified. A non-zero value in bits 0 and 1 specifies asynchronous operation and defines the relationship between data transfer baud rate and receiver or transmitter clock rate. Asynchronous serial data may be received or transmitted on every clock pulse, on every 16th clock pulse, or on every 64th clock pulse. A zero in both bits 0 and 1 defines the mode of operation as synchronous.

For synchronous and asynchronous modes, control bits 2 and 3 determine the number of data bits which will be present in each data character.

For synchronous and asynchronous modes, bits 4 and 5 determine whether there will be a parity bit in each character, and if so, whether odd or even parity will be adopted. Thus in synchronous mode a character will consist of five, six, seven or

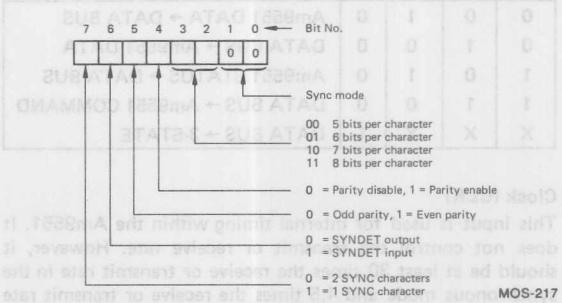



**Figure 2. Synchronous Mode Control Code.**

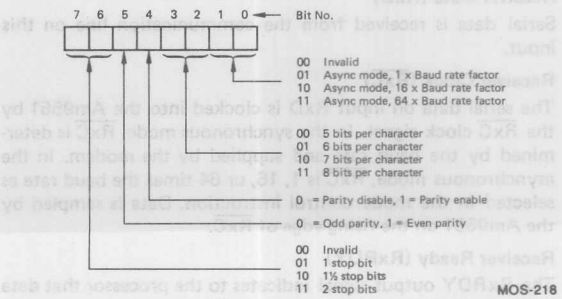



**Figure 3. Asynchronous Mode Control Code.**

## OPERATION AND PROGRAMMING (Cont.)

eight data bits, plus an optional parity bit. In asynchronous mode, the data unit will consist of five, six, seven or eight data bits, an optional parity bit, a preceeding start bit, plus 1, 1½, or 2 trailing stop bits. Interpretation of subsequent bits differs for synchronous or asynchronous modes.

Control code bits 6 and 7 in asynchronous mode determine how many stop bits will trail each data unit. 1½ stop bits can only be specified with a 16x or 64x baud rate factor. In these two cases, the half stop bit will be equivalent to 8 or 32 clock pulses, respectively.

In synchronous mode, control bits 6 and 7 determine how character synchronization will be achieved. When SYNDET is an output, internal synchronization is specified; one or two SYNC characters, as specified by control bit 7, must be detected at the head of a data stream in order to establish synchronization.

### COMMAND WORDS

Command words are used to initiate specific functions within the Am9551 such as, "reset all error flags" or "start searching for sync". Consequently, Command Words may be issued by the microprocessor to the Am9551 at any time during the execution of a program in which specific functions are to be initiated within the communication circuit.

Figure 4 shows the format for the Command Word.

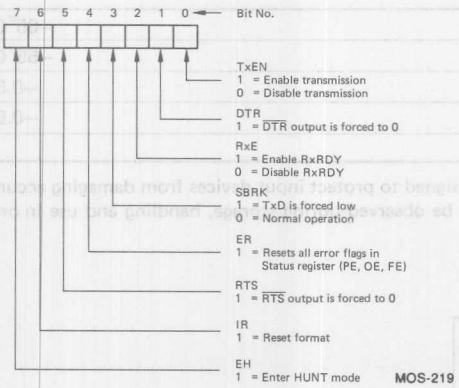



**Figure 4. Am9551 Control Command.**

Bit 0 of the Command Word is the Transmit Enable bit (TxEN). Data transmission from the Am9551 cannot take place unless TxEN is set in the command register. Figure 5 defines the way in which TxEN, TxE and TxRDY combine to control transmitter operations.

Bit 1 is the Data Terminal Ready (DTR) bit. When the DTR command bit is set, the DTR output connection is active (low). DTR is used to advise a modem that the data terminal is prepared to accept or transmit data.

Bit 2 is the Receiver Enable Command bit (RxE). RxE is used to enable the RxRDY output signal. RxE prevents the RxRDY signal from being generated to notify the processor that a complete character is framed in the Receive Character Buffer. It does not inhibit the assembly of data characters at the input, however. Consequently, if communication circuits are active, characters will be assembled by the receiver and transferred to the Receiver Character Buffer. If RxE is disabled, the overrun error (OE) will probably be set; to insure proper operation, the overrun error is usually reset with the same command that enables RxE.

| TxEN | TxE | TxRDY | |
|---|---|---|---|
| 1 | 1 | 1 | Transmit Output Regsiter and Transmit Character Buffer empty. TxD continues to mark if Am9551 is in the asynchronous mode. TxD will send Sync pattern if Am9551 is in the Synchronous Mode. Data can be entered into Buffer. |
| 1 | 0 | 1 | Transmit Output Register is shifting a character. Transmit Character Buffer is available to receive a new byte from the processor. |
| 1 | 1 | 0 | Transmit Register has finished sending. A new character is waiting for transmission. This is a transient condition. |
| 1 | 0 | 0 | Transmit Register is currently sending and an additional character is stored in the Transmit Character Buffer for transmission. |
| 0 | 0/1 | 0/1 | Transmitter is disabled. |

**Figure 5. Operation of the Transmitter Section as a Function of TxE, TxRDY and TxEN.**

Bit 3 is the Send Break Command bit (SBRK). When SBRK is set, the transmitter output (TxD) is interrupted and a continuous binary "0" level, (spacing) is applied to the TxD output signal. The break will continue until a subsequent Command Word is sent to the Am9551 to remove SBRK.

Bit 4 is the Error Reset bit (ER). When a Command Word is transmitted with the ER bit set, all three error flags in the Status Register are reset. Error Reset occurs when the Command Word is loaded into the Am9551. No latch is provided in the Command Register to save the ER command bit.

Bit 5, the Request To Send Command bit (RTS), sets a latch to reflect the RTS signal level. The output of this latch is created independently of other signals in the Am9551. As a result, data transfers may be made by the microprocessor to the Transmit Register, and data may be actively transmitted to the communication line through TxD regardless of the status of RTS.

Bit 6, the Internal Reset (IR), causes the Am9551 to return to the Idle mode. All functions within the Am9551 cease and no new operation can be resumed until the circuit is reinitialized. If the operating mode is to be altered during the execution of a microprocessor program, the Am9551 must first be reset. Either the external reset connection can be activated, or the Internal Reset Command can be sent to the Am9551. Internal Reset is a momentary function performed only when the command is issued.

Bit 7 is the Enter Hunt command bit (EH). The Enter Hunt mode command is only effective for the Am9551 when it is operating in the Synchronous mode. EH causes the receiver to stop assembling characters at the RxD input and start searching for the prescribed sync pattern. Once the "Enter Hunt" mode has been initiated, the search for the sync pattern will

7

Am9551, or when SYNC characters are recognized.

### STATUS REGISTER

The Status Register maintains information about the current operational status of the Am9551. Figure 6 shows the format of the Status Register.

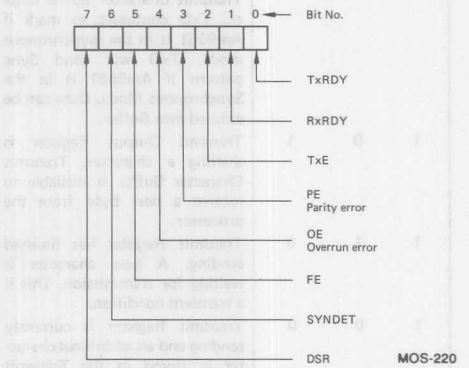



**Figure 6. The Am9551 Status Register.**

for transmission.

RxRDY signals the processor that a completed character is holding in the Receive Character Buffer Register for transfer to the processor.

TxE signals the processor that the Transmit Register is empty.

PE is the Parity Error signal indicating to the CPU that the character stored in the Receive Character Buffer was received with an incorrect number of binary "1" bits.

OE is the receiver Overrun Error. OE is set whenever a byte stored in the Receiver Character Register is overwritten with a new byte before being transferred to the processor.

FE is the character framing error which indicates that the asynchronous mode byte stored in the Receiver Character Buffer was received with incorrect character bit format, as specified by the current mode.

SYNDET is the synchronous mode status bit associated with internal sync detection.

DSR is the status bit set by the external Data Set Ready signal to indicate that the communication Data Set is operational. All status bits are set by the functions described for them. SYNDET is reset whenever the processor reads the Status Register. OE, FE, PE are reset only by command.

## MAXIMUM RATINGS Above which the useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| $V_{CC}$ with Respect to $V_{SS}$ | −0.5V to +7.0V |
| All Signal Voltages with Respect to $V_{SS}$ | −0.5V to +7.0V |
| Power Dissipation | 1.0W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGE

| Part Number | Ambient Temperature | $V_{CC}$ | $V_{SS}$ |
|---|---|---|---|
| Am9551CC<br>D8251<br>Am9551-4CC | $0°C \leq T_A \leq +70°C$ | +5.0V ± 5% | 0V |
| Am9551DM | $-55°C \leq T_A \leq +125°C$ | +5.0V ± 10% | 0V |

## ELECTRICAL CHARACTERISTICS Over Operating Range (Note 1)

| Parameters | Description | Test Conditions | C8251 Min. | C8251 Typ. | C8251 Max. | Am9551 Min. | Am9551 Typ. | Am9551 Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -200\mu A$ | | | | 2.4 | | | Volts |
| | | $I_{OH} = -100\mu A$ | 2.4 | | | | | | |
| $V_{OL}$ | Output LOW Voltage | $I_{OL} = 3.2mA$ (Note 6) | | | | | | 0.4 | Volts |
| | | $I_{OL} = 1.6mA$ | | | 0.40 | | | | |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | $V_{CC}$ | 2.0 | | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Voltage | | −0.5 | | 0.8 | −0.5 | | 0.8 | Volts |
| $I_{LI}$ | Input Load Current | $V_{SS} \leq V_{IN} \leq V_{CC}$ | | | 10 | | | 10 | µA |
| $I_{DL}$ | Data Bus Leakage | $V_{OUT} = 0.45V$ | | | −50 | | | −50 | µA |
| | | $V_{OUT} = V_{CC}$ | | | 10 | | | 10 | |
| $I_{CC}$ | $V_{CC}$ Supply Current | $T_A = +25°C$ | | 45 | | | 45 | | mA |
| | | $T_A = 0°C$ | | | 80 | | | 80 | |
| | | $T_A = -55°C$ | | | | | | 120 | |
| $C_O$ | Output Capacitance | fc = 1.0MHz, Inputs = 0V | | | | | | 15 | pF |
| $C_I$ | Input Capacitance | | | | 10 | | | 10 | pF |
| $C_{I/O}$ | I/O Capacitance | | | | 20 | | | 20 | pF |

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Note 2)

| Parameters | Description | | Am8251 Min. | Am8251 Max. | Am9551DM Am9551DC Min. | Am9551DM Am9551DC Max. | Am9551-4DC Min. | Am9551-4DC Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $t_{AR}$ | $\overline{CS}$, C/$\overline{D}$ Stable to $\overline{READ}$ Low Set-up Time | | 50 | | 50 | | 50 | | ns |
| $t_{AW}$ | $\overline{CS}$, C/$\overline{D}$ Stable to $\overline{WRITE}$ Low Set-up Time | | 20 | | 20 | | 20 | | ns |
| $t_{CR}$ | $\overline{DSR}$, $\overline{CTS}$ to $\overline{READ}$ Low Set-up Time | | | 16 | | 16 | | 16 | tCY |
| $t_{CY}$ | Clock Period | | .420 | 1.35 | .380 | 1.35 | .380 | 1.35 | μs |
| $t_{DF}$ | $\overline{READ}$ High to Data Bus Off Delay | | 25 | 200 | 25 | 200 | 25 | 200 | ns |
| $t_{DTx}$ | TxC Low to TxD Delay | | | 1.0 | | 1.0 | | 1.0 | μs |
| $t_{DW}$ | Data to $\overline{WRITE}$ High Set-up Time | | 200 | | 150 | | 100 | | ns |
| $t_{ES}$ | External SYNDET to RxC Low Set-up Time | | | 16 | | 16 | | 16 | tCY |
| $t_{HRx}$ | Sampling Pulse to Rx Data Hold Time | | 2.0 | | 2.0 | | 2.0 | | μs |
| $t_{IS}$ | Data Bit (Center) to Internal SYNDET Delay | | | 25 | | 25 | | 25 | tCY |
| $t_{\phi W}$ | Clock Pulse Width | | 220 | 0.7tCY | 175 | 0.7tCY | 175 | 0.7tCY | ns |
| $t_R$, $t_F$ | Clock Rise & Fall Time | | 0 | 50 | 0 | 50 | 0 | 50 | ns |
| $t_{RA}$ | $\overline{READ}$ High to $\overline{CS}$, C/D Hold Time | | 5.0 | | 5.0 | | 5.0 | | ns |
| $t_{RD}$ | $\overline{READ}$ Low to Data Bus On Delay | | | 350 | | 250 | | 180 | ns |
| $t_{RPD}$ | Receiver Clock High Time | 1x Baud Rate | 15 | | 15 | | 15 | | tCY |
| | | 16x & 64x Baud Rate | 3.0 | | 3.0 | | 3.0 | | |
| $t_{RPW}$ | Receiver Clock Low Time | 1x Baud Rate | 12 | | 12 | | 12 | | tCY |
| | | 16x & 64x Baud Rate | 1.0 | | 1.0 | | 1.0 | | |
| $t_{RR}$ | $\overline{READ}$ Pulse Width | | 430 | | 380 | | 250 | | ns |
| $t_{RV}$ | Time Between $\overline{WRITE}$ Pulses During Initialization (Note 3) | | 6.0 | | 6.0 | | 6.0 | | tCY |
| $t_{Rx}$ | Data Bit (Center) to RxRDY Delay | | | 20 | | 20 | | 20 | tCY |
| $t_{SRx}$ | Rx Data to Sampling Pulse Set-up Time | | 2.0 | | 2.0 | | 2.0 | | μs |
| $t_{TPD}$ | Transmitter Clock High Time | 1x Baud Rate | 15 | | 15 | | 15 | | tCY |
| | | 16x & 64x Baud Rate | 3.0 | | 3.0 | | 3.0 | | |
| $t_{TPW}$ | Transmitter Clock Low Time | 1x Baud Rate | 12 | | 12 | | 12 | | tCY |
| | | 16x & 64x Baud Rate | 1.0 | | 1.0 | | 1.0 | | |
| $t_{Tx}$ | Data Bit (Center) to TxRDY Delay | | | 16 | | 16 | | 16 | tCY |
| $t_{TxE}$ | Data Bit (Center) to Tx EMPTY Delay | | | 16 | | 16 | | 16 | tCY |
| $t_{WA}$ | $\overline{WRITE}$ High to $\overline{CS}$, C/D Hold Time | | 20 | | 20 | | 20 | | ns |
| $t_{WC}$ | $\overline{WRITE}$ High to TxE, $\overline{DTR}$, $\overline{RTS}$ Delay | | | 16 | | 16 | | 16 | tCY |
| $t_{WD}$ | $\overline{WRITE}$ High to Data Hold Time | | 40 | | 40 | | 40 | | ns |
| $t_{WW}$ | $\overline{WRITE}$ Pulse Width | | 400 | | 380 | | 250 | | ns |
| $f_{Rx}$ | Receiver Clock Frequency | 1x Baud Rate | DC | 56 | DC | 56 | DC | 56 | kHz |
| | | 16x & 64x Baud Rate | DC | 520 | DC | 520 | DC | 520 | |
| $f_{Tx}$ | Transmitter Clock Frequency | 1x Baud Rate | DC | 56 | DC | 56 | DC | 56 | kHz |
| | | 16x & 64x Baud Rate | DC | 520 | DC | 520 | DC | 520 | |

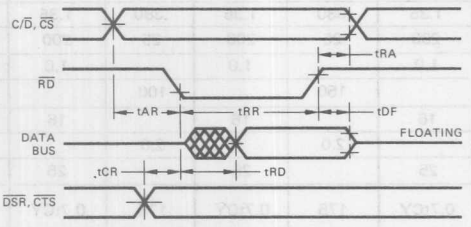
**NOTES:**

1. Typical values are for $T_A = 25°C$, nominal supply voltage and nominal processing parameters.
2. Test conditions include: transition times ≤ 20nS, output loading of 1TTL gate plus 100pF, input and output timing reference levels of 0.8V and 2.0V.
3. This time period between write pulses is specified for initialization purposes only; when MODE, SYNC 1, SYNC 2, COMMAND and first DATA BYTE are written into the Am9551. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1.
4. Reset Pulse Width = 6tCY min.
5. Switching Characteristic parameters are listed in alphabetical order.
6. The maximum Input Low Current ($I_{OL}$) is 1.6mA at $V_{OL}$ = .4V max over the military temperature range (−55 to +125°C) and $V_{CC}$ = 5V ±10%.

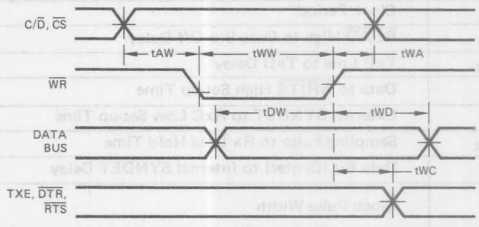
7

## SWITCHING WAVEFORMS

### READ OPERATION

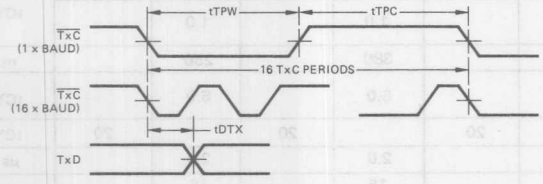



### WRITE OPERATION

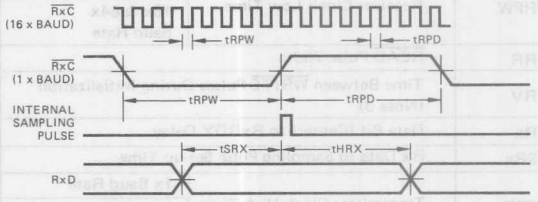



MOS-221

### TRANSMITTER CLOCK AND DATA

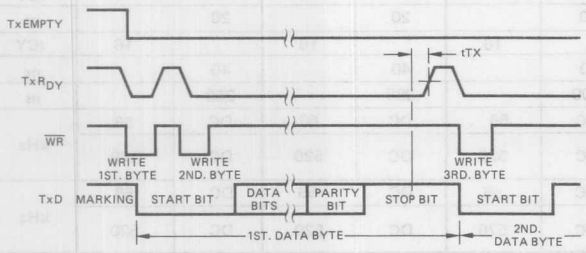



### RECEIVER CLOCK AND DATA

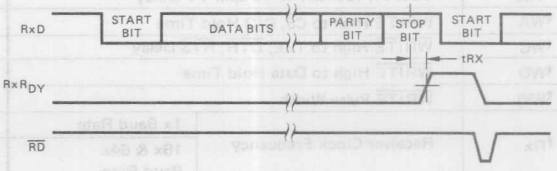



MOS-222

### TxRDY TIMING (ASYNC MODE)

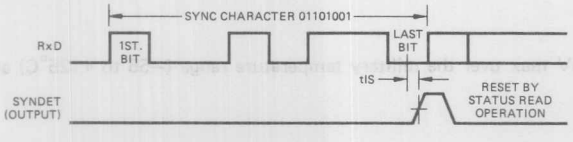



### RxRDY TIMING (ASYNC MODE)

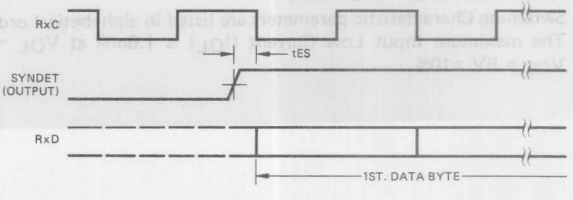



MOS-223

### INTERNAL SYNC DETECT (SYNC MODE ONLY)




### EXTERNAL SYNC DETECT (SYNC MODE ONLY)




MOS-224

# Am8253/Am8253-5

## Programmable Interval Timer

### ADVANCED INFORMATION

### DISTINCTIVE CHARACTERISTICS

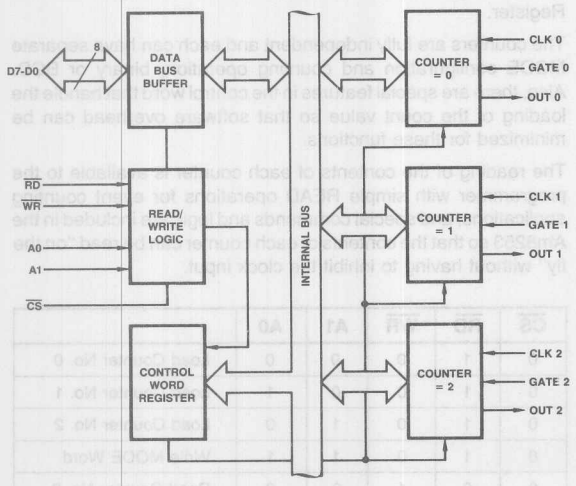
- Count binary or BCD
- Single +5V supply
- 24-pin dual-in-line package
- Three independent 16-bit counters
- DC to 2.5MHz
- Programmable counter modes
- Bus oriented I/O
- 100% reliability assurance testing to MIL-STD-883

### GENERAL DESCRIPTION

The Am8253/Am8253-5 are programmable counter/timer chips designed for use as Am8080A/Am8085A Family peripherals. They use NMOS technology with a single +5V supply and are direct replacements for Intel's 8253/8253-5.

Each device is organized as three independent 16-bit counters, each counter having a rate of up to 2.5MHz. All modes of operation are software programmable. For improved performance, see **Am9513 System Timing Controller.**

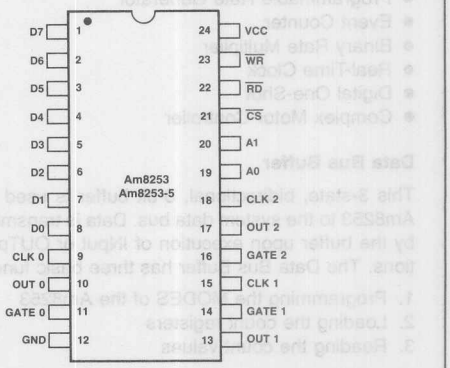
### BLOCK DIAGRAM




MOS-153

### CONNECTION DIAGRAM
Top View

Note: Pin 1 is marked for orientation.




### PIN NAMES

| | |
|---|---|
| D7-D0 | Data bus (8-bit) |
| CLK N | Counter clock inputs |
| GATE N | Counter gate inputs |
| OUT N | Counter outputs |
| $\overline{RD}$ | Read counter |
| $\overline{WR}$ | Write command or data |
| $\overline{CS}$ | Chip select |
| A0-A1 | Counter select |
| VCC | +5 Volts |
| GND | Ground |

MOS-154

### ORDERING INFORMATION

| Package Type | Ambient Temperature | Order Numbers | |
|---|---|---|---|
| Molded DIP | 0°C ≤ $T_A$ ≤ +70°C | AM8253PC/P8253 | AM8253-5PC/P8253-5 |
| Hermetic DIP* | | AM8253DC/D8253<br>AM8253CC/C8253 | AM8253-5DC/D8253-5<br>AM8253-5CC/C8253-5 |

*Hermetic = Ceramic = DC = CC = D-24-1.

## FUNCTIONAL DESCRIPTION

### General

The Am8253 is a programmable interval timer/counter specifically designed for use with the Am9080A Microcomputer systems. Its function is that of a general-purpose, multitiming element that can be treated as an array of I/O ports in the system software.

The Am8253 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in systems software, the programmer configures the Am8253 to match his requirements, initializes one of the counters of the Am8253 with the desired quantity, then upon command the Am8253 will count out the delay and interrupt the CPU when it has completed its tasks. It is easy to see that the software overhead is minimal and that multiple delays can easily be maintained by assignment of priority levels.

Other counter/timer functions that are non-delay in nature, but also common to most microcomputers can be implemented with the Am8253.

- Programmable Rate Generator
- Event Counter
- Binary Rate Multiplier
- Real-Time Clock
- Digital One-Shot
- Complex Motor Controller

### Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the Am8253 to the system data bus. Data is transmitted or received by the buffer upon execution of INput or OUTput CPU instructions. The Data Bus Buffer has three basic functions.

1. Programming the MODES of the Am8253
2. Loading the count registers
3. Reading the count values

### Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and in turn generates control signals for overall device operation. It is enabled or disabled by CS so that no operation can occur to change the function unless the device has been selected by the system logic.

### $\overline{RD}$ (Read)

A "low" on this input informs the Am8253 that the CPU is inputting data in the form of a counters value.

### $\overline{WR}$ (Write)

A "low" on this input informs the Am8253 that the CPU is outputting data in the form of MODE information or loading counters.

### A0, A1

These inputs are normally connected to the address bus. Their function is to select one of the three counters to be operated on and to address the control word register for MODE selection.

### $\overline{CS}$ (Chip Select)

A "low" on this input enables the Am8253. No reading or writing will occur unless the devices is selected. The $\overline{CS}$ input has no effect upon the actual operation of the counter.

### Control Word Register

The Control Word Register is selected when A0, A1 are 11. It then accepts information from the data bus buffer and stores it in a register. The information stored in this register controls the operational MODE of each counter, selection of binary or BCD counting and the loading of each count register.

The Control Word Register can only be written into; no read operation of its contents is available.

### Counter #0, Counter #1, Counter #2

These three functional blocks are identical in operation so only a single Counter will be described. Each Counter consists of a single, 16-bit, presettable, DOWN counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of MODES stored in the Control Word Register.

The counters are fully independent and each can have separate MODE configuration and counting operation, binary or BCD. Also, there are special features in the control word that handle the loading of the count value so that software overhead can be minimized for these functions.

The reading of the contents of each counter is available to the programmer with simple READ operations for event counting applications, and special commands and logic are included in the Am8253 so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

| $\overline{CS}$ | $\overline{RD}$ | $\overline{WR}$ | A1 | A0 | |
|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | Load Counter No. 0 |
| 0 | 1 | 0 | 0 | 1 | Load Counter No. 1 |
| 0 | 1 | 0 | 1 | 0 | Load Counter No. 2 |
| 0 | 1 | 0 | 1 | 1 | Write MODE Word |
| 0 | 0 | 1 | 0 | 0 | Read Counter No. 0 |
| 0 | 0 | 1 | 0 | 1 | Read Counter No. 1 |
| 0 | 0 | 1 | 1 | 0 | Read Counter No. 2 |
| 0 | 0 | 1 | 1 | 1 | No-Operation 3-State |
| 1 | X | X | X | X | Disable 3-State |
| 0 | 1 | 1 | X | X | No-Operation 3-State |

## OPERATIONAL DESCRIPTION

### General

The complete functional definition of the Am8253 is programmed by the systems software. A set of control words must be sent out by the CPU to initialize each counter of the Am8253 with the desired MODE and quantity information. These control words program the MODE, Loading sequence and selection of binary or BCD counting.

Once programmed, the Am8253 is ready to perform whatever timing tasks it is assigned to accomplish.

The actual counting operation of each counter is completely independent and additional logic is provided on-chip so that the usual problems associated with efficient monitoring and management of external, asynchronous events or rates to the microcomputer system have been eliminated.

### Programming the Am8253

All of the MODES for each counter are programmed by the systems software by simple I/O operations.

Each counter of the Am8253 is individually programmed by writing a control word into the Control Word Register (A0, A1 = 11).

### Control Word Format

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| SC1 | SC0 | RL1 | RL0 | M2 | M1 | M0 | BCD |

### Definition of Control

**SC – Select Counter:**

| SC1 | SC0 | |
|---|---|---|
| 0 | 0 | Select Counter 0 |
| 0 | 1 | Select Counter 1 |
| 1 | 0 | Select Counter 2 |
| 1 | 1 | Illegal |

**RL – Read/Load:**

| RL1 | RL0 | |
|---|---|---|
| 0 | 0 | Counter Latching operation. |
| 1 | 0 | Read/Load most significant byte only. |
| 0 | 1 | Read/Load least significant byte only. |
| 1 | 1 | Read/Load least significant byte first, then most significant byte. |

**M – MODE:**

| M2 | M1 | M0 | |
|---|---|---|---|
| 0 | 0 | 0 | MODE 0 |
| 0 | 0 | 1 | MODE 1 |
| X | 1 | 0 | MODE 2 |
| X | 1 | 1 | MODE 3 |
| 1 | 0 | 0 | MODE 4 |
| 1 | 0 | 1 | MODE 5 |

**BCD:**

| | |
|---|---|
| 0 | Binary Counter 16-bits |
| 1 | Binary Coded Decimal (BCD) Counter (4 Decades) |

### Counter Loading

The count register is not loaded until the count value is written (one or two bytes, depending on the mode selected by the RL bits), followed by a rising edge and a falling edge of the clock. Any read of the counter prior to that falling clock edge may yield invalid data.

### MODE DEFINITION

#### MODE 0: Interrupt on Terminal Count

The output will be initially low after the mode set operation. After the count is loaded into the selected count register, the output will remain low and the counter will count. When terminal count is reached the output will go high and remain high until the selected count register is reloaded with the mode or a new count is loaded. The counter continues to decrement after terminal count has been reached.

Rewriting a counter register during counting results in the following:

1. Write 1st byte stops the current counting.
2. Write 2nd byte starts the new count.

#### MODE 1: Programmable One-Shot

The output will go low on the count following the rising edge of the gate input.

The output will go high on the terminal count. If a new count value is loaded while the output is low it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

#### MODE 2: Rate Generator

Divide by N counter. The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. Thus, the gate input can be used to synchronize the counter.

When this mode is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

#### MODE 3: Square Wave Rate Generator

Similar to MODE 2 except that the output will remain high until one half the count has been completed (for even numbers) and go low for the other half of the count. This is accomplished by decrementing the counter by two on the falling edge of each clock pulse. When the counter reaches terminal count, the state of the output is changed and the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by one. Subsequent clock pulses decrement the clock by two. After timeout, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by three. Subsequent clock pulses decrement the count by two until timeout. Then the whole process is repeated. In this way, if the count is odd, the output will be high for (N + 1)/2 counts and low for (N – 1)/2 counts.

7

### MODE 4: Software-Triggered Strobe

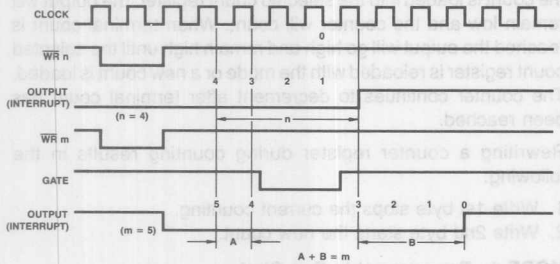
After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value. The count will be inhibited while the gate input is low. Reloading the counter register will restart counting beginning with the new number.

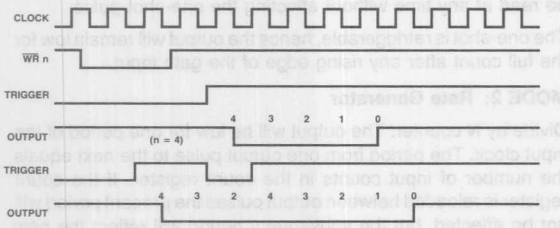
### MODE 5: Hardware-Triggered Strobe

The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of any trigger.

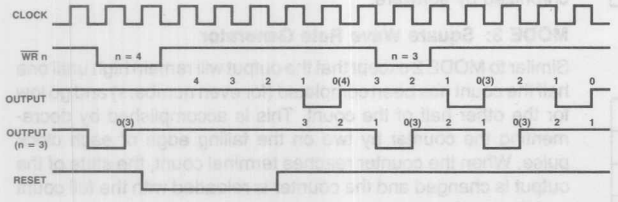
**MODE 0. Interrupt on Terminal Count.**



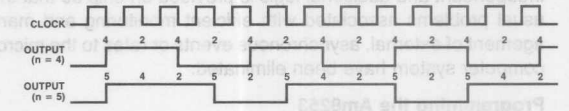

**MODE 1. Programmable One-Shot.**



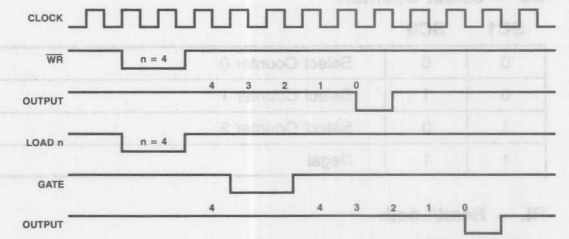

**MODE 2. Rate Generator.**




**MODE 3. Square Wave Generator.**




**MODE 4. Software-Triggered Strobe.**




**MODE 5. Hardware-Triggered Strobe.**

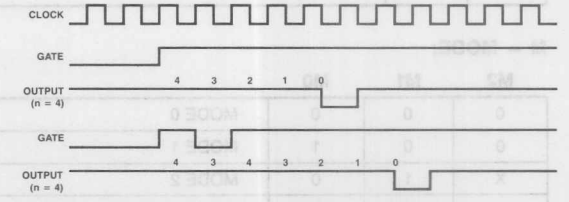



**Figure 1. Am8253 Timing Diagrams.**

## MAXIMUM RATINGS above which useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65 to +150°C |
| Ambient Temperature Under Bias | 0 to 70°C |
| Voltage On Any Pin with Respect to Ground | −0.5V to +7.0V |
| Power Dissipation | 1W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## DC CHARACTERISTICS ($T_A$ = 0 to 70°C; VCC = 5.0V ±5% unless otherwise specified)

| Parameter | Description | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| VIL | Input Low Voltage | | −0.5 | | 0.8 | Volts |
| VIH | Input High Voltage | | 2.2 | | VCC+.5V | Volts |
| VOL | Output Low Voltage | Note 1 | | | 0.45 | Volts |
| VOH | Output High Voltage | Note 2 | 2.4 | | | Volts |
| IIL | Input Load Current | VIN = VCC to 0V | | | ±10 | μA |
| IOFL | Output Float Leakage | VOUT = VCC to 0V | | | ±10 | μA |
| ICC | VCC Supply Current | | | | 140 | mA |

Notes: 1. Am8253, IOL = 1.6mA; Am8253-5, IOL = 2.2mA.
2. Am8253, IOH = −150μA; Am8253-5, IOH = −400μA.

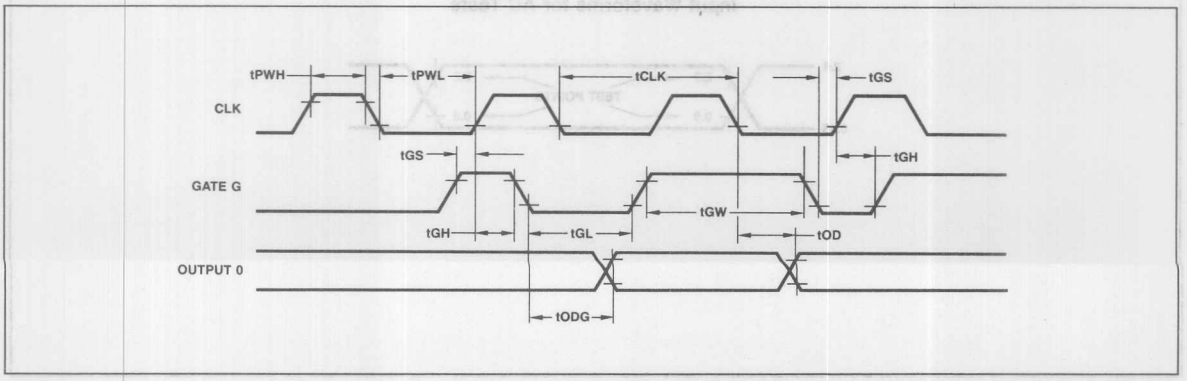
## CAPACITANCE $T_A$ = 25°C; VCC = GND = 0V

| Parameter | Description | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| CIN | Input Capacitance | fc = 1MHz | | | 10 | pF |
| CI/O | I/O Capacitance | Unmeasured pins returned to VSS | | | 20 | pF |

## CLOCK AND GATE TIMING

| Parameter | Description | Am8253 Min | Am8253 Max | Am8253-5 Min | Am8253-5 Max | Units |
|---|---|---|---|---|---|---|
| tCLK | Clock Period | 380 | dc | 380 | dc | ns |
| tPWH | High Pulse Width | 230 | | 230 | | ns |
| tPWL | Low Pulse Width | 150 | | 150 | | ns |
| tGW | Gate Width High | 150 | | 150 | | ns |
| tGL | Gate Width Low | 100 | | 100 | | ns |
| tGS | Gate Set Up Time to CLK↑ | 100 | | 100 | | ns |
| tGH | Gate Hold Time After CLK↑ | 50 | | 50 | | ns |
| tOD | Output Delay From CLK↓ (Note 1) | | 400 | | 400 | ns |
| tODG | Output Delay From Gate↓ (Note 1) | | 300 | | 300 | ns |

Note: 1. Test Conditions: Am8253: CL = 100pF; Am8253-5: CL = 150pF.



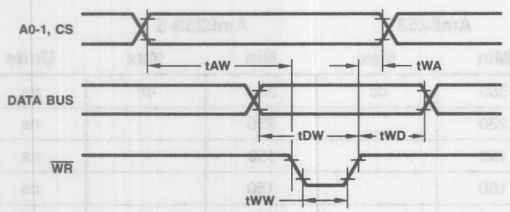
## AC CHARACTERISTICS ($T_A$ = 0 to 70°C; VCC = 5.0V ±5%; GND = 0V)

### Bus Parameters (Note 1)

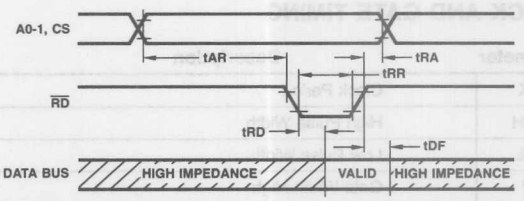
| Parameter | Description | Am8253 Min | Am8253 Max | Am8253-5 Min | Am8253-5 Max | Units |
|---|---|---|---|---|---|---|
| **Read Cycle:** | | | | | | |
| tAR | Address Stable Before $\overline{READ}$ | 50 | | 30 | | ns |
| tRA | Address Hold Time for $\overline{READ}$ | 5 | | 5 | | ns |
| tRR | $\overline{READ}$ Pulse Width | 400 | | 300 | | ns |
| tRD | Data Delay From $\overline{READ}$ (Note 2) | | 300 | | 200 | ns |
| tDF | $\overline{READ}$ to Data Floating | 25 | 125 | 25 | 100 | ns |
| tRV | Recovery Time Between READ and Any Other Control Signal | 1 | | 1 | | μs |
| **Write Cycle:** | | | | | | |
| tAW | Address Stable Before $\overline{WRITE}$ | 50 | | 30 | | ns |
| tWA | Address Hold Time for $\overline{WRITE}$ | 30 | | 30 | | ns |
| tWW | $\overline{WRITE}$ Pulse Width | 400 | | 300 | | ns |
| tDW | Data Set Up Time for $\overline{WRITE}$ | 300 | | 250 | | ns |
| tWD | Data Hold Time for $\overline{WRITE}$ | 40 | | 30 | | ns |
| tRV | Recovery Time Between $\overline{WRITE}$ and Any Other Control Signal | 1 | | 1 | | μs |

Notes: 1. AC timings measured at VOH = 2.2, VOL = 0.8.
2. Test Conditions: Am8253, CL = 100pF, Am8253-5: CL = 150pF.

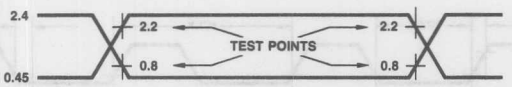
**Write Timing**




**Read Timing**




**Input Waveforms for AC Tests**



# Am8255A/8255A-5

## Programmable Peripheral Interface

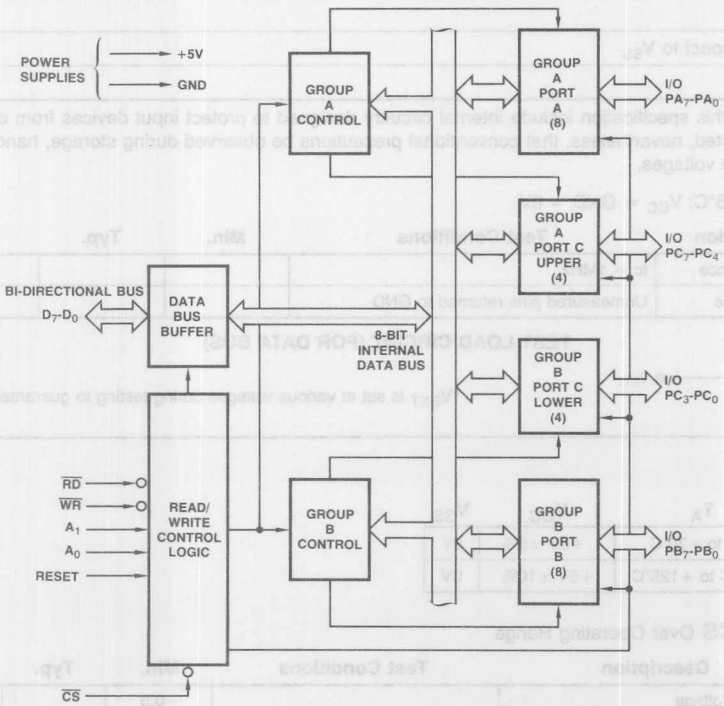
### DISTINCTIVE CHARACTERISTICS

- Direct bit set/reset capability easing control application interface
- Reduces system package count
- Improved DC driving capability
- 24 programmable I/O pins
- Completely TTL compatible
- Fully compatible with 8080A and 8085A microprocessor families
- Improved timing characteristics
- Military version available

### GENERAL DESCRIPTION

The Am8255A is a general purpose programmable I/O device designed for use with Am8080A and Am8085A microprocessors. It has 24 I/O pins which may be individually programmed in two groups of twelve and used in three major modes of operation. In the first mode, each group of twelve I/O pins may be programmed in sets of 4 and 8 to be input or output. In Mode 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining four pins three are used for handshaking and interrupt control signals. The third mode of operation (Mode 2) is a bi-directional bus mode which uses eight lines for a bi-directional bus, and five lines, borrowing one from the other group, for handshaking.

### Am8255A BLOCK DIAGRAM



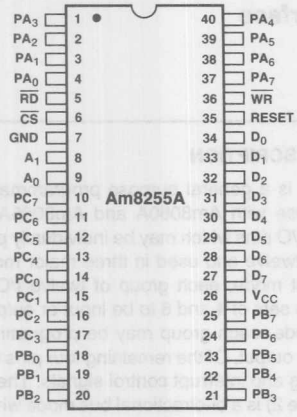

MOS-107

### ORDERING INFORMATION

| Package Type | Ambient Temperature Specification | Order Numbers | |
|---|---|---|---|
| Hermetic DIP* | 0°C ≤ $T_A$ ≤ +70°C | AM8255ADC<br>AM8255ACC | AM8255A-5DC<br>AM8255A-5CC |
| Molded DIP | | AM8255APC | AM8255A-5PC |
| Hermetic DIP | −55°C ≤ $T_A$ ≤ +125°C | AM9555ADM/M8255A | |

*Hermetic = Ceramic = DC = CC = D-40-1.

**CONNECTION DIAGRAM – Top View**




MOS-108

**PIN NAMES**

| | |
|---|---|
| $D_7$-$D_0$ | Data Bus (Bi-Directional) |
| Reset | Reset Input |
| $\overline{CS}$ | Chip Select |
| $\overline{RD}$ | Read Input |
| $\overline{WR}$ | Write Input |
| $A_0$, $A_1$ | Port Address |
| $PA_7$-$PA_0$ | Port A (Bit) |
| $PB_7$-$PB_0$ | Port B (Bit) |
| $PC_7$-$PC_0$ | Port C (Bit) |
| $V_{CC}$ | +5 Volts |
| GND | 0 Volts |

## MAXIMUM RATINGS above which useful life may be impaired

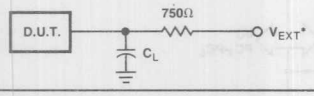
| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| $V_{CC}$ with Respect to $V_{SS}$ | −0.5V to +7.0V |
| All Signal Voltages with Respect to $V_{SS}$ | −0.5V to +7.0V |
| Power Dissipation | 1.0W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## CAPACITANCE $T_A$ = 25°C; $V_{CC}$ = GND = 0V

| Parameter | Description | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | fc = 1MHz | | | 10 | pF |
| $C_{I/O}$ | I/O Capacitance | Unmeasured pins returned to GND | | | 20 | pF |

**TEST LOAD CIRCUIT (FOR DATA BUS)**




*$V_{EXT}$ is set at various voltages during testing to guarantee the specification.

## OPERATING RANGE

| Part Number | $T_A$ | $V_{CC}$ | $V_{SS}$ |
|---|---|---|---|
| Am8255ACC/PC | 0°C to +70°C | +5V ±5% | 0V |
| Am9555ADM | −55°C to +125°C | +5V ±10% | 0V |

## DC CHARACTERISTICS Over Operating Range

| Parameter | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | | −0.5 | | 0.8 | Volts |
| $V_{IH}$ | Input High Voltage | | 2.0 | | $V_{CC}$ | Volts |
| $V_{OL}$(DB) | Output Low Voltage (Data Bus) | $I_{OL}$ = 2.5mA | | | 0.45 | Volts |
| $V_{OL}$(PER) | Output Low Voltage (Peripheral Port) | $I_{OL}$ = 1.7mA | | | 0.45 | Volts |
| $V_{OH}$(DB) | Output High Voltage (Data Bus) | $I_{OH}$ = −400μA | 2.4 | | | Volts |
| $V_{OH}$(PER) | Output High Voltage (Peripheral Port) | $I_{OH}$ = −200μA | 2.4 | | | Volts |
| $I_{DAR}$ (Note 1) | Darlington Drive Current | $R_{EXT}$ = 750Ω; $V_{EXT}$ = 1.5V | −1.0 | | −4.0 | mA |
| $I_{CC}$ | Power Supply Current | | | | 120 | mA |
| $I_{IL}$ | Input Load Current | $V_{IN}$ = $V_{CC}$ to 0V | | | ±10 | μA |
| $I_{OFL}$ | Output Float Leakage | $V_{OUT}$ = $V_{CC}$ to 0V | | | ±10 | μA |

Note 1: Available on any 8 pins from Port B and C.

## AC CHARACTERISTICS Over Operating Range

### BUS PARAMETERS:

**Read:**

| Parameter | Description | Am8255A Min. | Am8255A Max. | Am8255A-5 Min. | Am8255A-5 Max. | Am9555ADM Min. | Am9555ADM Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{AR}$ | Address Stable Before READ | 0 | | 0 | | 0 | | ns |
| $t_{RA}$ | Address Stable After READ | 0 | | 0 | | 0 | | ns |
| $t_{RR}$ | READ Pulse Width | 300 | | 300 | | 300 | | ns |
| $t_{RD}$ | Data Valid From READ (Note 1) | | 250 | | 200 | | 250 | ns |
| $t_{DF}$ | Data Float After READ | 10 | 150 | 10 | 100 | 10 | 150 | ns |
| $t_{RV}$ | Time Between READs and/or WRITEs | 850 | | 850 | | 850 | | ns |

**Write:**

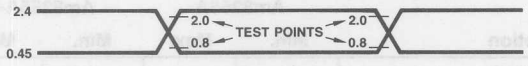
| Parameter | Description | Am8255A Min. | Am8255A Max. | Am8255A-5 Min. | Am8255A-5 Max. | Am9555ADM Min. | Am9555ADM Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{AW}$ | Address Stable Before WRITE | 0 | | 0 | | 0 | | ns |
| $t_{WA}$ | Address Stable After WRITE | 20 | | 20 | | 20 | | ns |
| $t_{WW}$ | WRITE Pulse Width | 400 | | 300 | | 400 | | ns |
| $t_{DW}$ | Data Valid to WRITE (T.E.) | 100 | | 100 | | 100 | | ns |
| $t_{WD}$ | Data Valid After WRITE | 30 | | 30 | | 30 | | ns |

**Other Timings:**

| Parameter | Description | Am8255A Min. | Am8255A Max. | Am8255A-5 Min. | Am8255A-5 Max. | Am9555ADM Min. | Am9555ADM Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{WB}$ | WR = 1 to Output (Note 1) | | 350 | | 350 | | 350 | ns |
| $t_{IR}$ | Peripheral Data Before RD | 0 | | 0 | | 0 | | ns |
| $t_{HR}$ | Peripheral Data After RD | 0 | | 0 | | 0 | | ns |
| $t_{AK}$ | ACK Pulse Width | 300 | | 300 | | 300 | | ns |
| $t_{ST}$ | STB Pulse Width | 500 | | 500 | | 500 | | ns |
| $t_{PS}$ | Per. Data Before T.E. of STB | 0 | | 0 | | 0 | | ns |
| $t_{PH}$ | Per. Data After T.E. of STB | 180 | | 180 | | 180 | | ns |
| $t_{AD}$ | ACK = 0 to Output (Note 1) | | 300 | | 300 | | 300 | ns |
| $t_{KD}$ | ACK = 1 to Output Float | 20 | 250 | 20 | 250 | 20 | 250 | ns |
| $t_{WOB}$ | WR = 1 to OBF = 0 (Note 1) | | 650 | | 650 | | 650 | ns |
| $t_{AOB}$ | ACK = 0 to OBF = 1 (Note 1) | | 350 | | 350 | | 350 | ns |
| $t_{SIB}$ | STB = 0 to IBF = 1 (Note 1) | | 300 | | 300 | | 300 | ns |
| $t_{RIB}$ | RD = 1 to IBF = 0 (Note 1) | | 300 | | 300 | | 300 | ns |
| $t_{RIT}$ | RD = 0 to INTR = 0 (Note 1) | | 400 | | 400 | | 400 | ns |
| $t_{SIT}$ | STB = 1 to INTR = 1 (Note 1) | | 300 | | 300 | | 300 | ns |
| $t_{AIT}$ | ACK = 1 to INTR = 1 (Note 1) | | 350 | | 350 | | 350 | ns |
| $t_{WIT}$ | WR = 0 to INTR = 0 (Note 1) | | 850 | | 850 | | 850 | ns |

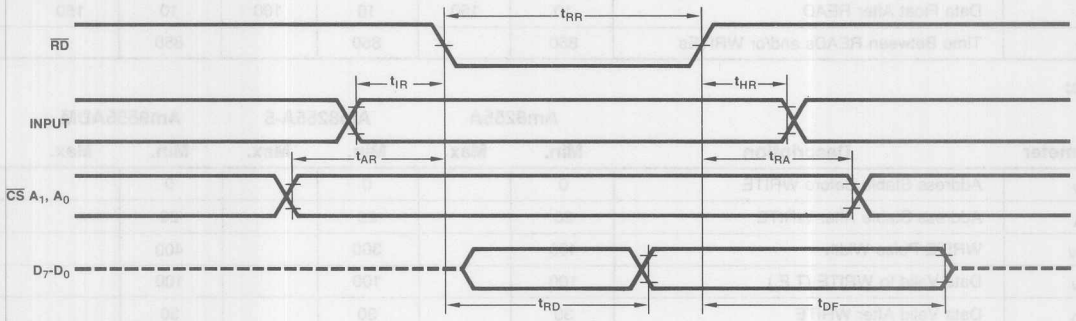
Notes: 1. Test Conditions: Am8255A/Am9555ADM: $C_L$ = 100pF; Am8255A-5: $C_L$ = 150pF.
2. Period of Reset pulse must be at least 50$\mu$s during or after power on. Subsequent Reset pulse can be 500ns min.

7



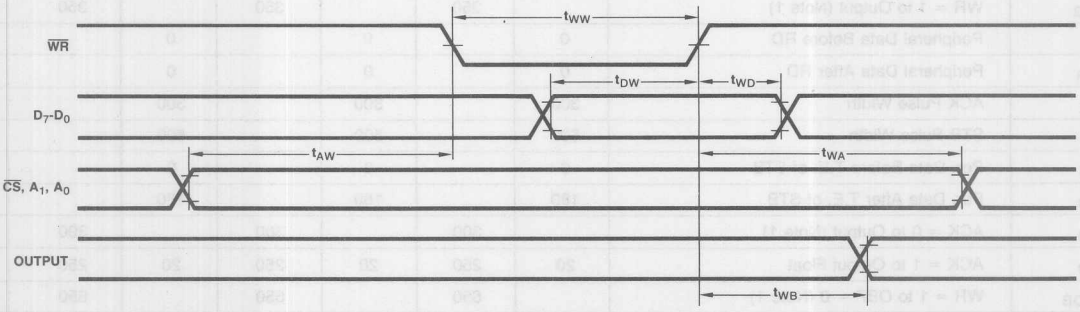

**Input Waveforms For A.C. Tests**

MOS-109



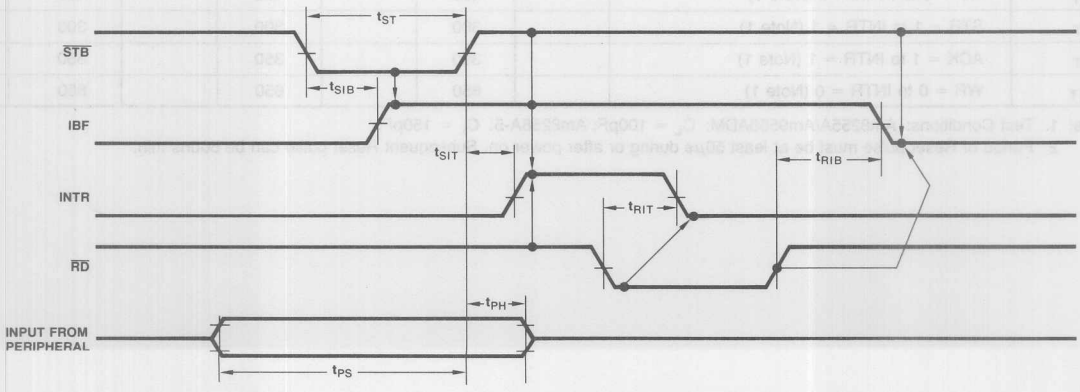

**Mode 0 (Basic Input)**

MOS-110




**Mode 0 (Basic Output)**

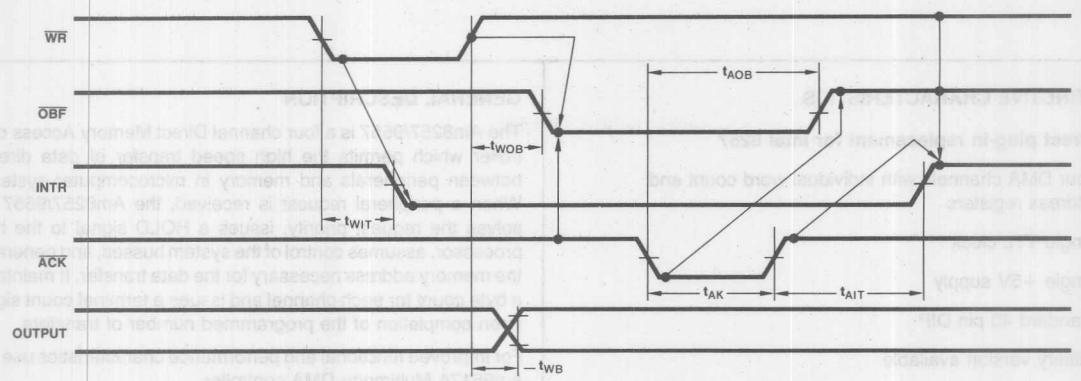
MOS-111




**Mode 1 (Strobed Input)**

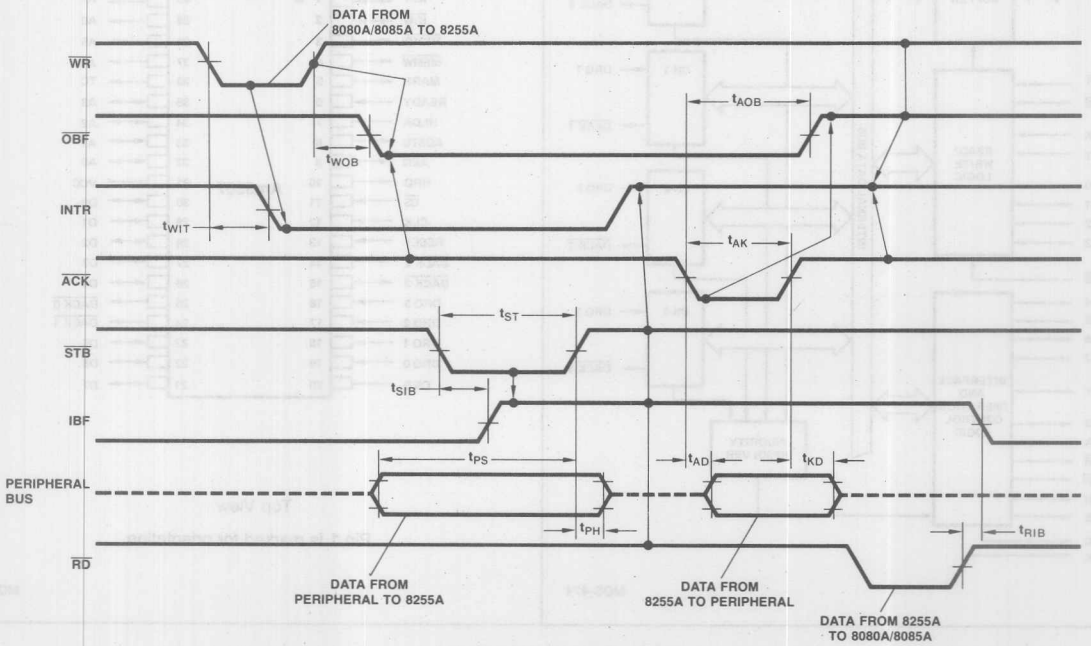
MOS-112

## WAVEFORMS (Cont.)




**Mode 1 (Strobed Output)**

MOS-113




Note: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
($INTR = IBF \cdot \overline{MASK} \cdot \overline{STB} \cdot \overline{RD} + \overline{OBF} \cdot \overline{MASK} \cdot \overline{ACK} \cdot \overline{WR}$)

**Mode 2 (Bi-directional)**

MOS-114

7

# Am8257/9557

## Programmable DMA Controller

### DISTINCTIVE CHARACTERISTICS

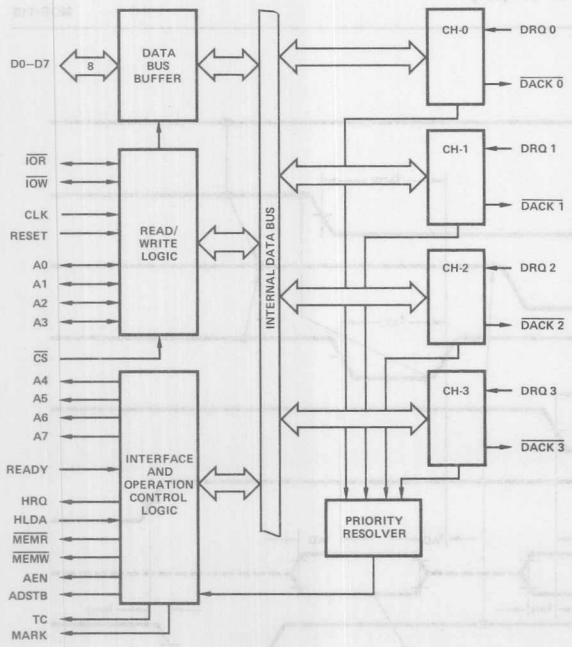
- **Direct plug-in replacement for Intel 8257**
- Four DMA channels with individual word count and address registers
- Single TTL clock
- Single +5V supply
- Standard 40 pin DIP
- Military version available
- 100% MIL-STD-883 reliability assurance testing

### GENERAL DESCRIPTION

The Am8257/9557 is a four channel Direct Memory Access controller which permits the high speed transfer of data directly between peripherals and memory in microcomputer systems. When a peripheral request is received, the Am8257/9557 resolves the request priority, issues a HOLD signal to the host processor, assumes control of the system busses, and generates the memory address necessary for the data transfer. It maintains a byte count for each channel and issues a terminal count signal upon completion of the programmed number of transfers.

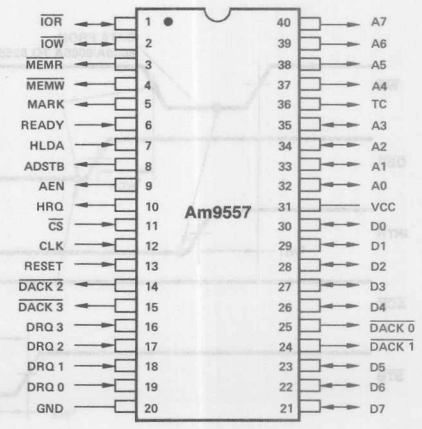
For improved functional and performance characteristics use the Am9517A Multimode DMA controller.

### BLOCK DIAGRAM




MOS-474

### CONNECTION DIAGRAM




Top View

Pin 1 is marked for orientation.

MOS-475

### ORDERING INFORMATION

| Package Type | Ambient Temperature | Order Number |
|---|---|---|
| Molded DIP | $0°C \leq T_A \leq +70°C$ | AM9557PC/P8257 |
| Hermetic DIP* | | AM9557DC/D8257<br>AM9557CC/C8257 |
| Hermetic DIP | $-55°C \leq T_A \leq +125°C$ | AM9557DM |

*Hermetic = Ceramic = DC = CC = D-40-1.

## MAXIMUM RATINGS above which useful life may be impaired

| | |
|---|---|
| Ambient Temperature Under Bias | 0 to 70°C |
| Storage Temperature | −65 to +150°C |
| Voltage on Any Pin with Respect to Ground | −0.5 to +7.0V |
| Power Dissipation | 1.0W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## DC CHARACTERISTICS ($T_A$ = 0 to 70°C, VCC = +5.0V ±5%, GND = 0V)

| Parameters | Description | Test Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| VIL | Input Low Voltage | | −0.5 | 0.8 | Volts |
| VIH | Input High Voltage | | 2.0 | VCC+.5 | Volts |
| VOL | Output Low Voltage | IOL = 1.6mA | | 0.45 | Volts |
| VOH | Output High Voltage | IOH = −150μA for AB, DB and AEN<br>IOH = −80μA for Others | 2.4 | VCC | Volts |
| VHH | HRQ Output High Voltage | IOH = −80μA | 3.3 | VCC | Volts |
| ICC | VCC Current Drain | | | 120 | mA |
| IIL | Input Leakage | VIN = VCC to 0V | | ±10 | μA |
| IOFL | Output Leakage During Float | VOUT = VCC to 0V | | ±10 | μA |

## CAPACITANCE ($T_A$ = 25°C; VCC = GND = 0V)

| Parameters | Description | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| CIN | Input Capacitance | fc = 1MHz | | | 10 | pF |
| CI/O | I/O Capacitance | Unmeasured Pins Returned to GND | | | 20 | pF |

7

## AC CHARACTERISTICS: PERIPHERAL (SLAVE) MODE ($T_A$ = 0 to 70°C, VCC = 5.0V ±5%, GND = 0V, Note 1)

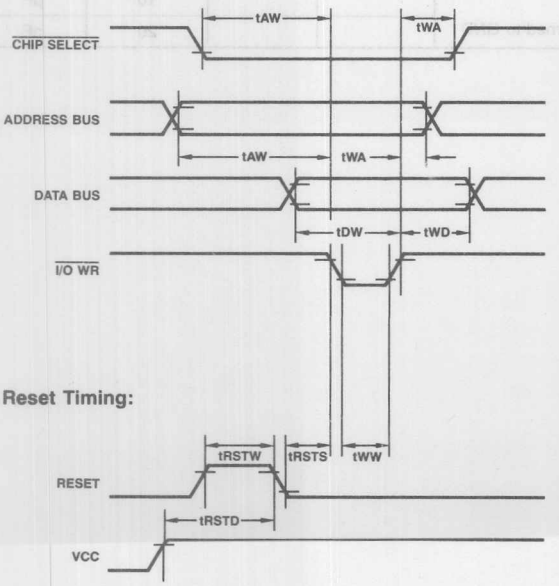
### Am9080A Bus Parameters

| Parameters | Description | Test Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| **Read Cycle:** | | | | | |
| tAR | Address or $\overline{CS}\downarrow$ Setup to $\overline{RD}\downarrow$ | | 0 | | ns |
| tRA | Address of $\overline{CS}\uparrow$ Hold from $\overline{RD}\uparrow$ | | 0 | | ns |
| tRD | Data Access from $\overline{RD}\downarrow$ | Note 2 | 0 | 300 | ns |
| tDF | DB → Float Delay from $\overline{RD}\uparrow$ | | 20 | 150 | ns |
| tRR | $\overline{RD}$ Width | | 250 | | ns |
| **Write Cycle:** | | | | | |
| tAW | Address Setup to $\overline{WR}\downarrow$ | | 20 | | ns |
| tWA | Address Hold from $\overline{WR}\uparrow$ | | 20 | | ns |
| tDW | Data Setup to $\overline{WR}\uparrow$ | | 200 | | ns |
| tWD | Data Hold from $\overline{WR}\uparrow$ | | 20 | | ns |
| tWW | $\overline{WR}$ Width | | 200 | | ns |
| **Other Timing:** | | | | | |
| tRSTW | Reset Pulse Width | | 300 | | ns |
| tRSTD | Power Supply↑ (VCC) Setup to Reset↓ | | 500 | | μs |
| tr | Signal Rise Time | | | 20 | ns |
| tf | Signal Fall Time | | | 20 | ns |
| tRSTS | Reset to First $\overline{I/O}\overline{WR}$ | | 2 | | tCY |

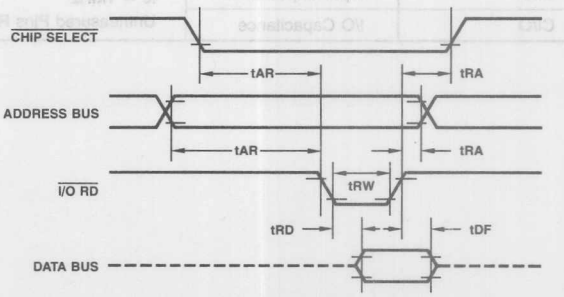
Notes: 1. All timing measurements are made at the following reference voltages unless otherwise specified: Input "1" at 2.0V, "0" at 0.8V, Output "1" at 2.0V, "0" at 0.8V.
2. CL = 100pF.

## PERIPHERAL MODE TIMING DIAGRAMS

**Write Timing:**



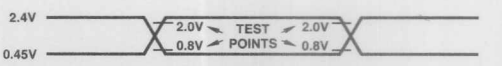

**Read Timing:**




**Reset Timing:**




**Input Waveform for AC Tests:**




MOS-511

## AC CHARACTERISTICS: DMA (MASTER) MODE ($T_A$ = 0 to 70°C, VCC = 5.0V ±5%, GND = 0V)

**Timing Requirements**

| Parameters | Description | Min | Max | Units |
|---|---|---|---|---|
| tCY | Cycle Time (Period) | 0.320 | 4 | μs |
| tθ | Clock Active (High) | 120 | .8tCY | ns |
| tQS | DRQ↑ Setup to θ↓ (S1, S4) | 120 | | ns |
| tQC | DRQ↓ Hold from CLK↓ (S1) | 0 | | ns |
| tHS | HLDA↑ or ↓Setup to θ↓ (S1, S4) | 100 | | ns |
| tRS | READY Setup Time to θ↑ (S3, Sw) | 30 | | ns |
| tRH | READY Hold Time from θ↑ (S3, Sw) | 20 | | ns |

### TRACKING PARAMETERS

Signals labeled as Tracking Parameters (footnotes 4-7 under AC Specifications) are signals that follow similar paths through the silicon die. The propagation speed of these signals varies in the manufacturing process but the relationship between all these parameters is constant. The variation is less than or equal to 50ns.

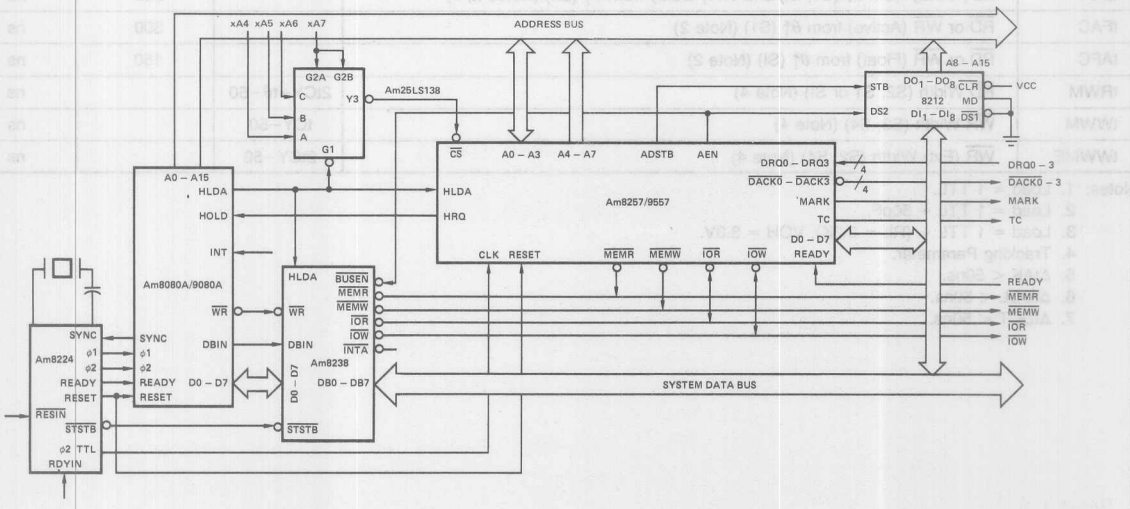
Suppose the following timing equation is being evaulated,

$$TA(MIN) + TB(MAX) \leq 150ns$$

and only minimum specifications exist for TA and TB. If TA(MIN) is used, and if TA and TB are tracking parameters, TB(MAX) can be taken as TB(MIN) + 50ns.

$$TA(MIN) + (TB(MIN)^* + 50ns) \leq 150ns$$

*If TA and TB are tracking parameters.




**Basic DMA Configuration.** MOS-476

## AC CHARACTERISTICS: DMA (MASTER) MODE ($T_A$ = 0 to 70°C, VCC = 5.0V ±5%, GND = 0V)

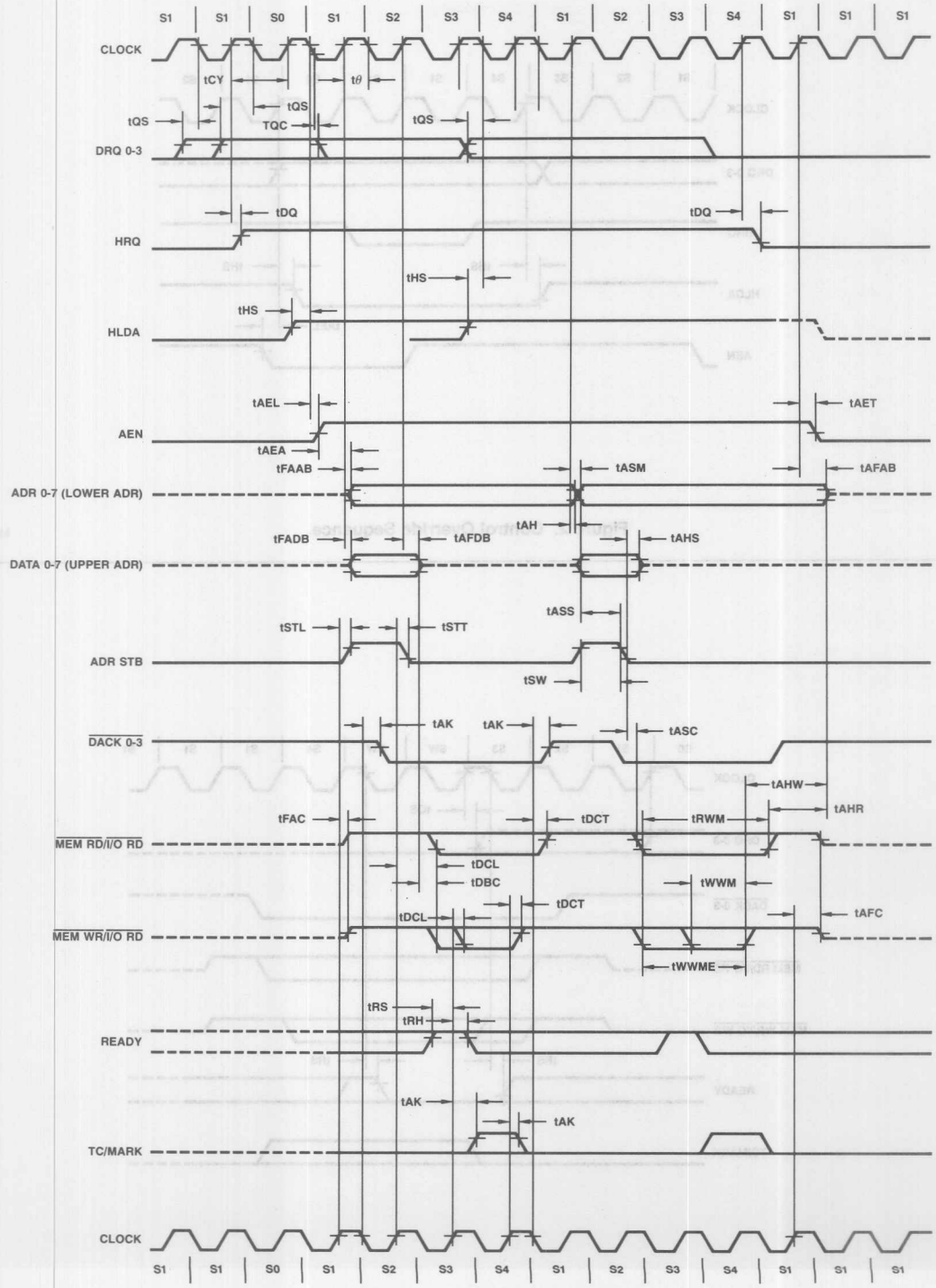
### Timing Requirements

| Parameters | Description | Min | Max | Units |
|---|---|---|---|---|
| tDQ | HRQ↑ or ↓Delay from θ↑ (SI, S4) (Measured at 2.0V) (Note 1) | | 160 | ns |
| tDQ1 | HRQ↑ or ↓Delay from θ↑ (SI, S4) (Measured at 3.3V) (Note 3) | | 250 | ns |
| tAEL | AEN↑ Delay from θ↓ (S1) (Note 1) | | 300 | ns |
| tAET | AEN↓ Delay from θ↑ (SI) (Note 1) | | 200 | ns |
| tAEA | Address (AB) (Active) Delay from AEN↑ (S1) (Note 4) | 20 | | ns |
| tFAAB | Address (AB) (Active) Delay from θ↑ (S1) (Note 2) | | 250 | ns |
| tAFAB | Address (AB) (Float) Delay from θ↑ (SI) (Note 2) | | 150 | ns |
| tASM | Address (AB) (Stable) Delay from θ↑ (S1) (Note 2) | | 250 | ns |
| tAH | Address (AB) (Stable) Hold from θ↑ (S1) (Note 2) | tASM−50 | | ns |
| tAHR | Address (AB) (Valid) Hold from $\overline{RD}$↑ (S1, SI) (Note 4) | 60 | | ns |
| tAHW | Address (AB) (Valid) Hold from $\overline{WR}$↑ (S1, SI) (Note 4) | 300 | | ns |
| tFADB | Address (DB) (Active) Delay from θ↑ (S1) (Note 2) | | 300 | ns |
| tAFDB | Address (DB) (Float) Delay from θ↑ (S2) (Note 2) | tSTT+20 | 250 | ns |
| tASS | Address (DB) Setup to Address Stable↓ (S1, S2) (Note 4) | 100 | | ns |
| tAHS | Address (DB) (Valid) Hold from Address Stable↓ (S2) (Note 4) | 50 | | ns |
| tSTL | Address Stable↑ Delay from θ↑ (S1) (Note 1) | | 200 | ns |
| tSTT | Address Stable↓ Delay from θ↑ (S2) (Note 1) | | 140 | ns |
| tSW | Address Stable Width (S1, S2) (Note 4) | tCY−100 | | ns |
| tASC | $\overline{RD}$↓ or $\overline{WR}$ (Ext)↓ Delay from Address Stable↓ (S2) (Note 4) | 70 | | ns |
| tDBC | $\overline{RD}$↓ or $\overline{WR}$ (Ext)↓ Delay from Address (DB) (Float) (S2) (Note 4) | 20 | | ns |
| tAK | DACK↑ or ↓Delay from θ↓ (S2, S1) and TC/Mark↑ Delay from θ↑ (S3) and TC/Mark↓ Delay from θ↑ (S4) (Notes 1, 5) | | 250 | ns |
| tDCL | $\overline{RD}$↓ or $\overline{WR}$ (Ext)↓ Delay from θ↑ (S2) and $\overline{WR}$↓ Delay from θ↑ (S3) (Notes 2, 6) | | 200 | ns |
| tDCT | $\overline{RD}$↑ Delay from θ↓ (S1, SI) and $\overline{WR}$↑ Delay from θ↑ (S4) (Notes 2, 7) | | 200 | ns |
| tFAC | $\overline{RD}$ or $\overline{WR}$ (Active) from θ↑ (S1) (Note 2) | | 300 | ns |
| tAFC | $\overline{RD}$ or $\overline{WR}$ (Float) from θ↑ (SI) (Note 2) | | 150 | ns |
| tRWM | $\overline{RD}$ Width (S2, S1 or SI) (Note 4) | 2tCY+tθ−50 | | ns |
| tWWM | $\overline{WR}$ Width (S3, S4) (Note 4) | tCY−50 | | ns |
| tWWME | $\overline{WR}$ (Ext) Width (S2, S4) (Note 4) | 2tCY−50 | | ns |

Notes:
1. Load = 1 TTL.
2. Load = 1 TTL + 50pF.
3. Load = 1 TTL + (RL = 3.3K), VOH = 3.3V.
4. Tracking Parameter.
5. ΔtAK < 50ns.
6. ΔtDCL < 50ns.
7. ΔtDCT < 50ns.

## DMA MODE WAVEFORMS

### CONSECUTIVE CYCLES AND BURST MODE SEQUENCE




Note: The clock waveform is duplicated for clarity. The Am8257/9557 requires only one clock input.

**Figure 1. Consecutive Cycles and Burst Mode Sequence.** MOS-512

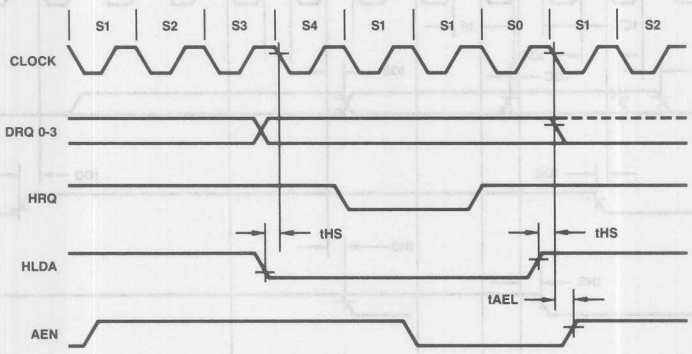



**Figure 2. Control Override Sequence.** MOS-513

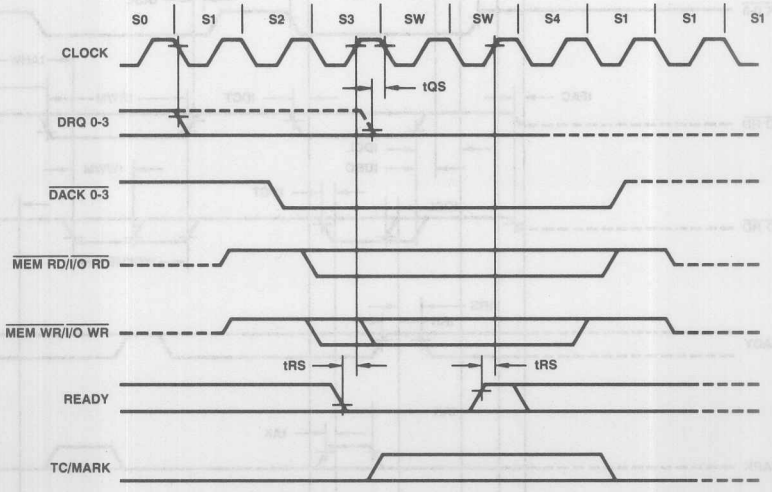
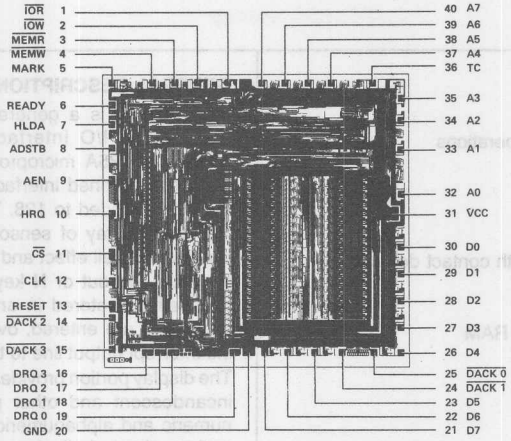



**Figure 3. Not Ready Sequence.** MOS-514

## Metallization and Pad Layout




DIE SIZE 0.196" x 0.210"

7

# Am8279/Am8279-5

## Programmable Keyboard/Display Interface

### DISTINCTIVE CHARACTERISTICS

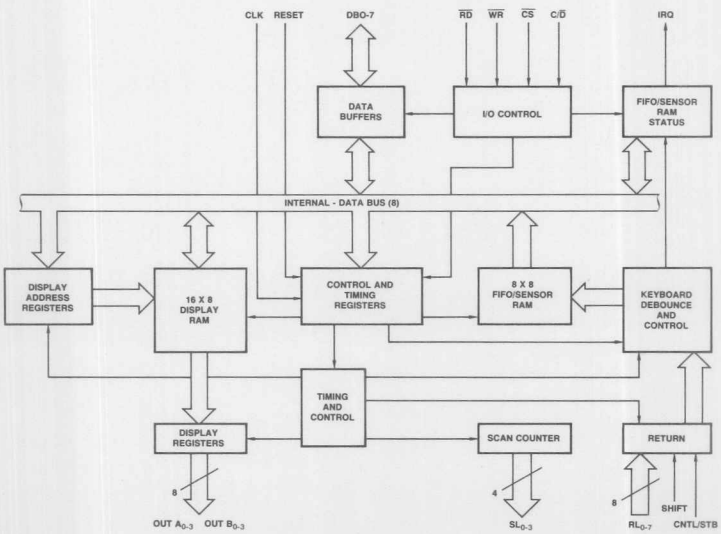
- Am8085A Compatible
- Simultaneous keyboard display operations
- Scanned keyboard mode
- Scanned sensor mode
- Strobed input entry mode
- 8 character keyboard FIFO
- 2 key lockout or N key rollover with contact debounce
- Dual 8 or 16 numerical display
- Single 16 character display
- Right or left entry 16-byte display RAM
- Mode programmable from CPU
- Programmable scan timing
- Interrupt output on key entry

### GENERAL DESCRIPTION

The Am8279 is a general purpose programmable keyboard and display I/O interface device designed for use with Am8080A/8085A microprocessors. The keyboard portion can provide a scanned interface to a 64 contact key matrix which can be expanded to 128. The keyboard portion will also interface to an array of sensors or a strobed interface keyboard, such as the Hall effect and Ferrite variety. Key depressions can be 2 key lockout or N key rollover. Keyboard entries are debounced and stored in an 8 character FIFO. If more than 8 characters are entered, over run status is set. Key entries set the interrupt output line to the CPU.

The display portion provides a scanned display interface for LED, incandescent and other popular display technologies. Both numeric and alphanumeric segment displays may be used as well as simple indicators. The Am8279 has a 16 x 8 display RAM which can be organized into a dual 16 x 4. The RAM can be loaded or interrogated by the CPU. Both right entry, calculator and left entry typewriter display formats are possible. Both read and write of the display RAM can be done with auto-increment of the display RAM address.

### BLOCK DIAGRAM



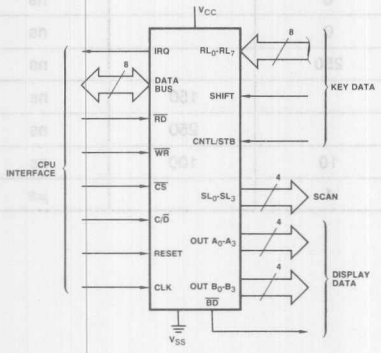

MOS-132

### ORDERING INFORMATION

| Package Type | Ambient Temperature Specification | Order Numbers | |
|---|---|---|---|
| Hermetic DIP* | $0°C \leq T_A \leq +70°C$ | AM8279DC<br>AM8279CC | AM8279-5DC<br>AM8279-5CC |
| Molded DIP | | AM8279PC | AM8279-5PC |

*Hermetic = Ceramic = DC = CC = D-40-1.

## LOGIC SYMBOL

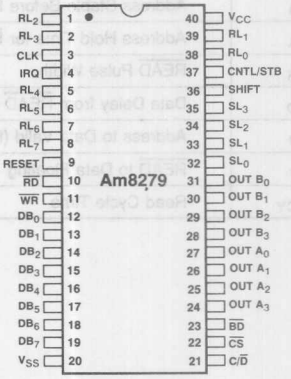



MOS-133

## PIN NAMES

| Name | I/O | Function |
|---|---|---|
| $DB_0$-$DB_7$ | I/O | Data Bus (Bidirectional) |
| CLK | I | Clock Input |
| RESET | I | Reset Input |
| $\overline{CS}$ | I | Chip Select |
| $\overline{RD}$ | I | Read Input |
| $\overline{WR}$ | I | Write Input |
| $C/\overline{D}$ | I | Buffer Address |
| IRQ | O | Interrupt Request Output |
| $SL_0$-$SL_3$ | O | Scan Lines |
| $RL_0$-$RL_7$ | I | Return Lines |
| SHIFT | I | Shift Input |
| CNTL/STB | I | Control/Strobe Input |
| $OUT\ A_0$-$A_3$ | O | Display (A) Outputs |
| $OUT\ B_0$-$B_3$ | O | Display (B) Outputs |
| $\overline{BD}$ | O | Blank Display Output |

## CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

MOS-134

## MAXIMUM RATINGS above which useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| $V_{CC}$ with Respect to $V_{SS}$ | −0.5V to +7.0V |
| All Signal Voltages with Respect to $V_{SS}$ | −0.5V to +7.0V |
| Power Dissipation | 1W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

7

## DC CHARACTERISTICS $T_A$ = 0°C to +70°C, $V_{SS}$ = 0V (Note 1)

| Parameter | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{IL1}$ | Input Low Voltage for Return lines Only | | −0.5 | | 1.4 | V |
| $V_{IL2}$ | Input Low Voltage for All Others | | −0.5 | | 0.8 | V |
| $V_{IH1}$ | Input High Voltage for Return lines Only | | 2.2 | | | V |
| $V_{IH2}$ | Input High Voltage for All Others | | 2.0 | | | V |
| $V_{OL}$ | Output Low Voltage | Note 2 | | | .45 | V |
| $V_{OH}$ | Output High Voltage on Interrupt Line | Note 3 | 3.5 | | | V |
| $I_{IL1}$ | Input Current on Shift, Control and Returns | $V_{IN} = V_{CC}$<br>$V_{IN}$ = 0V | | | +10<br>−100 | μA<br>μA |
| $I_{IL2}$ | Input Leakage Current on All Others | $V_{IN} = V_{CC}$ to 0V | | | ±10 | μA |
| $I_{OFL}$ | Output Float Leakage | $V_{OUT} = V_{CC}$ to 0V | | | ±10 | μA |
| $I_{CC}$ | Power Supply Current | | | | 120 | mA |

Notes: 1. Am8279, $V_{CC}$ = +5.0V ±5%; Am8279-5, $V_{CC}$ = +5.0V ±10%.
2. Am8279, $I_{OL}$ = 1.6mA; Am8279-5, $I_{OL}$ = 2.2mA.
3. Am8279, $I_{OH}$ = −100μA; Am8279-5, $I_{OH}$ = −400μA.

## CAPACITANCE

| Parameter | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN} = V_{CC}$ | | 5 | 10 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT} = V_{CC}$ | | 10 | 20 | pF |

| Parameter | Description | Am8279 Min. | Am8279 Max. | Am8279-5 Min. | Am8279-5 Max. | Units |
|---|---|---|---|---|---|---|
| $t_{AR}$ | Address Stable Before $\overline{READ}$ | 50 | | 0 | | ns |
| $t_{RA}$ | Address Hold Time for $\overline{READ}$ | 5 | | 0 | | ns |
| $t_{RR}$ | $\overline{READ}$ Pulse Width | 420 | | 250 | | ns |
| $t_{RD}$ | Data Delay from $\overline{READ}$ (Note 2) | | 300 | | 150 | ns |
| $t_{AD}$ | Address to Data Valid (Note 2) | | 450 | | 250 | ns |
| $t_{DF}$ | $\overline{READ}$ to Data Floating | 10 | 100 | 10 | 100 | ns |
| $t_{RCY}$ | Read Cycle Time | 1 | | 1 | | $\mu$s |

**Write Cycle:**

| Parameter | Description | Am8279 Min. | Am8279 Max. | Am8279-5 Min. | Am8279-5 Max. | Units |
|---|---|---|---|---|---|---|
| $t_{AW}$ | Address Stable Before $\overline{WRITE}$ | 50 | | 0 | | ns |
| $t_{WA}$ | Address Hold Time for $\overline{WRITE}$ | 20 | | 0 | | ns |
| $t_{WW}$ | $\overline{WRITE}$ Pulse Width | 400 | | 250 | | ns |
| $t_{DW}$ | Data Set-up Time for $\overline{WRITE}$ | 300 | | 150 | | ns |
| $t_{WD}$ | Data Hold Time for $\overline{WRITE}$ | 40 | | 0 | | ns |

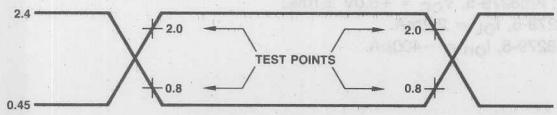
Notes: 1. Am8279, $V_{CC}$ = +5.0V ±5%; Am8279-5, $V_{CC}$ = +5.0V ±10%.
2. Am8279, $C_L$ = 100pF; Am8279-5, $C_L$ = 150pF.

**Other Timings:**

| Parameter | Description | Am8279 Min. | Am8279 Max. | Am8279-5 Min. | Am8279-5 Max. | Units |
|---|---|---|---|---|---|---|
| $t_{\phi W}$ | Clock Pulse Width | 230 | | 120 | | ns |
| $t_{CY}$ | Clock Period | 500 | | 320 | | ns |

| | | | |
|---|---|---|---|
| Keyboard Scan Time | 5.1msec | Digit-on Time | 480$\mu$sec |
| Keyboard Debounce Time | 10.3msec | Blanking Time | 160$\mu$sec |
| Key Scan Time | 80$\mu$sec | Internal Clock Cycle | 10$\mu$sec |
| Display Scan Time | 10.3msec | | |

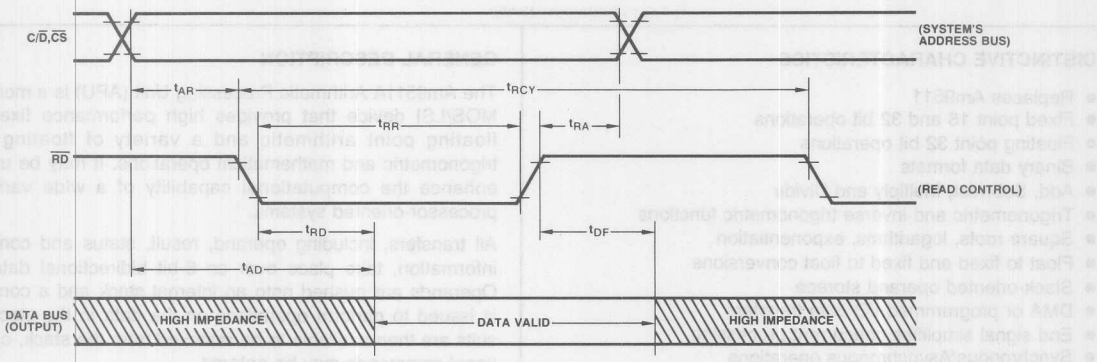
**INPUT WAVEFORMS FOR AC TESTS**




MOS-135

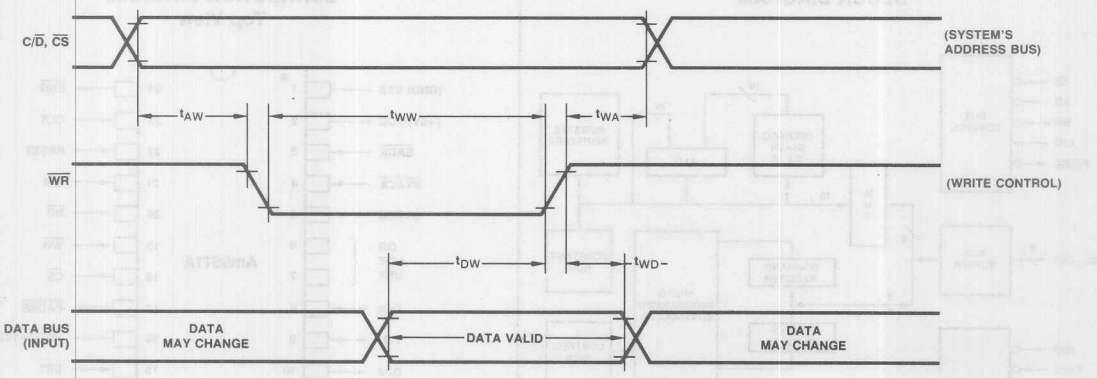
## WAVEFORMS

### READ OPERATION



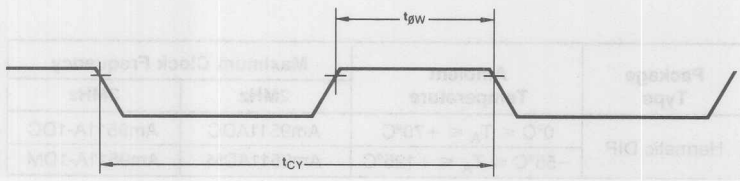

MOS-136

### WRITE OPERATION




MOS-137

### CLOCK INPUT




MOS-138

7

# Am9511A
## Arithmetic Processor

### DISTINCTIVE CHARACTERISTICS

- Replaces Am9511
- Fixed point 16 and 32 bit operations
- Floating point 32 bit operations
- Binary data formats
- Add, Subtract, Multiply and Divide
- Trigonometric and inverse trigonometric functions
- Square roots, logarithms, exponentiation
- Float to fixed and fixed to float conversions
- Stack-oriented operand storage
- DMA or programmed I/O data transfers
- End signal simplifies concurrent processing
- Synchronous/Asynchronous operations
- General purpose 8-bit data bus interface
- Standard 24 pin package
- +12 volt and +5 volt power supplies
- Advanced N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

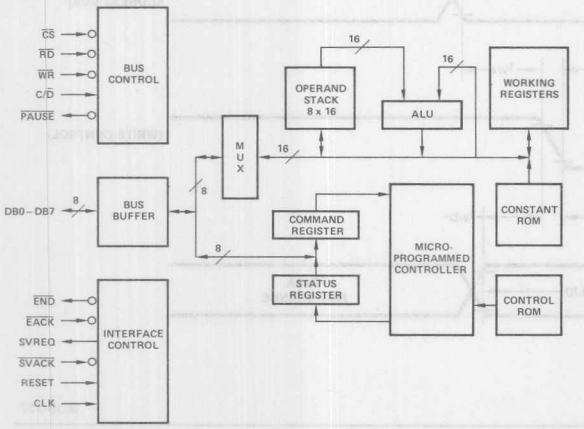
### GENERAL DESCRIPTION

The Am9511A Arithmetic Processing Unit (APU) is a monolithic MOS/LSI device that provides high performance fixed and floating point arithmetic and a variety of floating point trigonometric and mathematical operations. It may be used to enhance the computational capability of a wide variety of processor-oriented systems.

All transfers, including operand, result, status and command information, take place over an 8-bit bidirectional data bus. Operands are pushed onto an internal stack and a command is issued to perform operations on the data in the stack. Results are then available to be retrieved from the stack, or additional commands may be entered.

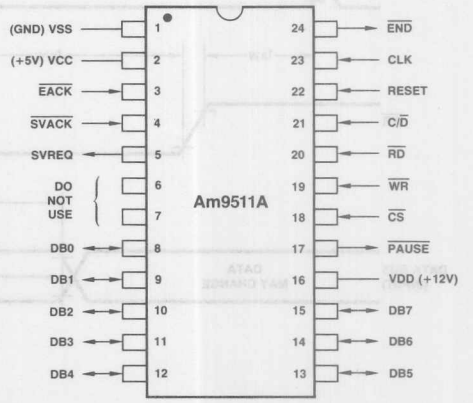
Transfers to and from the APU may be handled by the associated processor using conventional programmed I/O, or may be handled by a direct memory access controller for improved performance. Upon completion of each command, the APU issues an end of execution signal that may be used as an interrupt by the CPU to help coordinate program execution.

### BLOCK DIAGRAM




MOS-046

### CONNECTION DIAGRAM
**Top View**




Pin 1 is marked for orientation.

MOS-047

### ORDERING INFORMATION

| Package Type | Ambient Temperature | Maximum Clock Frequency | |
|---|---|---|---|
| | | 2MHz | 3MHz |
| Hermetic DIP | $0°C \leq T_A \leq +70°C$ | Am9511ADC | Am9511A-1DC |
| | $-55°C \leq T_A \leq +125°C$ | Am9511ADM | Am9511A-1DM |

## INTERFACE SIGNAL DESCRIPTION

**VCC:** +5V Power Supply
**VDD:** +12V Power Supply
**VSS:** Ground

### CLK (Clock, Input)

An external timing source connected to the CLK input provides the necessary clocking. The CLK input can be asynchronous to the $\overline{RD}$ and $\overline{WR}$ control signals.

### RESET (Reset, Input)

A HIGH on this input causes initialization. Reset terminates any operation in progress, and clears the status register to zero. The internal stack pointer is initialized and the contents of the stack may be affected but the command register is not affected by the reset operation. After a reset the $\overline{END}$ output will be HIGH, and the SVREQ output will be LOW. For proper initialization, the RESET input must be HIGH for at least five CLK periods following stable power supply voltages and stable clock.

### C/$\overline{D}$ (Command/Data Select, Input)

The C/$\overline{D}$ input together with the $\overline{RD}$ and $\overline{WR}$ inputs determines the type of transfer to be performed on the data bus as follows:

| C/$\overline{D}$ | $\overline{RD}$ | $\overline{WR}$ | Function |
|---|---|---|---|
| L | H | L | Push data byte into the stack |
| L | L | H | Pop data byte from the stack |
| H | H | L | Enter command byte from the data bus |
| H | L | H | Read Status |
| X | L | L | Undefined |

L = LOW
H = HIGH
X = DON'T CARE

### $\overline{END}$ (End of Execution, Output)

A LOW on this output indicates that execution of the current command is complete. This output will be cleared HIGH by activating the $\overline{EACK}$ input LOW or performing any read or write operation or device initialization using the RESET. If $\overline{EACK}$ is tied LOW, the $\overline{END}$ output will be a pulse (see $\overline{EACK}$ description). This is an open drain output and requires a pull up to +5V.

Reading the status register while a command execution is in progress is allowed. However any read or write operation clears the flip-flop that generates the $\overline{END}$ output. Thus such continuous reading could conflict with internal logic setting the $\overline{END}$ flip-flop at the completion of command execution.

### $\overline{EACK}$ (End Acknowledge, Output)

This input when LOW makes the $\overline{END}$ output go LOW. As mentioned earlier HIGH on the $\overline{END}$ output signals completion of a command execution. The $\overline{END}$ output signal is derived from an internal flip-flop which is clocked at the completion of a command. This flip-flop is clocked to the reset state when $\overline{EACK}$ is LOW. Consequently, if the $\overline{EACK}$ is tied LOW, the $\overline{END}$ output will be a pulse that is approximately one CLK period wide.

### SVREQ (Service Request, Output)

A HIGH on this output indicates completion of a command. In this sense this output is same as the $\overline{END}$ output. However, whether the SVREQ output will go HIGH at the completion of a command or not is determined by a service request bit in the command register. This bit must be 1 for SVREQ to go HIGH. The SVREQ can be cleared (i.e., go LOW) by activating the $\overline{SVACK}$ input LOW or initializing the device using the RESET. Also, the SVREQ will be automatically cleared after completion of any command that has the service request bit as 0.

### $\overline{SVACK}$ (Service Acknowledge, Input)

A LOW on this input activates the reset input of the flip-flop generating the SVREQ output. If the $\overline{SVACK}$ input is permanently tied LOW, it will conflict with the internal setting of the flip-flop to generate the SVREQ output. Thus the SVREQ indication cannot be relied upon if the $\overline{SVACK}$ is tied LOW.

### DB0-DB7 (Bidirectional Data Bus, Input/Output)

These eight bidirectional lines are used to transfer command, status and operand information between the device and the host processor. DB0 is the least significant and DB7 is the most significant bit position. HIGH on the data bus line corresponds to 1 and LOW corresponds to 0.

When pushing operands on the stack using the data bus, the least significant byte must be pushed first and most significant byte last. When popping the stack to read the result of an operation, the most significant byte will be available on the data bus first and the least significant byte will be the last. Moreover, for pushing operands and popping results, the number of transactions must be equal to the proper number of bytes appropriate for the chosen format. Otherwise, the internal byte pointer will not be aligned properly. The Am9511A single precision format requires 2 bytes, double precision and floating-point formats require 4 bytes.

### $\overline{CS}$ (Chip Select, Input)

This input must be LOW to accomplish any read or write operation to the Am9511A.

To perform a write operation data is presented on DB0 through DB7 lines, C/$\overline{D}$ is driven to an appropriate level and the $\overline{CS}$ input is made LOW. However, actual writing into the Am9511A cannot start until $\overline{WR}$ is made LOW. After initiating the write operation by a $\overline{WR}$ HIGH to LOW transition, the $\overline{PAUSE}$ output will go LOW momentarily (TPPWW).

The $\overline{WR}$ input can go HIGH after $\overline{PAUSE}$ goes HIGH. The data lines, C/$\overline{D}$ input and the $\overline{CS}$ input can change when appropriate hold time requirements are satisfied. See write timing diagram for details.

To perform a read operation an appropriate logic level is established on the C/$\overline{D}$ input and $\overline{CS}$ is made LOW. The Read operation does not start until the $\overline{RD}$ input goes LOW. $\overline{PAUSE}$ will go LOW for a period of TPPWR. When $\overline{PAUSE}$ goes back HIGH again, it indicates that read operation is complete and the required information is available on the DB0 through DB7 lines. This information will remain on the data lines as long as $\overline{RD}$ input is LOW. The $\overline{RD}$ input can return HIGH anytime after $\overline{PAUSE}$ goes HIGH. The $\overline{CS}$ input and C/$\overline{D}$ inputs can change anytime after $\overline{RD}$ returns HIGH. See read timing diagram for details.

### $\overline{RD}$ (Read, Input)

A LOW on this input is used to read information from an internal location and gate that information on to the data bus. The $\overline{CS}$ input must be LOW to accomplish the read operation. The C/$\overline{D}$ input determines what internal location is of interest. See C/$\overline{D}$, $\overline{CS}$ input descriptions and read timing diagram for details. If the END output was LOW, performing any read operation will make the $\overline{END}$ output go HIGH after the HIGH to LOW transition of the $\overline{RD}$ input (assuming $\overline{CS}$ is LOW).

7

**$\overline{WR}$ (Write, Input)**

A LOW on this input is used to transfer information from the data bus into an internal location. The $\overline{CS}$ must be LOW to accomplish the write operation. The C/$\overline{D}$ determines which internal location is to be written. See C/$\overline{D}$, $\overline{CS}$ input descriptions and write timing diagram for details.

If the $\overline{END}$ output was LOW, performing any write operation will make the $\overline{END}$ output go HIGH after the LOW to HIGH transition of the $\overline{WR}$ input (assuming $\overline{CS}$ is LOW).

**$\overline{PAUSE}$ (Pause, Output)**

This output is a handshake signal used while performing read or write transactions with the Am9511A. A LOW at this output indicates that the Am9511A has not yet completed its information transfer with the host over the data bus. During a read operation, after $\overline{CS}$ went LOW, the $\overline{PAUSE}$ will become LOW shortly (TRP) after $\overline{RD}$ goes LOW. $\overline{PAUSE}$ will return high only after the data bus contains valid output data. The $\overline{CS}$ and $\overline{RD}$ should remain LOW when $\overline{PAUSE}$ is LOW. The RD may go high anytime after $\overline{PAUSE}$ goes HIGH. During a write operation, after $\overline{CS}$ went LOW, the $\overline{PAUSE}$ will be LOW for a very short duration (TPPWN) after $\overline{WR}$ goes LOW. Since the minimum of TPPWW is 0, the $\overline{PAUSE}$ may not go LOW at all for fast devices. $\overline{WR}$ may go HIGH anytime after $\overline{PAUSE}$ goes HIGH.

## FUNCTIONAL DESCRIPTION

Major functional units of the Am9511A are shown in the block diagram. The Am9511A employs a microprogram controlled stack oriented architecture with 16-bit wide data paths.

The Arithmetic Logic Unit (ALU) receives one of its operands from the Operand Stack. This stack is an 8-word by 16-bit 2-port memory with last in-first out (LIFO) attributes. The second operand to the ALU is supplied by the internal 16-bit bus. In addition to supplying the second operand, this bidirectional bus also carries the results from the output of the ALU when required. Writing into the Operand Stack takes place from this internal 16-bit bus when required. Also connected to this bus are the Constant ROM and Working Registers. The ROM provides the required constants to perform the mathematical operations (Chebyshev Algorithms) while the Working Registers provide storage for the intermediate values during command execution.

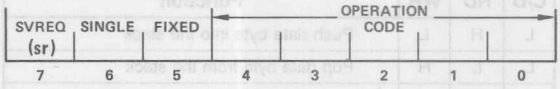
Communication between the external world and the Am9511A takes place on eight bidirectional input/output lines DB0 through DB7 (Data Bus). These signals are gated to the internal eight-bit bus through appropriate interface and buffer circuitry. Multiplexing facilities exist for bidirectional communication between the internal eight and sixteen-bit buses. The Status Register and Command Register are also accessible via the eight-bit bus.

The Am9511A operations are controlled by the microprogram contained in the Control ROM. The Program Counter supplies the microprogram addresses and can be partially loaded from the Command Register. Associated with the Program Counter is the Subroutine Stack where return addresses are held during subroutine calls in the microprogram. The Microinstruction Register holds the current microinstruction being executed. This register facilitates pipelined microprogram execution. The Instruction Decode logic generates various internal control signals needed for the Am9511A operation.

The Interface Control logic receives several external inputs and provides handshake related outputs to facilitate interfacing the Am9511A to microprocessors.

## COMMAND FORMAT

Each command entered into the Am9511A consists of a single 8-bit byte having the format illustrated below:




Bits 0-4 select the operation to be performed as shown in the table. Bits 5-6 select the data format for the operation. If bit 5 is a 1, a fixed point data format is specified. If bit 5 is a 0, floating point format is specified. Bit 6 selects the precision of the data to be operated on by fixed point commands (if bit 5 = 0, bit 6 must be 0). If bit 6 is a 1, single-precision (16-bit) operands are indicated; if bit 6 is a 0, double-precision (32-bit) operands are indicated. Results are undefined for all illegal combinations of bits in the command byte. Bit 7 indicates whether a service request is to be issued after the command is executed. If bit 7 is a 1, the service request output (SVREQ) will go high at the conclusion of the command and will remain high until reset by a low level on the service acknowledge pin ($\overline{SVACK}$) or until completion of execution of a succeeding command where bit 7 is 0. Each command issued to the Am9511A requests post execution service based upon the state of bit 7 in the command byte. When bit 7 is a 0, SVREQ remains low.

## COMMAND SUMMARY

| Command Code | | | | | | | | Command Mnemonic | Command Description |
|---|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| **FIXED-POINT 16-BIT** | | | | | | | | | |
| sr | 1 | 1 | 0 | 1 | 1 | 0 | 0 | SADD | Add TOS to NOS. Result to NOS. Pop Stack. |
| sr | 1 | 1 | 0 | 1 | 1 | 0 | 1 | SSUB | Subtract TOS from NOS. Result to NOS. Pop Stack. |
| sr | 1 | 1 | 0 | 1 | 1 | 1 | 0 | SMUL | Multiply NOS by TOS. Lower half of result to NOS. Pop Stack. |
| sr | 1 | 1 | 1 | 0 | 1 | 1 | 0 | SMUU | Multiply NOS by TOS. Upper half of result to NOS. Pop Stack. |
| sr | 1 | 1 | 0 | 1 | 1 | 1 | 1 | SDIV | Divide NOS by TOS. Result to NOS. Pop Stack. |
| **FIXED-POINT 32-BIT** | | | | | | | | | |
| sr | 0 | 1 | 0 | 1 | 1 | 0 | 0 | DADD | Add TOS to NOS. Result to NOS. Pop Stack. |
| sr | 0 | 1 | 0 | 1 | 1 | 0 | 1 | DSUB | Subtract TOS from NOS. Result to NOS. Pop Stack. |
| sr | 0 | 1 | 0 | 1 | 1 | 1 | 0 | DMUL | Multiply NOS by TOS. Lower half of result to NOS. Pop Stack. |
| sr | 0 | 1 | 1 | 0 | 1 | 1 | 0 | DMUU | Multiply NOS by TOS. Upper half of result to NOS. Pop Stack. |
| sr | 0 | 1 | 0 | 1 | 1 | 1 | 1 | DDIV | Divide NOS by TOS. Result to NOS. Pop Stack. |
| **FLOATING-POINT 32-BIT** | | | | | | | | | |
| sr | 0 | 0 | 1 | 0 | 0 | 0 | 0 | FADD | Add TOS to NOS. Result to NOS. Pop Stack. |
| sr | 0 | 0 | 1 | 0 | 0 | 0 | 1 | FSUB | Subtract TOS from NOS. Result to NOS. Pop Stack. |
| sr | 0 | 0 | 1 | 0 | 0 | 1 | 0 | FMUL | Multiply NOS by TOS. Result to NOS. Pop Stack. |
| sr | 0 | 0 | 1 | 0 | 0 | 1 | 1 | FDIV | Divide NOS by TOS. Result to NOS. Pop Stack. |
| **DERIVED FLOATING-POINT FUNCTIONS** | | | | | | | | | |
| sr | 0 | 0 | 0 | 0 | 0 | 0 | 1 | SQRT | Square Root of TOS. Result in TOS. |
| sr | 0 | 0 | 0 | 0 | 0 | 1 | 0 | SIN | Sine of TOS. Result in TOS. |
| sr | 0 | 0 | 0 | 0 | 0 | 1 | 1 | COS | Cosine of TOS. Result in TOS. |
| sr | 0 | 0 | 0 | 0 | 1 | 0 | 0 | TAN | Tangent of TOS. Result in TOS. |
| sr | 0 | 0 | 0 | 0 | 1 | 0 | 1 | ASIN | Inverse Sine of TOS. Result in TOS. |
| sr | 0 | 0 | 0 | 0 | 1 | 1 | 0 | ACOS | Inverse Cosine of TOS. Result in TOS. |
| sr | 0 | 0 | 0 | 0 | 1 | 1 | 1 | ATAN | Inverse Tangent of TOS. Result in TOS. |
| sr | 0 | 0 | 0 | 1 | 0 | 0 | 0 | LOG | Common Logarithm (base 10) of TOS. Result in TOS. |
| sr | 0 | 0 | 0 | 1 | 0 | 0 | 1 | LN | Natural Logarithm (base e) of TOS. Result in TOS. |
| sr | 0 | 0 | 0 | 1 | 0 | 1 | 0 | EXP | Exponential ($e^X$) of TOS. Result in TOS. |
| sr | 0 | 0 | 0 | 1 | 0 | 1 | 1 | PWR | NOS raised to the power in TOS. Result in NOS. Pop Stack. |
| **DATA MANIPULATION COMMANDS** | | | | | | | | | |
| sr | 0 | 0 | 0 | 0 | 0 | 0 | 0 | NOP | No Operation |
| sr | 0 | 0 | 1 | 1 | 1 | 1 | 1 | FIXS | Convert TOS from floating point to 16-bit fixed point format. |
| sr | 0 | 0 | 1 | 1 | 1 | 1 | 0 | FIXD | Convert TOS from floating point to 32-bit fixed point format. |
| sr | 0 | 0 | 1 | 1 | 1 | 0 | 1 | FLTS | Convert TOS from 16-bit fixed point to floating point format. |
| sr | 0 | 0 | 1 | 1 | 1 | 0 | 0 | FLTD | Convert TOS from 32-bit fixed point to floating point format. |
| sr | 1 | 1 | 1 | 0 | 1 | 0 | 0 | CHSS | Change sign of 16-bit fixed point operand on TOS. |
| sr | 0 | 1 | 1 | 0 | 1 | 0 | 0 | CHSD | Change sign of 32-bit fixed point operand on TOS. |
| sr | 0 | 0 | 1 | 0 | 1 | 0 | 1 | CHSF | Change sign of floating point operand on TOS. |
| sr | 1 | 1 | 1 | 0 | 1 | 1 | 1 | PTOS | Push 16-bit fixed point operand on TOS to NOS (Copy) |
| sr | 0 | 1 | 1 | 0 | 1 | 1 | 1 | PTOD | Push 32-bit fixed point operand on TOS to NOS. (Copy) |
| sr | 0 | 0 | 1 | 0 | 1 | 1 | 1 | PTOF | Push floating point operand on TOS to NOS. (Copy) |
| sr | 1 | 1 | 1 | 1 | 0 | 0 | 0 | POPS | Pop 16-bit fixed point operand from TOS. NOS becomes TOS. |
| sr | 0 | 1 | 1 | 1 | 0 | 0 | 0 | POPD | Pop 32-bit fixed point operand from TOS. NOS becomes TOS. |
| sr | 0 | 0 | 1 | 1 | 0 | 0 | 0 | POPF | Pop floating point operand from TOS. NOS becomes TOS. |
| sr | 1 | 1 | 1 | 1 | 0 | 0 | 1 | XCHS | Exchange 16-bit fixed point operands TOS and NOS. |
| sr | 0 | 1 | 1 | 1 | 0 | 0 | 1 | XCHD | Exchange 32-bit fixed point operands TOS and NOS. |
| sr | 0 | 0 | 1 | 1 | 0 | 0 | 1 | XCHF | Exchange floating point operands TOS and NOS. |
| sr | 0 | 0 | 1 | 1 | 0 | 1 | 0 | PUPI | Push floating point constant "$\pi$" onto TOS. Previous TOS becomes NOS. |

NOTES:

1. TOS means Top of Stack. NOS means Next on Stack.
2. AMD Application Brief "Algorithm Details for the Am9511A APU" provides detailed descriptions of each command function, including data ranges, accuracies, stack configurations, etc.
3. Many commands destroy one stack location (bottom of stack) during development of the result. The derived functions may destroy several stack locations. See Application Brief for details.
4. The trigonometric functions handle angles in radians, not degrees.
5. No remainder is available for the fixed-point divide functions.
6. Results will be undefined for any combination of command coding bits not specified in this table.

7

### COMMAND INITIATION

After properly positioning the required operands on the stack, a command may be issued. The procedure for initiating a command execution is as follows:

1. Enter the appropriate command on the DB0-DB7 lines.
2. Establish HIGH on the C/$\overline{D}$ input.
3. Establish LOW on the $\overline{CS}$ input.
4. Establish LOW on the $\overline{WR}$ input after an appropriate set up time (see timing diagrams).
5. Sometime after the HIGH to LOW level transition of $\overline{WR}$ input, the $\overline{PAUSE}$ output will become LOW. After a delay of TPPWW, it will go HIGH to acknowledge the write operation. The WR input can return to HIGH anytime after $\overline{PAUSE}$ going HIGH. The DB0-DB7, C/$\overline{D}$ and $\overline{CS}$ inputs are allowed to change after the hold time requirements are satisfied (see timing diagram).

An attempt to issue a new command while the current command execution is in progress is allowed. Under these circumstances, the $\overline{PAUSE}$ output will not go HIGH until the current command execution is completed.

### OPERAND ENTRY

The Am9511A commands operate on the operands located at the TOS and NOS and results are returned to the stack at NOS and then popped to TOS. The operands required for the Am9511A are one of three formats – single precision fixed-point (2 bytes), double precision fixed-point (4 bytes) or floating-point (4 bytes). The result of an operation has the same format as the operands except for float to fix or fix to float commands.

Operands are always entered into the stack least significant byte first and most significant byte last. The following procedure must be followed to enter operands onto the stack:

1. The lower significant operand byte is established on the DB0-DB7 lines.
2. A LOW is established on the C/$\overline{D}$ input to specify that data is to be entered into the stack.
3. The $\overline{CS}$ input is made LOW.
4. After appropriate set up time (see timing diagrams), the $\overline{WR}$ input is made LOW. The $\overline{PAUSE}$ output will become LOW.
5. Sometime after this event, the $\overline{PAUSE}$ will return HIGH to indicate that the write operation has been acknowledged.
6. Anytime after the $\overline{PAUSE}$ output goes HIGH the $\overline{WR}$ input can be made HIGH. The DB0-DB7, C/$\overline{D}$ and $\overline{CS}$ inputs can change after appropriate hold time requirements are satisfied (see timing diagrams).

The above procedure must be repeated until all bytes of the operand are pushed into the stack. It should be noted that for single precision fixed-point operands 2 bytes should be pushed and 4 bytes must be pushed for double precision fixed-point or floating-point. Not pushing all the bytes of a quantity will result in byte pointer misalignment.

The Am9511A stack can accommodate 8 single precision fixed-point quantities or 4 double precision fixed-point or floating-point quantities. Pushing more quantities than the capacity of the stack will result in loss of data which is usual with any LIFO stack.

### DATA REMOVAL

Result from an operation will be available at the TOS. Results can be transferred from the stack to the data bus by reading the stack. When the stack is popped for results, the most significant byte is available first and the least significant byte last. A result is always of the same precision as the operands that produced it except for format conversion commands. Thus when the result is taken from the stack, the total number of bytes popped out should be appropriate with the precision – single precision results are 2 bytes and double precision and floating-point results are 4 bytes. The following procedure must be used for reading the result from the stack:

1. A LOW is established on the C/$\overline{D}$ input.
2. The $\overline{CS}$ input is made LOW.
3. After appropriate set up time (see timing diagrams), the $\overline{RD}$ input is made LOW. The $\overline{PAUSE}$ will become LOW.
4. Sometime after this, $\overline{PAUSE}$ will return HIGH indicating that the data is available on the DB0-DB7 lines. This data will remain on the DB0-DB7 lines as long as the $\overline{RD}$ input remains LOW.
5. Anytime after $\overline{PAUSE}$ goes HIGH, the $\overline{RD}$ input can return HIGH to complete transaction.
6. The $\overline{CS}$ and C/$\overline{D}$ inputs can change after appropriate hold time requirements are satisfied (see timing diagram).
7. Repeat this procedure until all bytes appropriate for the precision of the result are popped out.

Reading of the stack does not alter its data; it only adjusts the byte pointer. If more data is popped than the capacity of the stack, the internal byte pointer will wrap around and older data will be read again, consistent with the LIFO stack.

### STATUS READ

The Am9511A status register can be read without any regard to whether a command is in progress or not. The only implication that has to be considered is the effect this might have on the END output discussed in the signal descriptions.

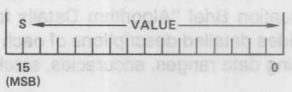
The following procedure must be followed to accomplish status register reading.

1. Establish HIGH on the C/$\overline{D}$ input.
2. Establish LOW on the $\overline{CS}$ input.
3. After appropriate set up time (see timing diagram) $\overline{RD}$ input is made LOW. The $\overline{PAUSE}$ will become LOW.
4. Sometime after the HIGH to LOW transition of $\overline{RD}$ input, the $\overline{PAUSE}$ will become HIGH indicating that status register contents are available on the DB0-DB7 lines. The status data will remain on DB0-DB7 as long as $\overline{RD}$ input is LOW.
5. The $\overline{RD}$ input can be returned HIGH anytime after $\overline{PAUSE}$ goes HIGH.
6. The C/$\overline{D}$ input and $\overline{CS}$ input can change after satisfying appropriate hold time requirements (see timing diagram).

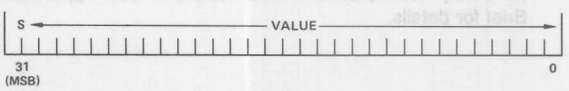
### DATA FORMATS

The Am9511A Arithmetic Processing Unit handles operands in both fixed-point and floating-point formats. Fixed-point operands may be represented in either single (16-bit operands) or double precision (32-bit operands), and are always represented as binary, two's complement values.

**16-BIT FIXED-POINT FORMAT**




**32-BIT FIXED-POINT FORMAT**



The sign (positive or negative) of the operand is located in the most significant bit (MSB). Positive values are represented by a sign bit of zero (S = 0). Negative values are represented by the two's complement of the corresponding positive value with a sign bit equal to 1 (S = 1). The range of values that may be accommodated by each of these formats is −32,768 to +32,767 for single precision and −2,147,483,648 to +2,147,483,647 for double precision.

Floating point binary values are represented in a format that permits arithmetic to be performed in a fashion analogous to operations with decimal values expressed in scientific notation.

$$(5.83 \times 10^2)(8.16 \times 10^1) = (4.75728 \times 10^4)$$

In the decimal system, data may be expressed as values between 0 and 10 times 10 raised to a power that effectively shifts the implied decimal point right or left the number of places necessary to express the result in conventional form (e.g., 47,572.8). The value-portion of the data is called the mantissa. The exponent may be either negative or positive.

The concept of floating point notation has both a gain and a loss associated with it. The gain is the ability to represent the significant digits of data with values spanning a large dynamic range limited only by the capacity of the exponent field. For example, in decimal notation if the exponent field is two digits wide, and the mantissa is five digits, a range of values (positive or negative) from $1.0000 \times 10^{-99}$ to $9.9999 \times 10^{+99}$ can be accommodated. The loss is that only the significant digits of the value can be represented. Thus there is no distinction in this representation between the values 123451 and 123452, for example, since each would be expressed as: $1.2345 \times 10^5$. The sixth digit has been discarded. In most applications where the dynamic range of values to be represented is large, the loss of significance, and hence accuracy of results, is a minor consideration. For greater precision a fixed point format could be chosen, although with a loss of potential dynamic range.

The Am9511 is a binary arithmetic processor and requires that floating point data be represented by a fractional mantissa value between .5 and 1 multiplied by 2 raised to an appropriate power. This is expressed as follows:

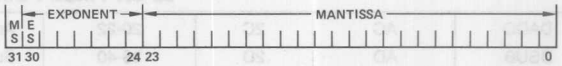
$$\text{value} = \text{mantissa} \times 2^{\text{exponent}}$$

For example, the value 100.5 expressed in this form is $0.11001001 \times 2^7$. The decimal equivalent of this value may be computed by summing the components (powers of two) of the mantissa and then multiplying by the exponent as shown below:

$$\begin{aligned}\text{value} &= (2^{-1} + 2^{-2} + 2^{-5} + 2^{-8}) \times 2^7 \\ &= (0.5 + 0.25 + 0.03125 + 0.00290625) \times 128 \\ &= 0.78515625 \times 128 \\ &= 100.5\end{aligned}$$

## FLOATING POINT FORMAT

The format for floating-point values in the Am9511A is given below. The mantissa is expressed as a 24-bit (fractional) value; the exponent is expressed as an unbiased two's complement 7-bit value having a range of −64 to +63. The most significant bit is the sign of the mantissa (0 = positive, 1 = negative), for a total of 32 bits. The binary point is assumed to be to the left of the most significant mantissa bit (bit 23). All floating-point data values must be normalized. Bit 23 must be equal to 1, except for the value zero, which is represented by all zeros.




The range of values that can be represented in this format is $\pm(2.7 \times 10^{-20}$ to $9.2 \times 10^{18})$ and zero.

## STATUS REGISTER

The Am9511A contains an eight bit status register with the following bit assignments:

| BUSY | SIGN | ZERO | ERROR CODE | | | | CARRY |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

BUSY: Indicates that Am9511A is currently executing a command (1 = Busy).

SIGN: Indicates that the value on the top of stack is negative (1 = Negative).

ZERO: Indicates that the value on the top of stack is zero (1 = Value is zero).

ERROR CODE: This field contains an indication of the validity of the result of the last operation. The error codes are:

- 0000 – No error
- 1000 – Divide by zero
- 0100 – Square root or log of negative number
- 1100 – Argument of inverse sine, cosine, or $e^x$ too large
- XX10 – Underflow
- XX01 – Overflow

CARRY: Previous operation resulted in carry or borrow from most significant bit. (1 = Carry/Borrow, 0 = No Carry/No Borrow)

If the BUSY bit in the status register is a one, the other status bits are not defined; if zero, indicating not busy, the operation is complete and the other status bits are defined as given above.

7

| | | | | |
|---|---|---|---|---|
| **16-BIT FIXED-POINT OPERATIONS** | | | | |
| SADD | EC | 6C | 16-18 | Add TOS to NOS. Result to NOS. Pop Stack. |
| SSUB | ED | 6D | 30-32 | Subtract TOS from NOS. Result to NOS. Pop Stack. |
| SMUL | EE | 6E | 84-94 | Multiply NOS by TOS. Lower result to NOS. Pop Stack. |
| SMUU | F6 | 76 | 80-98 | Multiply NOS by TOS. Upper result to NOS. Pop Stack. |
| SDIV | EF | 6F | 84-94 | Divide NOS by TOS. Result to NOS. Pop Stack. |
| **32-BIT FIXED-POINT OPERATIONS** | | | | |
| DADD | AC | 2C | 20-22 | Add TOS to NOS. Result to NOS. Pop Stack. |
| DSUB | AD | 2D | 38-40 | Subtract TOS from NOS. Result to NOS. Pop Stack. |
| DMUL | AE | 2E | 194-210 | Multiply NOS by TOS. Lower result to NOS. Pop Stack. |
| DMUU | B6 | 36 | 182-218 | Multiply NOS by TOS. Upper result to NOS. Pop Stack. |
| DDIV | AF | 2F | 196-210 | Divide NOS by TOS. Result to NOS. Pop Stack. |
| **32-BIT FLOATING-POINT PRIMARY OPERATIONS** | | | | |
| FADD | 90 | 10 | 54-368 | Add TOS to NOS. Result to NOS. Pop Stack. |
| FSUB | 91 | 11 | 70-370 | Subtract TOS from NOS. Result to NOS. Pop Stack. |
| FMUL | 92 | 12 | 146-168 | Multiply NOS by TOS. Result to NOS. Pop Stack. |
| FDIV | 93 | 13 | 154-184 | Divide NOS by TOS. Result to NOS. Pop Stack. |
| **32-BIT FLOATING-POINT DERIVED OPERATIONS** | | | | |
| SQRT | 81 | 01 | 782-870 | Square Root of TOS. Result to TOS. |
| SIN | 82 | 02 | 3796-4808 | Sine of TOS. Result to TOS. |
| COS | 83 | 03 | 3840-4878 | Cosine of TOS. Result to TOS. |
| TAN | 84 | 04 | 4894-5886 | Tangent of TOS. Result to TOS. |
| ASIN | 85 | 05 | 6230-7938 | Inverse Sine of TOS. Result to TOS. |
| ACOS | 86 | 06 | 6304-8284 | Inverse Cosine of TOS. Result to TOS. |
| ATAN | 87 | 07 | 4992-6536 | Inverse Tangent of TOS. Result to TOS. |
| LOG | 88 | 08 | 4474-7132 | Common Logarithm of TOS. Result to TOS. |
| LN | 89 | 09 | 4298-6956 | Natural Logarithm of TOS. Result to TOS. |
| EXP | 8A | 0A | 3794-4878 | e raised to power in TOS. Result to TOS. |
| PWR | 8B | 0B | 8290-12032 | NOS raised to power in TOS. Result to NOS. Pop Stack. |
| **DATA AND STACK MANIPULATION OPERATIONS** | | | | |
| NOP | 80 | 00 | 4 | No Operation. Clear or set SVREQ. |
| FIXS | 9F | 1F | 90-214 | Convert TOS from floating point format to fixed point format. |
| FIXD | 9E | 1E | 90-336 | |
| FLTS | 9D | 1D | 62-156 | Convert TOS from fixed point format to floating point format. |
| FLTD | 9C | 1C | 56-342 | |
| CHSS | F4 | 74 | 22-24 | Change sign of fixed point operand on TOS. |
| CHSD | B4 | 34 | 26-28 | |
| CHSF | 95 | 15 | 16-20 | Change sign of floating point operand on TOS. |
| PTOS | F7 | 77 | 16 | Push stack. Duplicate NOS in TOS. |
| PTOD | B7 | 37 | 20 | |
| PTOF | 97 | 17 | 20 | |
| POPS | F8 | 78 | 10 | Pop stack. Old NOS becomes new TOS. Old TOS rotates to bottom. |
| POPD | B8 | 38 | 12 | |
| POPF | 98 | 18 | 12 | |
| XCHS | F9 | 79 | 18 | Exchange TOS and NOS. |
| XCHD | B9 | 39 | 26 | |
| XCHF | 99 | 19 | 26 | |
| PUPI | 9A | 1A | 16 | Push floating point constant $\pi$ onto TOS. Previous TOS becomes NOS. |

## COMMAND DESCRIPTIONS

This section contains detailed descriptions of the APU commands. They are arranged in alphabetical order by command mnemonic. In the descriptions, TOS means Top Of Stack and NOS means Next On Stack.

All derived functions except Square Root use Chebyshev polynomial approximating algorithms. This approach is used to help minimize the internal microprogram, to minimize the maximum error values and to provide a relatively even distribution of errors over the data range. The basic arithmetic operations are used by the derived functions to compute the various Chebyshev terms. The basic operations may produce error codes in the status register as a result.

Execution times are listed in terms of clock cycles and may be converted into time values by multiplying by the clock period used. For example, an execution time of 44 clock cycles when running at a 3MHz rate translates to 14 microseconds (44 x 32$\mu$s = 14$\mu$s). Variations in execution cycles reflect the data dependency of the algorithms.

In some operations exponent overflow or underflow may be possible. When this occurs, the exponent returned in the result will be 128 greater or smaller than its true value.

Many of the functions use portions of the data stack as scratch storage during development of the results. Thus previous values in those stack locations will be lost. Scratch locations destroyed are listed in the command descriptions and shown with the crossed-out locations in the Stack Contents After diagram.

Table 1 is a summary of all the Am9511A commands. It shows the hex codes for each command, the mnemonic abbreviation, a brief description and the execution time in clock cycles. The commands are grouped by functional classes.

The command mnemonics in alphabetical order are shown below in Table 2.

**Table 2.**
**Command Mnemonics in Alphabetical Order.**

| | |
|---|---|
| ACOS | ARCCOSINE |
| ASIN | ARCSINE |
| ATAN | ARCTANGENT |
| CHSD | CHANGE SIGN DOUBLE |
| CHSF | CHANGE SIGN FLOATING |
| CHSS | CHANGE SIGN SINGLE |
| COS | COSINE |
| DADD | DOUBLE ADD |
| DDIV | DOUBLE DIVIDE |
| DMUL | DOUBLE MULTIPLY LOWER |
| DMUU | DOUBLE MULTIPLY UPPER |
| DSUB | DOUBLE SUBTRACT |
| EXP | EXPONENTIATION ($e^X$) |
| FADD | FLOATING ADD |
| FDIV | FLOATING DIVIDE |
| FIXD | FIX DOUBLE |
| FIXS | FIX SINGLE |
| FLTD | FLOAT DOUBLE |
| FLTS | FLOAT SINGLE |
| FMUL | FLOATING MULTIPLY |
| FSUB | FLOATING SUBTRACT |
| LOG | COMMON LOGARITHM |
| LN | NATURAL LOGARITHM |
| NOP | NO OPERATION |
| POPD | POP STACK DOUBLE |
| POPF | POP STACK FLOATING |
| POPS | POP STACK SINGLE |
| PTOD | PUSH STACK DOUBLE |
| PTOF | PUSH STACK FLOATING |
| PTOS | PUSH STACK SINGLE |
| PUPI | PUSH $\pi$ |
| PWR | POWER ($X^Y$) |
| SADD | SINGLE ADD |
| SDIV | SINGLE DIVIDE |
| SIN | SINE |
| SMUL | SINGLE MULTIPLY LOWER |
| SMUU | SINGLE MULTIPLY UPPER |
| SQRT | SQUARE ROOT |
| SSUB | SINGLE SUBTRACT |
| TAN | TANGENT |
| XCHD | EXCHANGE OPERANDS DOUBLE |
| XCHF | EXCHANGE OPERANDS FLOATING |
| XCHS | EXCHANGE OPERANDS SINGLE |

7

# ACOS

## 32-BIT FLOATING-POINT INVERSE COSINE

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

**Hex Coding:** 86 with sr = 1
06 with sr = 0

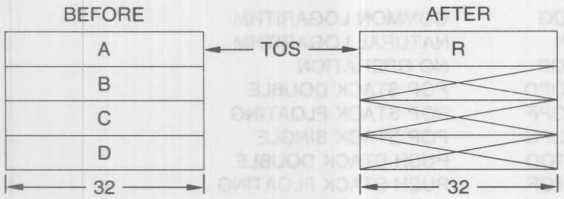
**Execution Time:** 6304 to 8284 clock cycles

**Description:**
The 32-bit floating-point operand A at the TOS is replaced by the 32-bit floating-point inverse cosine of A. The result R is a value in radians between 0 and $\pi$. Initial operands A, B, C and D are lost. ACOS will accept all input data values within the range of −1.0 to +1.0. Values outside this range will return an error code of 1100 in the status register.

**Accuracy:** ACOS exhibits a maximum relative error of 2.0 x $10^{-7}$ over the valid input data range.

**Status Affected:** Sign, Zero, Error Field

**STACK CONTENTS**




# ATAN

## 32-BIT FLOATING-POINT INVERSE TANGENT

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

**Hex Coding:** 87 with sr = 1
07 with sr = 0

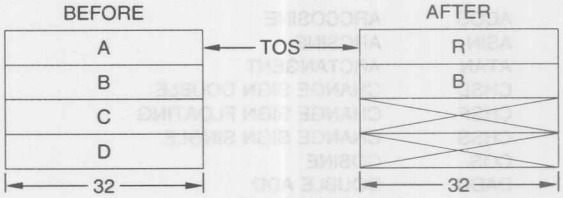
**Execution Time:** 4992 to 6536 clock cycles

**Description:**
The 32-bit floating-point operand A at the TOS is replaced by the 32-bit floating-point inverse tangent of A. The result R is a value in radians between $-\pi/2$ and $+\pi/2$. Initial operands A, C and D are lost. Operand B is unchanged.
ATAN will accept all input data values that can be represented in the floating point format.

**Accuracy:** ATAN exhibits a maximum relative error of 3.0 x $10^{-7}$ over the input data range.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




# ASIN

## 32-BIT FLOATING-POINT INVERSE SINE

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

**Hex Coding:** 85 with sr = 1
05 with sr = 0

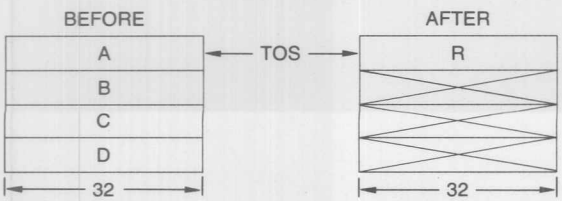
**Execution Time:** 6230 to 7938 clock cycles

**Description:**
The 32-bit floating-point operand A at the TOS is replaced by the 32-bit floating-point inverse sine of A. The result R is a value in radians between $-\pi/2$ and $+\pi/2$. Initial operands A, B, C and D are lost.
ASIN will accept all input data values within the range of −1.0 to +1.0. Values outside this range will return an error code of 1100 in the status register.

**Accuracy:** ASIN exhibits a maximum relative error of 4.0 x $10^{-7}$ over the valid input data range.

**Status Affected:** Sign, Zero, Error Field

**STACK CONTENTS**




# CHSD

## 32-BIT FIXED-POINT SIGN CHANGE

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 1 | 1 | 0 | 1 | 0 | 0 |

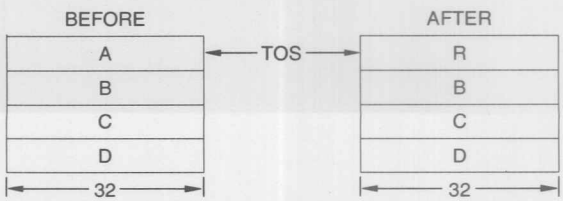
**Hex Coding:** B4 with sr = 1
34 with sr = 0

**Execution Time:** 26 to 28 clock cycles

**Description:**
The 32-bit fixed-point two's complement integer operand A at the TOS is subtracted from zero. The result R replaces A at the TOS. Other entries in the stack are not disturbed.
Overflow status will be set and the TOS will be returned unchanged when A is input as the most negative value possible in the format since no positive equivalent exists.

**Status Affected:** Sign, Zero, Error Field (overflow)

**STACK CONTENTS**



# CHSF

## 32-BIT FLOATING-POINT SIGN CHANGE

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 0 | 1 | 0 | 1 |

**Hex Coding:** 95 with sr = 1
15 with sr = 0

**Execution Time:** 16 to 20 clock cycles

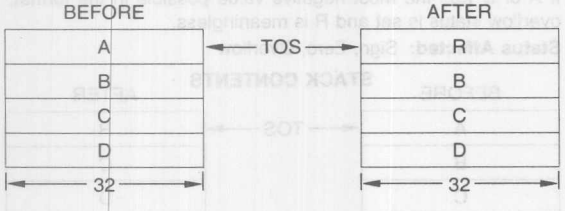
**Description:**

The sign of the mantissa of the 32-bit floating-point operand A at the TOS is inverted. The result R replaces A at the TOS. Other stack entries are unchanged.

If A is input as zero (mantissa MSB = 0), no change is made.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




# CHSS

## 16-BIT FIXED-POINT SIGN CHANGE

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 1 | 1 | 1 | 0 | 1 | 0 | 0 |

**Hex Coding:** F4 with sr = 1
74 with sr = 0

**Execution Time:** 22 to 24 clock cycles

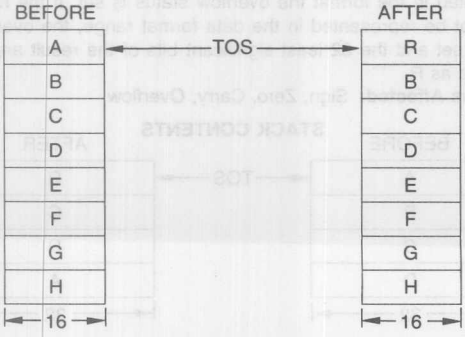
**Description:**

16-bit fixed-point two's complement integer operand A at the TOS is subtracted from zero. The result R replaces A at the TOS. All other operands are unchanged.

Overflow status will be set and the TOS will be returned unchanged when A is input as the most negative value possible in the format since no positive equivalent exists.

**Status Affected:** Sign, Zero, Overflow

**STACK CONTENTS**




# COS

## 32-BIT FLOATING-POINT COSINE

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

**Hex Coding:** 83 with sr = 1
03 with sr = 0

**Execution Time:** 3840 to 4878 clock cycles

**Description:**

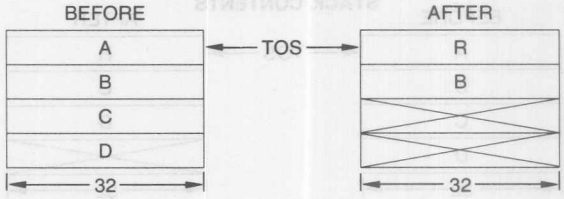
The 32-bit floating-point operand A at the TOS is replaced by R, the 32-bit floating-point cosine of A. A is assumed to be in radians. Operands A, C and D are lost. B is unchanged.

The COS function can accept any input data value that can be represented in the data format. All input values are range reduced to fall within an interval of $-\pi/2$ to $+\pi/2$ radians.

**Accuracy:** COS exhibits a maximum relative error of $5.0 \times 10^{-7}$ for all input data values in the range of $-2\pi$ to $+2\pi$ radians.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




# DADD

## 32-BIT FIXED-POINT ADD

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 1 | 0 | 1 | 1 | 0 | 0 |

**Hex Coding:** AC with sr = 1
2C with sr = 0

**Execution Time:** 20 to 22 clock cycles

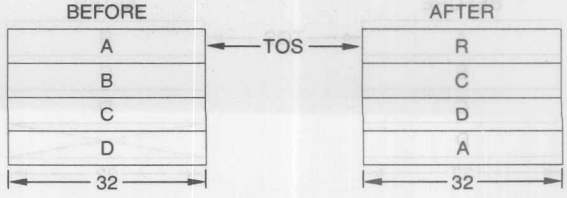
**Description:**

The 32-bit fixed-point two's complement integer operand A at the TOS is added to the 32-bit fixed-point two's complement integer operand B at the NOS. The result R replaces operand B and the Stack is moved up so that R occupies the TOS. Operand B is lost. Operands A, C and D are unchanged. If the addition generates a carry it is reported in the status register.

If the result is too large to be represented by the data format, the least significant 32 bits of the result are returned and overflow status is reported.

**Status Affected:** Sign, Zero, Carry, Error Field

**STACK CONTENTS**




7

## 32-BIT FIXED-POINT DIVIDE

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 1 | 0 | 1 | 1 | 1 | 1 |

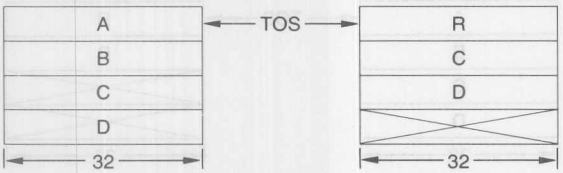
**Hex Coding:** AF with sr = 1
2F with sr = 0

**Execution Time:** 196 to 210 clock cycles when A ≠ 0
18 clock cycles when A = 0.

**Description:**
The 32-bit fixed-point two's complement integer operand B at NOS is divided by the 32-bit fixed-point two's complement integer operand A at the TOS. The 32-bit integer quotient R replaces B and the stack is moved up so that R occupies the TOS. No remainder is generated. Operands A and B are lost. Operands C and D are unchanged.
If A is zero, R is set equal to B and the divide-by-zero error status will be reported. If either A or B is the most negative value possible in the format, R will be meaningless and the overflow error status will be reported.

**Status Affected:** Sign, Zero, Error Field

**STACK CONTENTS**




# DMUL

## 32-BIT FIXED-POINT MULTIPLY, LOWER

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 1 | 0 | 1 | 1 | 1 | 0 |

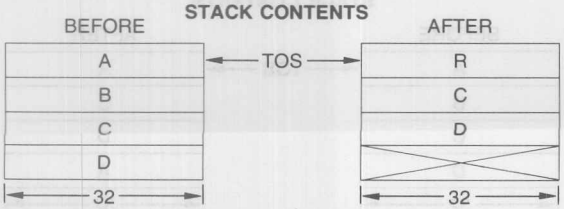
**Hex Coding:** AE with sr = 1
2E with sr = 0

**Execution Time:** 194 to 210 clock cycles

**Description:**
The 32-bit fixed-point two's complement integer operand A at the TOS is multiplied by the 32-bit fixed-point two's complement integer operand B at the NOS. The 32-bit least significant half of the product R replaces B and the stack is moved up so that R occupies the TOS. The most significant half of the product is lost. Operands A and B are lost. Operands C and D are unchanged.
The overflow status bit is set if the discarded upper half was non-zero. If either A or B is the most negative value that can be represented in the format, that value is returned as R and the overflow status is set.

**Status Affected:** Sign, Zero, Overflow

**STACK CONTENTS**




## 32-BIT FIXED-POINT MULTIPLY, UPPER

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 1 | 1 | 0 | 1 | 1 | 0 |

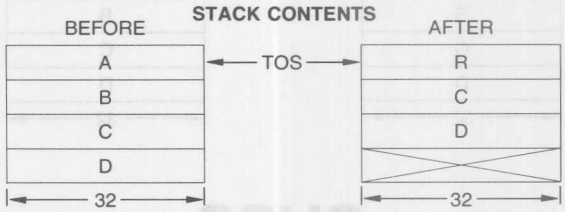
**Hex Coding:** B6 with sr = 1
36 with sr = 0

**Execution Time:** 182 to 218 clock cycles

**Description:**
The 32-bit fixed-point two's complement integer operand A at the TOS is multiplied by the 32-bit fixed-point two's complement integer operand B at the NOS. The 32-bit most significant half of the product R replaces B and the stack is moved up so that R occupies the TOS. The least significant half of the product is lost. Operands A and B are lost. Operands C and D are unchanged.
If A or B was the most negative value possible in the format, overflow status is set and R is meaningless.

**Status Affected:** Sign, Zero, Overflow

**STACK CONTENTS**




# DSUB

## 32-BIT FIXED-POINT SUBTRACT

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 1 | 0 | 1 | 1 | 0 | 1 |

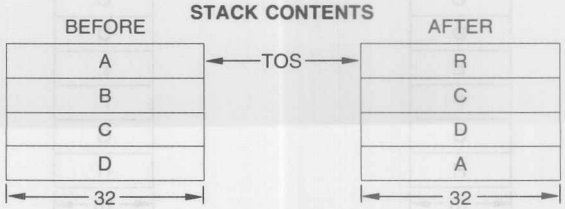
**Hex Coding:** AD with sr = 1
2D with sr = 0

**Execution Time:** 38 to 40 clock cycles

**Description:**
The 32-bit fixed-point two's complement operand A at the TOS is subtracted from the 32-bit fixed-point two's complement operand B at the NOS. The difference R replaces operand B and the stack is moved up so that R occupies the TOS. Operand B is lost. Operands A, C and D are unchanged.
If the subtraction generates a borrow it is reported in the carry status bit. If A is the most negative value that can be represented in the format the overflow status is set. If the result cannot be represented in the data format range, the overflow bit is set and the 32 least significant bits of the result are returned as R.

**Status Affected:** Sign, Zero, Carry, Overflow

**STACK CONTENTS**



# EXP

## 32-BIT FLOATING-POINT $e^X$

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

**Hex Coding:** 8A with sr = 1
0A with sr = 0

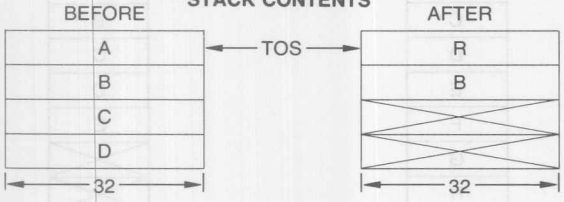
**Execution Time:** 3794 to 4878 clock cycles for $|A| \leq 1.0 \times 2^5$
34 clock cycles for $|A| > 1.0 \times 2^5$

**Description:**
The base of natural logarithms, e, is raised to an exponent value specified by the 32-bit floating-point operand A at the TOS. The result R of $e^A$ replaces A. Operands A, C and D are lost. Operand B is unchanged.
EXP accepts all input data values within the range of $-1.0 \times 2^{+5}$ to $+1.0 \times 2^{+5}$. Input values outside this range will return a code of 1100 in the error field of the status register.

**Accuracy:** EXP exhibits a maximum relative error of $5.0 \times 10^{-7}$ over the valid input data range.

**Status Affected:** Sign, Zero, Error Field

**STACK CONTENTS**




# FADD

## 32-BIT FLOATING-POINT ADD

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

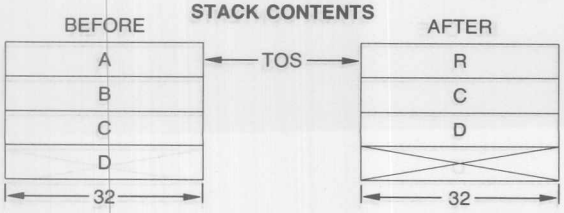
**Hex Coding:** 90 with sr = 1
10 with sr = 0

**Execution Time:** 54 to 368 clock cycles for A ≠ 0
24 clock cycles for A = 0

**Description:**
32-bit floating-point operand A at the TOS is added to 32-bit floating-point operand B at the NOS. The result R replaces B and the stack is moved up so that R occupies the TOS. Operands A and B are lost. Operands C and D are unchanged.
Exponent alignment before the addition and normalization of the result accounts for the variation in execution time. Exponent overflow and underflow are reported in the status register, in which case the mantissa is correct and the exponent is offset by 128.

**Status Affected:** Sign, Zero, Error Field

**STACK CONTENTS**




# FDIV

## 32-BIT FLOATING-POINT DIVIDE

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 0 | 0 | 1 | 1 |

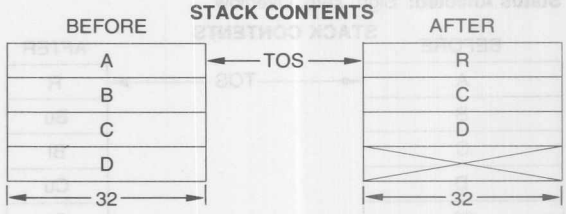
**Hex Coding:** 93 with sr = 1
13 with sr = 0

**Execution Time:** 154 to 184 clock cycles for A ≠ 0
22 clock cycles for A = 0

**Description:**
32-bit floating-point operand B at NOS is divided by 32-bit floating-point operand A at the TOS. The result R replaces B and the stack is moved up so that R occupies the TOS. Operands A and B are lost. Operands C and D are unchanged.
If operand A is zero, R is set equal to B and the divide-by-zero error is reported in the status register. Exponent overflow or underflow is reported in the status register, in which case the mantissa portion of the result is correct and the exponent portion is offset by 128.

**Status Affected:** Sign, Zero, Error Field

**STACK CONTENTS**




# FIXD

## 32-BIT FLOATING-POINT TO 32-BIT FIXED-POINT CONVERSION

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 1 | 1 | 1 | 0 |

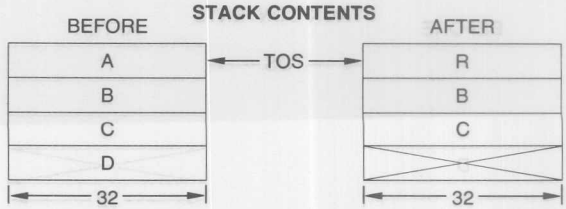
**Hex Coding:** 9E with sr = 1
1E with sr = 0

**Execution Time:** 90 to 336 clock cycles

**Description:**
32-bit floating-point operand A at the TOS is converted to a 32-bit fixed-point two's complement integer. The result R replaces A. Operands A and D are lost. Operands B and C are unchanged.
If the integer portion of A is larger than 31 bits when converted, the overflow status will be set and A will not be changed. Operand D, however, will still be lost.

**Status Affected:** Sign, Zero Overflow

**STACK CONTENTS**




7

# FIXS

## 32-BIT FLOATING-POINT TO 16-BIT FIXED-POINT CONVERSION

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

**Hex Coding:** 9F with sr = 1
1F with sr = 0

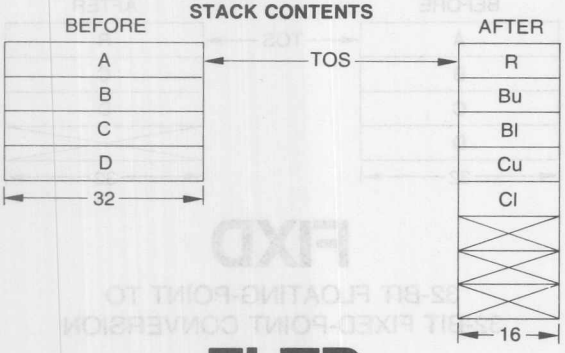
**Execution Time:** 90 to 214 clock cycles

**Description:**
32-bit floating-point operand A at the TOS is converted to a 16-bit fixed-point two's complement integer. The result R replaces the lower half of A and the stack is moved up by two bytes so that R occupies the TOS. Operands A and D are lost. Operands B and C are unchanged, but appear as upper (u) and lower (l) halves on the 16-bit wide stack if they are 32-bit operands.

If the integer portion of A is larger than 15 bits when converted, the overflow status will be set and A will not be changed. Operand D, however, will still be lost.

**Status Affected:** Sign, Zero, Overflow

**STACK CONTENTS**




# FLTD

## 32-BIT FIXED-POINT TO 32-BIT FLOATING-POINT CONVERSION

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 1 | 1 | 0 | 0 |

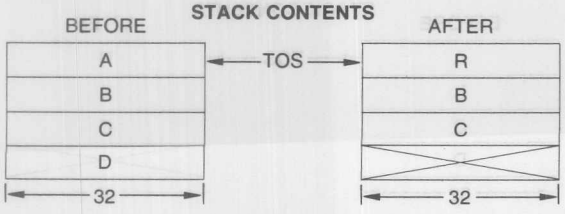
**Hex Coding:** 9C with sr = 1
1C with sr = 0

**Execution Time:** 56 to 342 clock cycles

**Description:**
32-bit fixed-point two's complement integer operand A at the TOS is converted to a 32-bit floating-point number. The result R replaces A at the TOS. Operands A and D are lost. Operands B and C are unchanged.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




# FLTS

## 16-BIT FIXED-POINT TO 32-BIT FLOATING-POINT CONVERSION

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 1 | 1 | 0 | 1 |

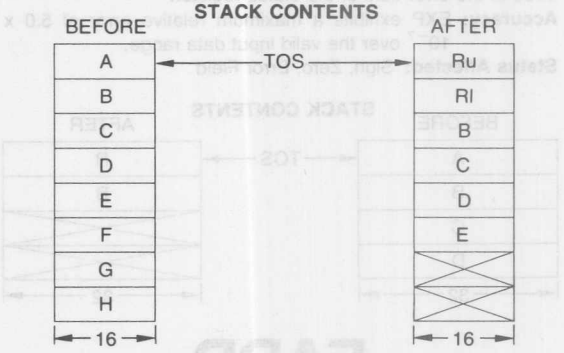
**Hex Coding:** 9D with sr = 1
1D with sr = 0

**Execution Time:** 62 to 156 clock cycles

**Description:**
16-bit fixed-point two's complement integer A at the TOS is converted to a 32-bit floating-point number. The lower half of the result R (Rl) replaces A, the upper half (Ru) replaces H and the stack is moved down so that Ru occupies the TOS. Operands A, F, G and H are lost. Operands B, C, D and E are unchanged.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




# FMUL

## 32-BIT FLOATING-POINT MULTIPLY

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 0 | 0 | 1 | 0 |

**Hex Coding:** 92 with sr = 1
12 with sr = 0

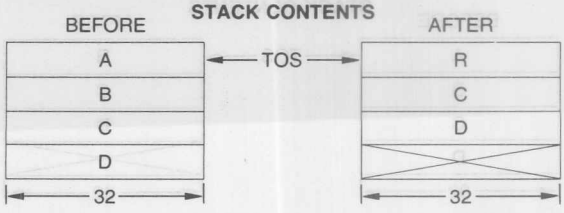
**Execution Time:** 146 to 168 clock cycles

**Description:**
32-bit floating-point operand A at the TOS is multiplied by the 32-bit floating-point operand B at the NOS. The normalized result R replaces B and the stack is moved up so that R occupies the TOS. Operands A and B are lost. Operands C and D are unchanged.

Exponent overflow or underflow is reported in the status register, in which case the mantissa portion of the result is correct and the exponent portion is offset by 128.

**Status Affected:** Sign, Zero, Error Field

**STACK CONTENTS**



# FSUB

## 32-BIT FLOATING-POINT SUBTRACTION

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

**Hex Coding:** 91 with sr = 1
11 with sr = 0

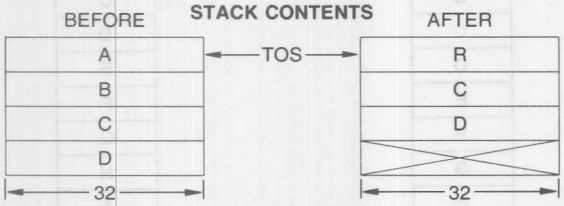
**Execution Time:** 70 to 370 clock cycles for A ≠ 0
26 clock cycles for A = 0

**Description:**
32-bit floating-point operand A at the TOS is subtracted from 32-bit floating-point operand B at the NOS. The normalized difference R replaces B and the stack is moved up so that R occupies the TOS. Operands A and B are lost. Operands C and D are unchanged.

Exponent alignment before the subtraction and normalization of the result account for the variation in execution time.

Exponent overflow or underflow is reported in the status register in which case the mantissa portion of the result is correct and the exponent portion is offset by 128.

**Status Affected:** Sign, Zero, Error Field (overflow)




# LOG

## 32-BIT FLOATING-POINT COMMON LOGARITHM

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

**Hex Coding:** 88 with sr = 1
08 with sr = 0

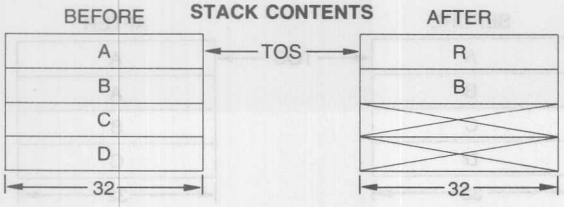
**Execution Time:** 4474 to 7132 clock cycles for A > 0
20 clock cycles for A ≤ 0

**Description:**
The 32-bit floating-point operand A at the TOS is replaced by R, the 32-bit floating-point common logarithm (base 10) of A. Operands A, C and D are lost. Operand B is unchanged.

The LOG function accepts any positive input data value that can be represented by the data format. If LOG of a non-positive value is attempted an error status of 0100 is returned.

**Accuracy:** LOG exhibits a maximum absolute error of $2.0 \times 10^{-7}$ for the input range from 0.1 to 10, and a maximum relative error of $2.0 \times 10^{-7}$ for positive values less than 0.1 or greater than 10.

**Status Affected:** Sign, Zero, Error Field




# LN

## 32-BIT FLOATING-POINT NATURAL LOGARITHM

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 0 | 1 | 0 | 0 | 1 |

**Hex Coding:** 89 with sr = 1
09 with sr = 0

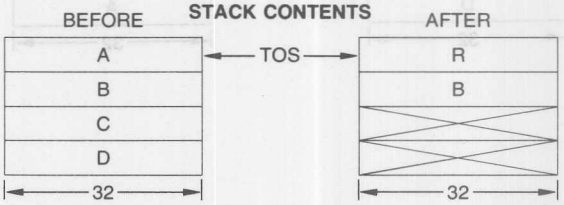
**Execution Time:** 4298 to 6956 clock cycles for A > 0
20 clock cycles for A≤ 0

**Description:**
The 32-bit floating-point operand A at the TOS is replaced by R, the 32-bit floating-point natural logarithm (base e) of A. Operands A, C and D are lost. Operand B is unchanged.

The LN function accepts all positive input data values that can be represented by the data format. If LN of a non-positive number is attempted an error status of 0100 is returned.

**Accuracy:** LN exhibits a maximum absolute error of $2 \times 10^{-7}$ for the input range from $e^{-1}$ to e, and a maximum relative error of $2.0 \times 10^{-7}$ for positive values less than $e^{-1}$ or greater than e.

**Status Affected:** Sign, Zero, Error Field




# NOP

## NO OPERATION

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Hex Coding:** 80 with sr = 1
00 with sr = 0

**Execution Time:** 4 clock cycles

**Description:**
The NOP command performs no internal data manipulations. It may be used to set or clear the service request interface line without changing the contents of the stack.

**Status Affected:** The status byte is cleared to all zeroes.

7

# POPD

## 32-BIT STACK POP

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 1 | 1 | 1 | 0 | 0 | 0 |

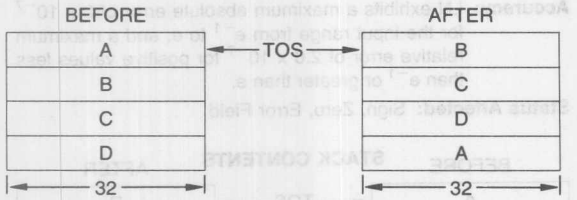
**Hex Coding:** B8 with sr = 1
38 with sr = 0

**Execution Time:** 12 clock cycles

**Description:**
The 32-bit stack is moved up so that the old NOS becomes the new TOS. The previous TOS rotates to the bottom of the stack. All operand values are unchanged. POPD and POPF execute the same operation.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




# POPS

## 16-BIT STACK POP

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 1 | 1 | 1 | 1 | 0 | 0 | 0 |

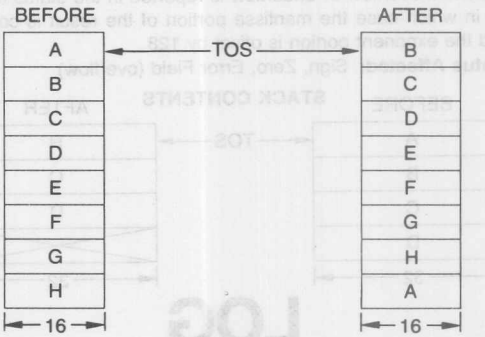
**Hex Coding:** F8 with sr = 1
78 with sr = 0

**Execution Time:** 10 clock cycles

**Description:**
The 16-bit stack is moved up so that the old NOS becomes the new TOS. The previous TOS rotates to the bottom of the stack. All operand values are unchanged.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




# POPF

## 32-BIT STACK POP

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

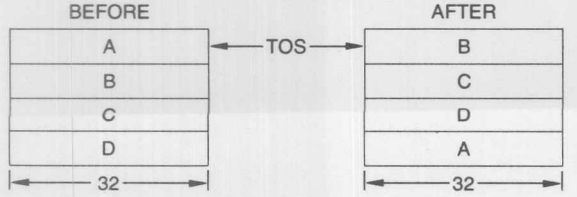
**Hex Coding:** 98 with sr = 1
18 with sr = 0

**Execution Time:** 12 clock cycles

**Description:**
The 32-bit stack is moved up so that the old NOS becomes the new TOS. The old TOS rotates to the bottom of the stack. All operand values are unchanged. POPF and POPD execute the same operation.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




# PTOD

## PUSH 32-BIT TOS ONTO STACK

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 1 | 1 | 0 | 1 | 1 | 1 |

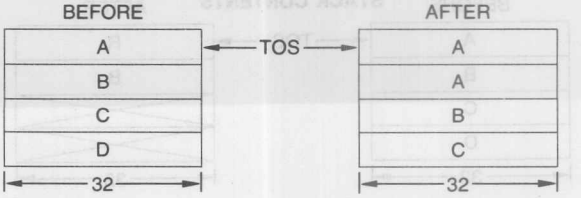
**Hex Coding:** B7 with sr = 1
37 with sr = 0

**Execution Time:** 20 clock cycles

**Description:**
The 32-bit stack is moved down and the previous TOS is copied into the new TOS location. Operand D is lost. All other operand values are unchanged. PTOD and PTOF execute the same operation.

**Status Affected:** Sign, Zero

**STACK CONTENTS**



# PTOF

## PUSH 32-BIT TOS ONTO STACK

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 0 | 1 | 1 | 1 |

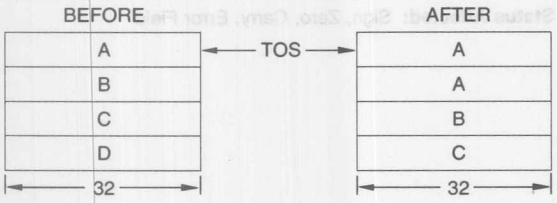
**Hex Coding:** 97 with sr = 1
17 with sr = 0

**Execution Time:** 20 clock cycles

**Description:**
The 32-bit stack is moved down and the previous TOS is copied into the new TOS location. Operand D is lost. All other operand values are unchanged. PTOF and PTOD execute the same operation.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




# PTOS

## PUSH 16-BIT TOS ONTO STACK

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 1 | 1 | 1 | 0 | 1 | 1 | 1 |

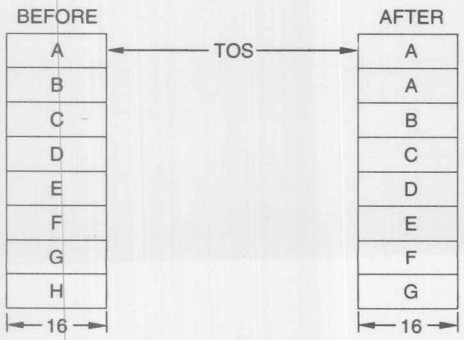
**Hex Coding:** F7 with sr = 1
77 with sr = 0

**Execution Time:** 16 clock cycles

**Description:**
The 16-bit stack is moved down and the previous TOS is copied into the new TOS location. Operand H is lost and all other operand values are unchanged.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




# PUPI

## PUSH 32-BIT FLOATING-POINT $\pi$

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 1 | 0 | 1 | 0 |

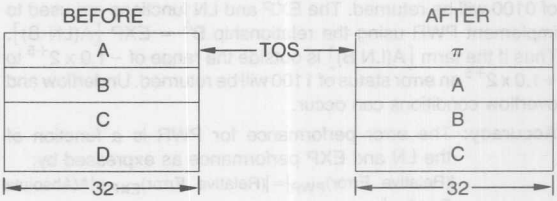
**Hex Coding:** 9A with sr = 1
1A with sr = 0

**Execution Time:** 16 clock cycles

**Description:**
The 32-bit stack is moved down so that the previous TOS occupies the new NOS location. 32-bit floating-point constant $\pi$ is entered into the new TOS location. Operand D is lost. Operands A, B and C are unchanged.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




7

# PWR

## 32-BIT FLOATING-POINT $X^Y$

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 0 | 1 | 0 | 1 | 1 |

**Hex Coding:** 8B with sr = 1
0B with sr = 0

**Execution Time:** 8290 to 12032 clock cycles

**Description:**

32-bit floating-point operand B at the NOS is raised to the power specified by the 32-bit floating-point operand A at the TOS. The result R of $B^A$ replaces B and the stack is moved up so that R occupies the TOS. Operands A, B, and D are lost. Operand C is unchanged.

The PWR function accepts all input data values that can be represented in the data format for operand A and all positive values for operand B. If operand B is non-positive an error status of 0100 will be returned. The EXP and LN functions are used to implement PWR using the relationship $B^A = EXP\,[A(LN\ B)]$. Thus if the term $[A(LN\ B)]$ is outside the range of $-1.0 \times 2^{+5}$ to $+1.0 \times 2^{+5}$ an error status of 1100 will be returned. Underflow and overflow conditions can occur.

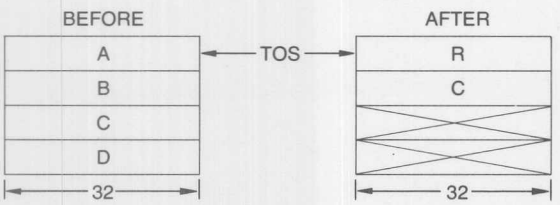
**Accuracy:** The error performance for PWR is a function of the LN and EXP performance as expressed by:

$$|(\text{Relative Error})_{PWR}| = |(\text{Relative Error})_{EXP} + |A(\text{Absolute Error})_{LN}|$$

The maximum relative error for PWR occurs when A is at its maximum value while $[A(LN\ B)]$ is near $1.0 \times 2^5$ and the EXP error is also at its maximum. For most practical applications the relative error for PWR will be less than $7.0 \times 10^{-7}$.

**Status Affected:** Sign, Zero, Error Field

**STACK CONTENTS**




# SADD

## 16-BIT FIXED-POINT ADD

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 1 | 1 | 0 | 1 | 1 | 0 | 0 |

**Hex Coding:** EC with sr = 1
6C with sr = 0

**Execution Time:** 16 to 18 clock cycles

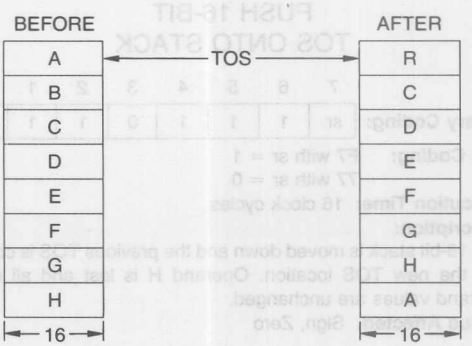
**Description:**

16-bit fixed-point two's complement integer operand A at the TOS is added to 16-bit fixed-point two's complement integer operand B at the NOS. The result R replaces B and the stack is moved up so that R occupies the TOS. Operand B is lost. All other operands are unchanged.

If the addition generates a carry bit it is reported in the status register. If an overflow occurs it is reported in the status register and the 16 least significant bits of the result are returned.

**Status Affected:** Sign, Zero, Carry, Error Field

**STACK CONTENTS**



# SDIV

## 16-BIT FIXED-POINT DIVIDE

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 1 | 1 | 0 | 1 | 1 | 1 | 1 |

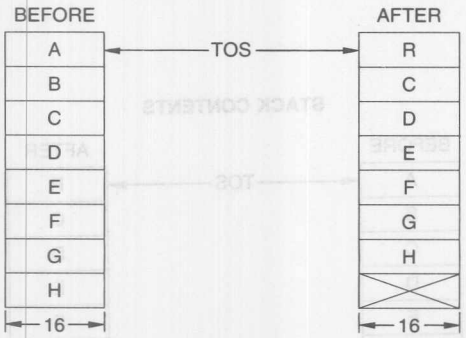
**Hex Coding:** EF with sr = 1
6F with sr = 0

**Execution Time:** 84 to 94 clock cycles for A ≠ 0
14 clock cycles for A = 0

**Description:**
16-bit fixed-point two's complement integer operand B at the NOS is divided by 16-bit fixed-point two's complement integer operand A at the TOS. The 16-bit integer quotient R replaces B and the stack is moved up so that R occupies the TOS. No remainder is generated. Operands A and B are lost. All other operands are unchanged.
If A is zero, R will be set equal to B and the divide-by-zero error status will be reported.

**Status Affected:** Sign, Zero, Error Field

**STACK CONTENTS**




# SIN

## 32-BIT FLOATING-POINT SINE

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

**Hex Coding:** 82 with sr = 1
02 with sr = 0

**Execution Time:** 3796 to 4808 clock cycles for $|A| > 2^{-12}$ radians
30 clock cycles for $|A| \leq 2^{-12}$ radians

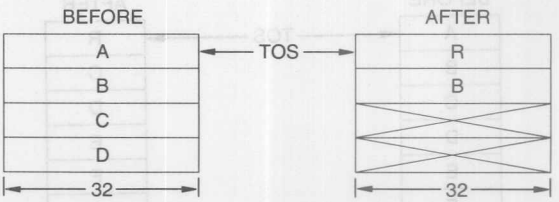
**Description:**
The 32-bit floating-point operand A at the TOS is replaced by R, the 32-bit floating-point sine of A. A is assumed to be in radians. Operands A, C and D are lost. Operand B is unchanged.

The SIN function will accept any input data value that can be represented by the data format. All input values are range reduced to fall within the interval $-\pi/2$ to $+\pi/2$ radians.

**Accuracy:** SIN exhibits a maximum relative error of $5.0 \times 10^{-7}$ for input values in the range of $-2\pi$ to $+2\pi$ radians.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




7

# SMUL

## 16-BIT FIXED-POINT MULTIPLY, LOWER

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 1 | 1 | 0 | 1 | 1 | 1 | 0 |

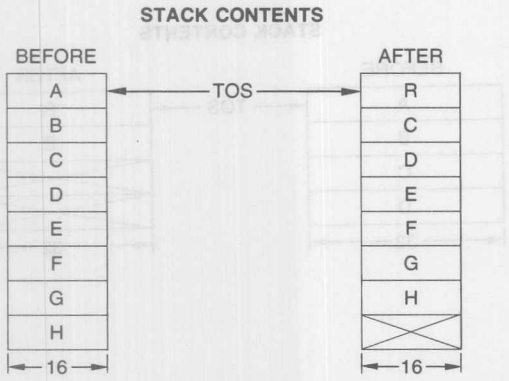
**Hex Coding:** EE with sr = 1
6E with sr = 0

**Execution Time:** 84 to 94 clock cycles

**Description:**

16-bit fixed-point two's complement integer operand A at the TOS is multiplied by the 16-bit fixed-point two's complement integer operand B at the NOS. The 16-bit least significant half of the product R replaces B and the stack is moved up so that R occupies the TOS. The most significant half of the product is lost. Operands A and B are lost. All other operands are unchanged. The overflow status bit is set if the discarded upper half was non-zero. If either A or B is the most negative value that can be represented in the format, that value is returned as R and the overflow status is set.

**Status Affected:** Sign, Zero, Error Field




# SMUU

## 16-BIT FIXED-POINT MULTIPLY, UPPER

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 1 | 1 | 1 | 0 | 1 | 1 | 0 |

**Hex Coding:** F6 with sr = 1
76 with sr = 0

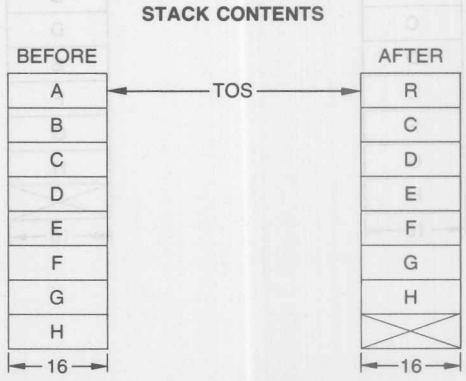
**Execution Time:** 80 to 98 clock cycles

**Description:**

16-bit fixed-point two's complement integer operand A at the TOS is multiplied by the 16-bit fixed-point two's complement integer operand B at the NOS. The 16-bit most significant half of the product R replaces B and the stack is moved up so that R occupies the TOS. The least significant half of the product is lost. Operands A and B are lost. All other operands are unchanged.

If either A or B is the most negative value that can be represented in the format, that value is returned as R and the overflow status is set.

**Status Affected:** Sign, Zero, Error Field



# SQRT

## 32-BIT FLOATING-POINT SQUARE ROOT

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**Hex Coding:** 81 with sr = 1
01 with sr = 0

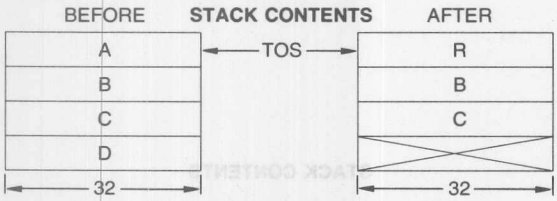
**Execution Time:** 782 to 870 clock cycles

**Description:**

32-bit floating-point operand A at the TOS is replaced by R, the 32-bit floating-point square root of A. Operands A and D are lost. Operands B and C are not changed.

SQRT will accept any non-negative input data value that can be represented by the data format. If A is negative an error code of 0100 will be returned in the status register.

**Status Affected:** Sign, Zero, Error Field




# SSUB

## 16-BIT FIXED-POINT SUBTRACT

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 1 | 1 | 0 | 1 | 1 | 0 | 1 |

**Hex Coding:** ED with sr = 1
6D with sr = 0

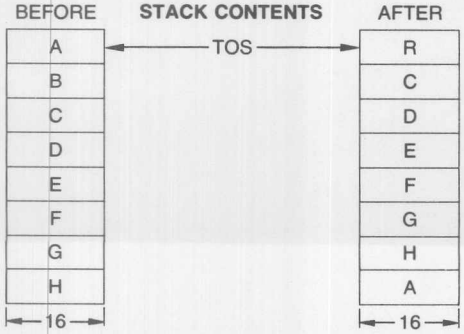
**Execution Time:** 30 to 32 clock cycles

**Description:**

16-bit fixed-point two's complement integer operand A at the TOS is subtracted from 16-bit fixed-point two's complement integer operand B at the NOS. The result R replaces B and the stack is moved up so that R occupies the TOS. Operand B is lost. All other operands are unchanged.

If the subtraction generates a borrow it is reported in the carry status bit. If A is the most negative value that can be represented in the format the overflow status is set. If the result cannot be represented in the format range, the overflow status is set and the 16 least significant bits of the result are returned as R.

**Status Affected:** Sign, Zero, Carry, Error Field




# TAN

## 32-BIT FLOATING-POINT TANGENT

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

**Hex Coding:** 84 with sr = 1
04 with sr = 0

**Execution Time:** 4894 to 5886 clock cycles for $|A| > 2^{-12}$ radians
30 clock cycles for $|A| \leq 2^{-12}$ radians

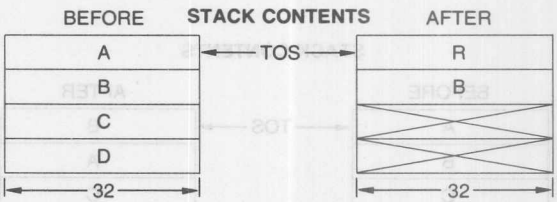
**Description:**

The 32-bit floating-point operand A at the TOS is replaced by the 32-bit floating-point tangent of A. Operand A is assumed to be in radians. A, C and D are lost. B is unchanged.

The TAN function will accept any input data value that can be represented in the data format. All input data values are range-reduced to fall within $-\pi/4$ to $+\pi/4$ radians. TAN is unbounded for input values near odd multiples of $\pi/2$ and in such cases the overflow bit is set in the status register. For angles smaller than $2^{-12}$ radians, TAN returns A as the tangent of A.

**Accuracy:** TAN exhibits a maximum relative error of $5.0 \times 10^{-7}$ for input data values in the range of $-2\pi$ to $+2\pi$ radians except for data values near odd multiples of $\pi/2$.

**Status Affected:** Sign, Zero, Error Field (overflow)




# XCHD

## EXCHANGE 32-BIT STACK OPERANDS

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 1 | 1 | 1 | 0 | 0 | 1 |

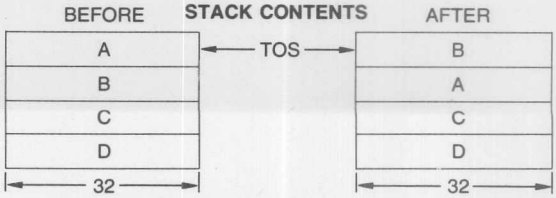
**Hex Coding:** B9 with sr = 1
39 with sr = 0

**Execution Time:** 26 clock cycles

**Description:**

32-bit operand A at the TOS and 32-bit operand B at the NOS are exchanged. After execution, B is at the TOS and A is at the NOS. All operands are unchanged. XCHD and XCHF execute the same operation.

**Status Affected:** Sign, Zero




7

# XCHF

## EXCHANGE 32-BIT STACK OPERANDS

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 1 | 0 | 0 | 1 |

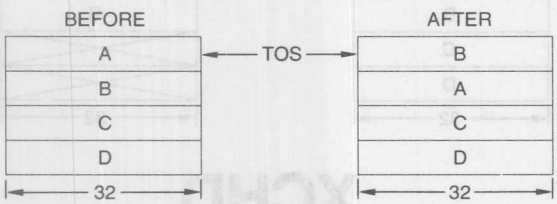
**Hex Coding:** 99 with sr = 1
19 with sr = 0

**Execution Time:** 26 clock cycles

**Description:**
32-bit operand A at the TOS and 32-bit operand B at the NOS are exchanged. After execution, B is at the TOS and A is at the NOS. All operands are unchanged. XCHD and XCHF execute the same operation.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




# XCHS

## EXCHANGE 16-BIT STACK OPERANDS

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 1 | 1 | 1 | 1 | 0 | 0 | 1 |

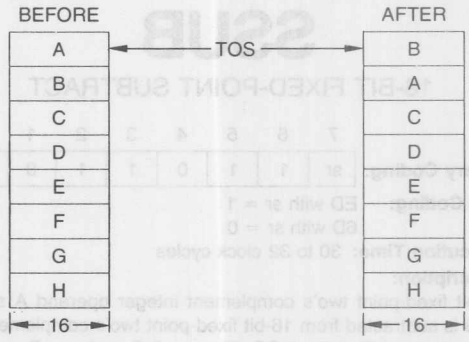
**Hex Coding:** F9 with sr = 1
79 with sr = 0

**Execution Time:** 18 clock cycles

**Description:**
16-bit operand A at the TOS and 16-bit operand B at the NOS are exchanged. After execution, B is at the TOS and A is at the NOS. All operand values are unchanged.

**Status Affected:** Sign, Zero

**STACK CONTENTS**



## MAXIMUM RATINGS beyond which useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| VDD with Respect to VSS | −0.5V to +15.0V |
| VCC with Respect to VSS | −0.5V to +7.0V |
| All Signal Voltages with Respect to VSS | −0.5V to +7.0V |
| Power Dissipation (Package Limitation) | 2.0W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGE

| Part Number | Ambient Temperature | VSS | VCC | VDD |
|---|---|---|---|---|
| Am9511ADC | $0°C \leq T_A \leq +70°C$ | 0V | +5.0V ±5% | +12V ±5% |
| Am9511ADM | $-55°C \leq T_A \leq +125°C$ | 0V | +5.0V ±10% | +12V ±10% |

## ELECTRICAL CHARACTERISTICS Over Operating Range (Note 1)

| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| VOH | Output HIGH Voltage | IOH = −200μA | 3.7 | | | Volts |
| VOL | Output LOW Voltage | IOL = 3.2mA | | | 0.4 | Volts |
| VIH | Input HIGH Voltage | | 2.0 | | VCC | Volts |
| VIL | Input LOW Voltage | | −0.5 | | 0.8 | Volts |
| IIX | Input Load Current | $VSS \leq VI \leq VCC$ | | | ±10 | μA |
| IOZ | Data Bus Leakage | VO = 0.4V | | | 10 | μA |
| | | VO = VCC | | | 10 | |
| ICC | VCC Supply Current | $T_A$ = +25°C | | 50 | 90 | mA |
| | | $T_A$ = 0°C | | | 95 | |
| | | $T_A$ = −55°C | | | 100 | |
| IDD | VDD Supply Current | $T_A$ = +25°C | | 50 | 90 | mA |
| | | $T_A$ = 0°C | | | 95 | |
| | | $T_A$ = −55°C | | | 100 | |
| CO | Output Capacitance | fc = 1.0MHz, Inputs = 0V | | 8 | 10 | pF |
| CI | Input Capacitance | | | 5 | 8 | pF |
| CIO | I/O Capacitance | | | 10 | 12 | pF |

7

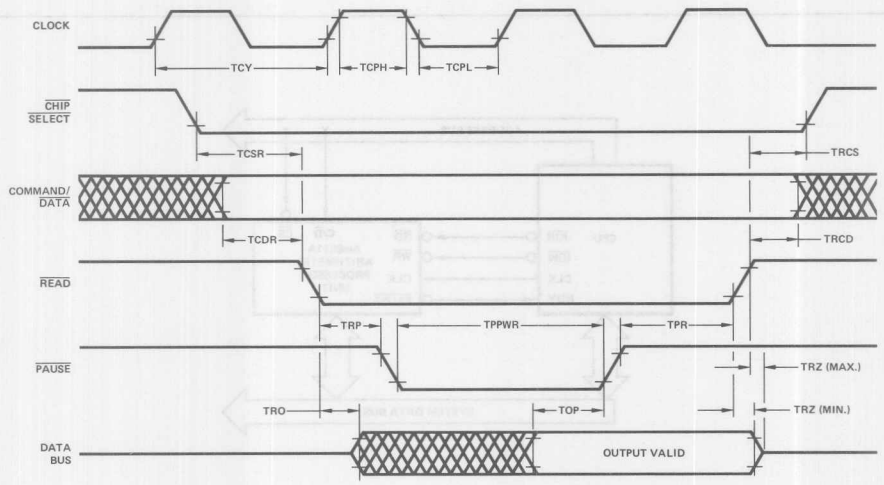
| Parameters | Description | | Am9511A Min. | Am9511A Max. | Am9511A-1 Min. | Am9511A-1 Max. | Units |
|---|---|---|---|---|---|---|---|
| TAPW | $\overline{EACK}$ LOW Pulse Width | | 100 | | 75 | | ns |
| TCDR | C/$\overline{D}$ to $\overline{RD}$ LOW Set up Time | | 0 | | 0 | | ns |
| TCDW | C/$\overline{D}$ to $\overline{WR}$ LOW Set up Time | | 0 | | 0 | | ns |
| TCPH | Clock Pulse HIGH Width | | 200 | | 140 | | ns |
| TCPL | Clock Pulse LOW Width | | 240 | | 160 | | ns |
| TCSR | $\overline{CS}$ LOW to $\overline{RD}$ LOW Set up Time | | 0 | | 0 | | ns |
| TCSW | $\overline{CS}$ LOW to $\overline{WR}$ LOW Set up Time | | 0 | | 0 | | ns |
| TCY | Clock Period | | 480 | 5000 | 320 | 3300 | ns |
| TDW | Data Bus Stable to $\overline{WR}$ HIGH Set up Time | | 150 | | 100 (Note 9) | | ns |
| TEAE | $\overline{EACK}$ LOW to $\overline{END}$ HIGH Delay | | | 200 | | 175 | ns |
| TEPW | $\overline{END}$ LOW Pulse Width (Note 4) | | 400 | | 300 | | ns |
| TOP | Data Bus Output Valid to $\overline{PAUSE}$ HIGH Delay | | 0 | | 0 | | ns |
| TPPWR | $\overline{PAUSE}$ LOW Pulse Width Read (Note 5) | Data | 3.5TCY+50 | 5.5TCY+300 | 3.5TCY+50 | 5.5TCY+200 | ns |
| | | Status | 1.5TCY+50 | 3.5TCY+300 | 1.5TCY+50 | 3.5TCY+200 | |
| TPPWW | $\overline{PAUSE}$ LOW Pulse Width Write (Note 8) | | | 50 | | 50 | ns |
| TPR | $\overline{PAUSE}$ HIGH to $\overline{RD}$ HIGH Hold Time | | 0 | | 0 | | ns |
| TPW | $\overline{PAUSE}$ HIGH to $\overline{WR}$ HIGH Hold Time | | 0 | | 0 | | ns |
| TRCD | $\overline{RD}$ HIGH to C/$\overline{D}$ Hold Time | | 0 | | 0 | | ns |
| TRCS | $\overline{RD}$ HIGH to $\overline{CS}$ HIGH Hold Time | | 0 | | 0 | | ns |
| TRO | $\overline{RD}$ LOW to Data Bus ON Delay | | 50 | | 50 | | ns |
| TRP | $\overline{RD}$ LOW to $\overline{PAUSE}$ LOW Delay (Note 6) | | | 150 | | 100 (Note 9) | ns |
| TRZ | $\overline{RD}$ HIGH to Data Bus OFF Delay | | 50 | 200 | 50 | 150 | ns |
| TSAPW | $\overline{SVACK}$ LOW Pulse Width | | 100 | | 75 | | ns |
| TSAR | $\overline{SVACK}$ LOW to SVREQ LOW Delay | | | 300 | | 200 | ns |
| TWCD | $\overline{WR}$ HIGH to C/$\overline{D}$ Hold Time | | 60 | | 30 | | ns |
| TWCS | $\overline{WR}$ HIGH to $\overline{CS}$ HIGH Hold Time | | 60 | | 30 | | ns |
| TWD | $\overline{WR}$ HIGH to Data Bus Hold Time | | 20 | | 20 | | ns |
| TWI | Write Inactive Time (Note 8) | Command | 3TCY | | 3TCY | | ns |
| | | Data | 4TCY | | 4TCY | | |
| TWP | $\overline{WR}$ LOW to $\overline{PAUSE}$ LOW Delay (Note 6) | | | 150 | | 100 (Note 9) | ns |

NOTES

1. Typical values are for $T_A = 25°C$, nominal supply voltages and nominal processing parameters.
2. Switching parameters are listed in alphabetical order.
3. Test conditions assume transition times of 20ns or less, output loading of one TTL gate plus 100pF and timing reference levels of 0.8V and 2.0V.
4. $\overline{END}$ low pulse width is specified for $\overline{EACK}$ tied to VSS. Otherwise TEAE applies.
5. Minimum values shown assume no previously entered command is being executed for the data access. If a previously entered command is being executed, $\overline{PAUSE}$ LOW Pulse Width is the time to complete execution plus the time shown. Status may be read at any time without exceeding the time shown.
6. $\overline{PAUSE}$ is pulled low for both command and data operations.
7. TEX is the execution time of the current command (see the Command Execution Times table).
8. $\overline{PAUSE}$ low pulse width is less than 50ns when writing into the data port or the control port as long as the duty cycle requirement (TWI) is observed and no previous command is being executed. TWI may be safely violated as long as the extended TPPWW that results is observed. If a previously entered command is being executed, $\overline{PAUSE}$ LOW Pulse Width is the time to complete execution plus the time shown.
9. 150ns for Am9511A-1DM.

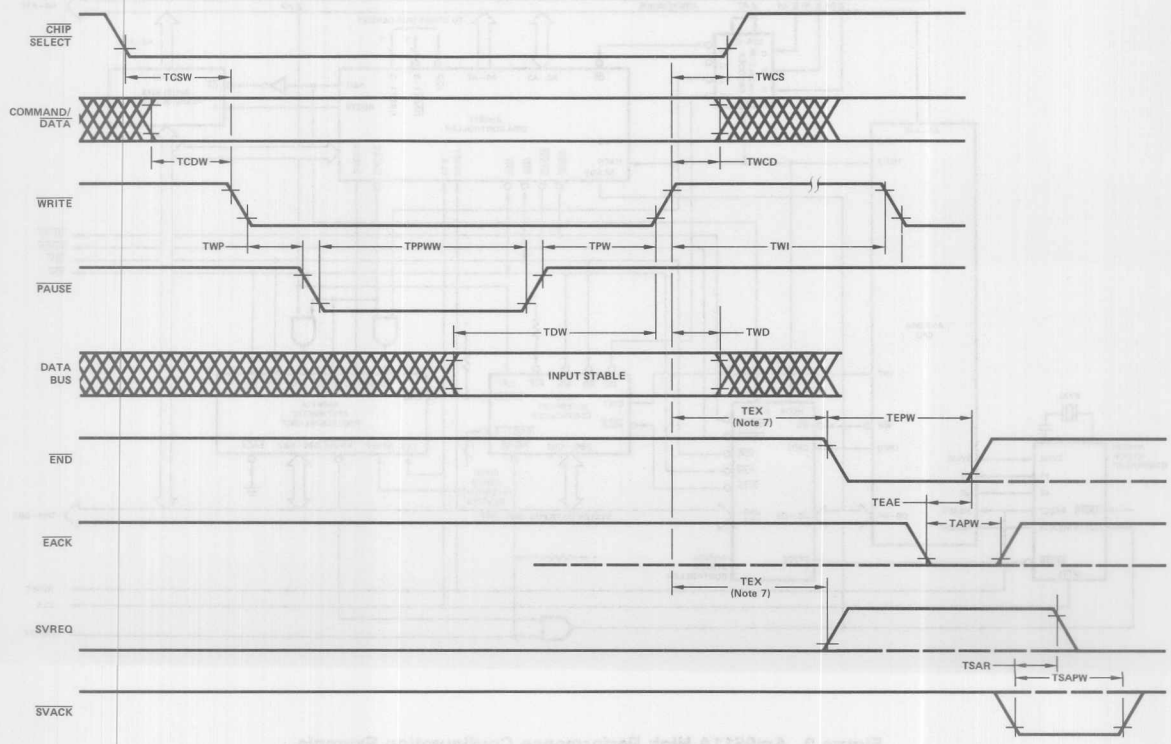
## SWITCHING WAVEFORMS

### READ OPERATIONS




MOS-048

### WRITE OPERATIONS




MOS-049

7

## APPLICATION INFORMATION

The diagram in Figure 2 shows the interface connections for the Am9511A APU with operand transfers handled by an Am9517 DMA controller, and CPU coordination handled by an Am9519 Interrupt Controller. The APU interrupts the CPU to indicate that a command has been completed. When the performance enhancements provided by the DMA and Interrupt operations are not required, the APU interface can be simplified as shown in Figure 1. The Am9511A APU is designed with a general purpose 8-bit data bus and interface control so that it can be conveniently used with any general 8-bit processor.

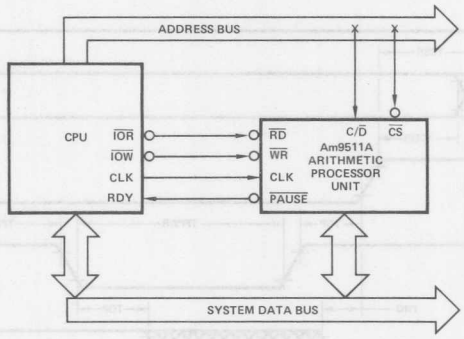



**Figure 1. Am9511A Minimum Configuration Example.**

MOS-050

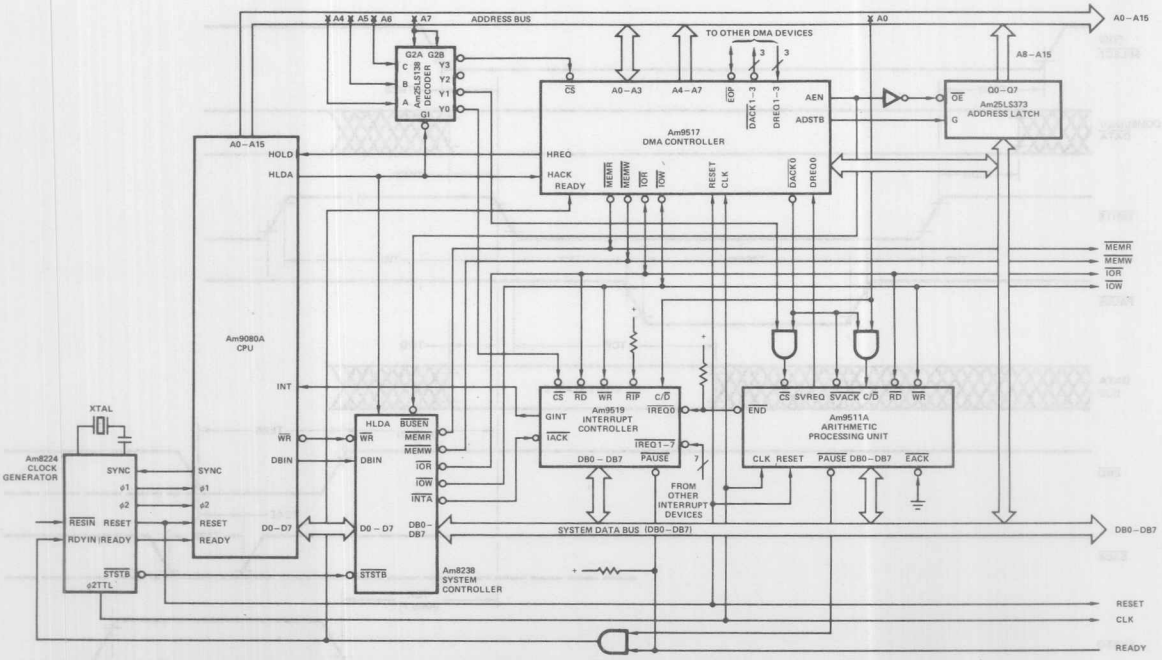



**Figure 2. Am9511A High Performance Configuration Example.**

MOS-051

# Am9512

## Floating-Point Processor

### DISTINCTIVE CHARACTERISTICS

- Single (32-bit) and double (64-bit) precision capability
- Add, subtract, multiply and divide functions
- Compatible with proposed IEEE format
- Easy interfacing to microprocessors
- 8-bit data bus
- Standard 24-pin package
- 12V and 5V power supplies
- Stack oriented operand storage
- Direct memory access or programmed I/O Data Transfers
- End of execution signal
- Error interrupt
- All inputs and outputs TTL level compatible
- Advanced N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

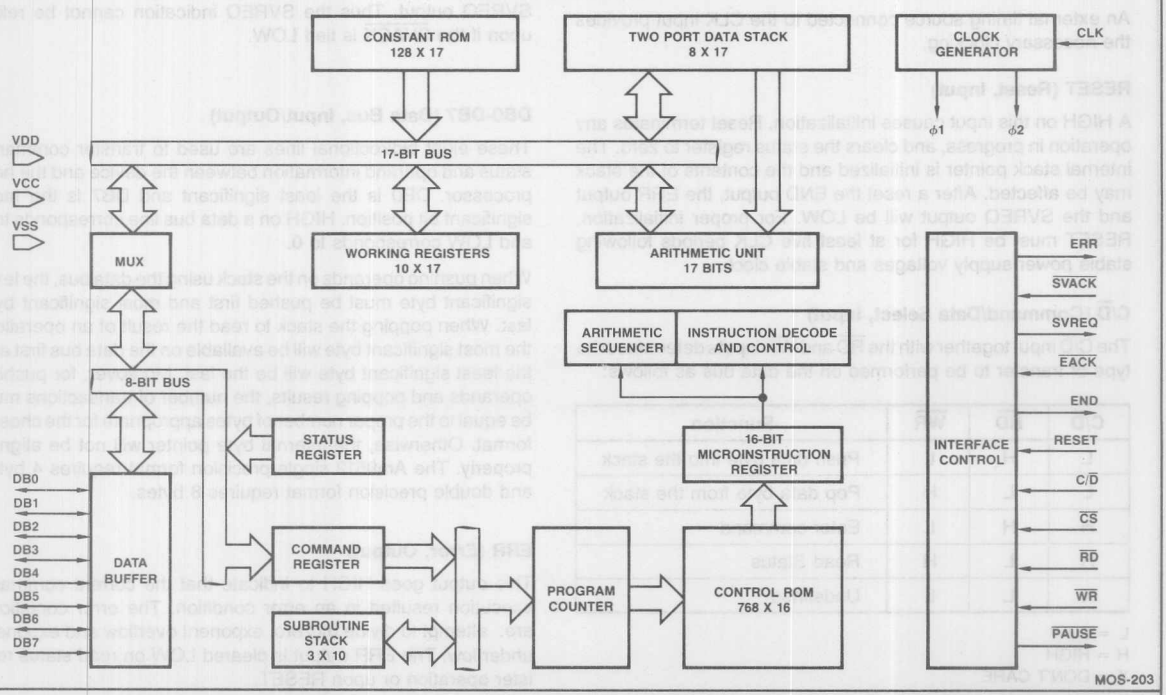
### GENERAL DESCRIPTION

The Am9512 is a high performance floating-point processor unit (FPU). It provides single precision (32-bit) and double precision (64-bit) add, subtract, multiply and divide operations. It can be easily interfaced to enhance the computational capabilities of the host microprocessor.

The operand, result, status and command information transfers take place over an 8-bit bidirectional data bus. Operands are pushed onto an internal stack by the host processor and a command is issued to perform an operation on the data stack. The results of this operation are available to the host processor by popping the stack.

Information transfers between the Am9512 and the host processor can be handled by using programmed I/O or direct memory access techniques. After completing an operation, the Am9512 activates an "end of execution" signal that can be used to interrupt the host processor.

### BLOCK DIAGRAM

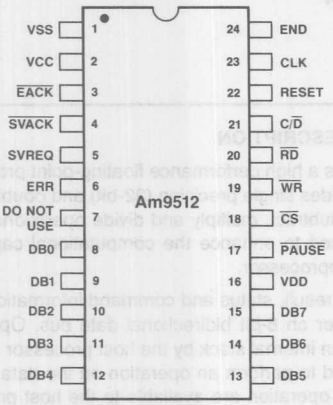



MOS-203

### ORDERING INFORMATION

| Package Type | Ambient Temperature | Maximum Clock Frequency | |
|---|---|---|---|
| | | 2MHz | 3MHz |
| Hermetic DIP | $0°C \leq T_A \leq 70°C$ | AM9512DC | AM9512-1DC |
| | $-55°C \leq T_A \leq +125°C$ | AM9512DM | AM9512-1DM |

**CONNECTION DIAGRAM**
**Top View**




Note: Pin 1 is marked for orientation.

MOS-204

## INTERFACE SIGNAL DESCRIPTION

**VCC:** +5V Power Supply

**VDD:** +12V Power Supply

**VSS:** Ground

### CLK (Clock, Input)

An external timing source connected to the CLK input provides the necessary clocking.

### RESET (Reset, Input)

A HIGH on this input causes initialization. Reset terminates any operation in progress, and clears the status register to zero. The internal stack pointer is initialized and the contents of the stack may be affected. After a reset the END output, the ERR output and the SVREQ output will be LOW. For proper initialization, RESET must be HIGH for at least five CLK periods following stable power supply voltages and stable clock.

### C/$\overline{D}$ (Command/Data Select, Input)

The C/$\overline{D}$ input together with the $\overline{RD}$ and $\overline{WR}$ inputs determines the type of transfer to be performed on the data bus as follows:

| C/$\overline{D}$ | $\overline{RD}$ | $\overline{WR}$ | Function |
|---|---|---|---|
| L | H | L | Push data byte into the stack |
| L | L | H | Pop data byte from the stack |
| H | H | L | Enter command |
| H | L | H | Read Status |
| X | L | L | Undefined |

L = LOW
H = HIGH
X = DON'T CARE

### END (End of Execution, Output)

A HIGH on this output indicates that execution of the current command is complete. This output will be cleared LOW by activating the $\overline{EACK}$ input LOW or performing any read or write operation or device initialization using the RESET. If $\overline{EACK}$ is tied LOW, the END output will be a pulse (see $\overline{EACK}$ description).

Reading the status register while a command execution is in progress is allowed. However any read or write operation clears the flip-flop that generates the END output. Thus such continuous reading could conflict with internal logic setting of the END flip-flop at the end of command execution.

### $\overline{EACK}$ (End Acknowledge, Input)

This input when LOW makes the END output go LOW. As mentioned earlier HIGH on the END output signals completion of a command execution. The END signal is derived from an internal flip-flop which is clocked at the completion of a command. This flip-flop is clocked to the reset state when $\overline{EACK}$ is LOW. Consequently, if $\overline{EACK}$ is tied LOW, the END output will be a pulse that is approximately one CLK period wide.

### SVREQ (Service Request, Output)

A HIGH on this output indicates completion of a command. In this sense this output is the same as the END output. However, the SVREQ output will go HIGH at the completion of a command. This bit must be 1 for SVREQ to go HIGH. The SVREQ can be cleared (i.e., go LOW) by activating the $\overline{SVACK}$ input LOW or initializing the device using the RESET. Also, the SVREQ will be automatically cleared after completion of any command that has the service request bit as 0.

### $\overline{SVACK}$ (Service Acknowledge, Input)

A LOW on this input clears SVREQ. If the $\overline{SVACK}$ input is permanently tied LOW, it will conflict with the internal setting of the SVREQ output. Thus the SVREQ indication cannot be relied upon if the $\overline{SVACK}$ is tied LOW.

### DB0-DB7 (Data Bus, Input/Output)

These eight bidirectional lines are used to transfer command, status and operand information between the device and the host processor. DB0 is the least significant and DB7 is the most significant bit position. HIGH on a data bus line corresponds to 1 and LOW corresponds to 0.

When pushing operands on the stack using the data bus, the least significant byte must be pushed first and most significant byte last. When popping the stack to read the result of an operation, the most significant byte will be available on the data bus first and the least significant byte will be the last. Moreover, for pushing operands and popping results, the number of transactions must be equal to the proper number of bytes appropriate for the chosen format. Otherwise, the internal byte pointer will not be aligned properly. The Am9512 single precision format requires 4 bytes and double precision format requires 8 bytes.

### ERR (Error, Output)

This output goes HIGH to indicate that the current command execution resulted in an error condition. The error conditions are: attempt to divide by zero, exponent overflow and exponent underflow. The ERR output is cleared LOW on read status register operation or upon RESET.

The ERR output is derived from the error bits in the status register. These error bits will be updated internally at an appropriate time during a command execution. Thus ERR output going HIGH may not correspond with the completion of a command. Reading of the status register can be performed while a command execution is in progress. However it should be noted that reading the status register clears the ERR output. Thus reading the status register while a command execution in progress may result in an internal conflict with the ERR output.

**$\overline{CS}$ (Chip Select, Input)**

This input must be LOW to accomplish any read or write operation to the Am9512.

To perform a write operation, appropriate data is presented on DB0 through DB7 lines, appropriate logic level on the C/$\overline{D}$ input and the $\overline{CS}$ input is made LOW. Whenever $\overline{WR}$ and $\overline{RD}$ inputs are both HIGH and $\overline{CS}$ is LOW, $\overline{PAUSE}$ goes LOW. However actual writing into the Am9512 cannot start until $\overline{WR}$ is made LOW. After initiating the write operation by the HIGH to LOW transition on the $\overline{WR}$ input, the $\overline{PAUSE}$ output will go HIGH indicating the write operation has been acknowledged. The $\overline{WR}$ input can go HIGH after $\overline{PAUSE}$ goes HIGH. The data lines, C/$\overline{D}$ input and the $\overline{CS}$ input can change when appropriate hold time requirements are satisfied. See write timing diagram for details.

To perform a read operation an appropriate logic level is established on the C/$\overline{D}$ input and $\overline{CS}$ is made LOW. The $\overline{PAUSE}$ output goes LOW because $\overline{WR}$ and $\overline{RD}$ inputs are HIGH. The read operation does not start until the $\overline{RD}$ input goes LOW. $\overline{PAUSE}$ will go HIGH indicating that read operation is complete and the required information is available on the DB0 through DB7 lines. This information will remain on the data lines as long as $\overline{RD}$ is LOW. The $\overline{RD}$ input can return HIGH anytime after $\overline{PAUSE}$ goes HIGH. The $\overline{CS}$ input and C/$\overline{D}$ input can change anytime after $\overline{RD}$ returns HIGH. See read timing diagram for details. If the $\overline{CS}$ is tied LOW permanently, $\overline{PAUSE}$ will remain LOW until the next Am9512 read or write access.

**$\overline{RD}$ (Read, Input)**

A LOW on this input is used to read information from an internal location and gate that information onto the data bus. The $\overline{CS}$ input must be LOW to accomplish the read operation. The C/$\overline{D}$ input determines what internal location is of interest. See C/$\overline{D}$, $\overline{CS}$ input descriptions and read timing diagram for details. If the END output was HIGH, performing any read operation will make the END output go LOW after the HIGH to LOW transition of the $\overline{RD}$ input (assuming $\overline{CS}$ is LOW). If the ERR output was HIGH performing a status register read operation will make the ERR output LOW. This will happen after the HIGH to LOW transition of the RD input (assuming $\overline{CS}$ is LOW).

**$\overline{WR}$ (Write, Input)**

A LOW on this input is used to transfer information from the data bus into an internal location. The $\overline{CS}$ must be LOW to accomplish the write operation. The C/$\overline{D}$ determines which internal location is to be written. See C/$\overline{D}$, $\overline{CS}$ input descriptions and write timing diagram for details.

If the END output was HIGH, performing any write operation will make the END output go LOW after the LOW to HIGH transition of the $\overline{WR}$ input (assuming $\overline{CS}$ is LOW).

**$\overline{PAUSE}$ (Pause, Output)**

This output is a handshake signal used while performing read or write transactions with the Am9512. If the $\overline{WR}$ and $\overline{RD}$ inputs are both HIGH, the $\overline{PAUSE}$ output goes LOW with the $\overline{CS}$ input in anticipation of a transaction. If $\overline{WR}$ goes LOW to initiate a write transaction with proper signals established on the DB0-DB7, C/$\overline{D}$ inputs, the $\overline{PAUSE}$ will return HIGH indicating that the write operation has been accomplished. The $\overline{WR}$ can be made HIGH after this event. On the other hand, if a read operation is desired, the $\overline{RD}$ input is made LOW after activating $\overline{CS}$ LOW and establishing proper C/$\overline{D}$ input. (The $\overline{PAUSE}$ will go LOW in response to $\overline{CS}$ going LOW.) The $\overline{PAUSE}$ will return HIGH indicating completion of read. The $\overline{RD}$ can return HIGH after this event. It should be noted that a read or write operation can be initiated without any regard to whether a command execution is in progress or not. Proper device operation is assured by obeying the $\overline{PAUSE}$ output indication as described.

## FUNCTIONAL DESCRIPTION

Major functional units of the Am9512 are shown in the block diagram. The Am9512 employs a microprogram controlled stack oriented architecture with 17-bit wide data paths.

The Arithmetic Unit receives one of its operands from the Operand Stack. This stack is an eight word by 17-bit two port memory with last in – first out (LIFO) attributes. The second operand to the Arithmetic Unit is supplied by the internal 17-bit bus. In addition to supplying the second operand, this bidirectional bus also carries the results from the output of the Arithmetic Unit when required. Writing into the Operand Stack takes place from this internal 17-bit bus when required. Also connected to this bus are the Constant ROM and Working Registers. The ROM provides the required constants to perform the mathematical operations while the Working Registers provide storage for the intermediate values during command execution.

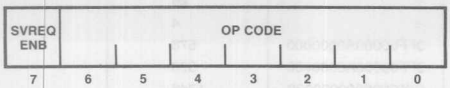
Communication between the external world and the Am9512 takes place on eight bidirectional input/output lines, DB0 through DB7 (Data Bus). These signals are gated to the internal 8-bit bus through appropriate interface and buffer circuitry. Multiplexing facilities exist for bidirectional communication between the internal eight and 17-bit buses. The Status Register and Command Register are also located on the 8-bit bus.

The Am9512 operations are controlled by the microprogram contained in the Control ROM. The Program Counter supplies the microprogram addresses and can be partially loaded from the Command Register. Associated with the Program Counter is the Subroutine Stack where return addresses are held during subroutine calls in the microprogram. The Microinstruction Register holds the current microinstruction being executed. The register facilitates pipelined microprogram execution. The Instruction Decode logic generates various internal control signals needed for the Am9512 operation.

The Interface Control logic receives several external inputs and provides handshake related outputs to facilitate interfacing the Am9512 to microprocessors.

## COMMAND FORMAT

The Operation of the Am9512 is controlled from the host processor by issuing instructions called commands. The command format is shown below:




The command consists of 8 bits; the least significant 7 bits specify the operation to be performed as detailed in the accompanying table. The most significant bit is the Service Request Enable bit. This bit must be a 1 if SVREQ is to go high at end of executing a command.

The Am9512 commands fall into three categories: Single precision arithmetic, double precision arithmetic and data manipulation. There are four arithmetic operations that can be performed with single precision (32-bit), or double precision (64-bit) floating-point numbers: add, subtract, multiply and divide. These operations require two operands. The Am9512 assumes that these operands are located in the internal stack as Top of Stack

(TOS) and Next on Stack (NOS). The result will always be returned to the previous NOS which becomes the new TOS. Results from an operation are of the same precision and format as the operands. The results will be rounded to preserve the accuracy. The actual data formats and rounding procedures are described in a later section. In addition to the arithmetic operations, the Am9512 implements eight data manipulating operations. These include changing the sign of a double or single precision operand located in TOS, exchanging single precision operands located at TOS and NOS, as well as copying and popping single or double precision operands. See also the sections on status register and operand formats.

The Execution times of the Am9512 commands are all data dependent. Table 2 shows one example of each command execution time:

**Table 1. Command Decoding Table.**

| Command Bits | | | | | | | | Mnemonic | Description |
|---|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| X | 0 | 0 | 0 | 0 | 0 | 0 | 1 | SADD | Add TOS to NOS Single Precision and result to NOS. Pop stack. |
| X | 0 | 0 | 0 | 0 | 0 | 1 | 0 | SSUB | Subtract TOS from NOS Single Precision and result to NOS. Pop stack. |
| X | 0 | 0 | 0 | 0 | 0 | 1 | 1 | SMUL | Multiply NOS by TOS Single Precision and result to NOS. Pop stack. |
| X | 0 | 0 | 0 | 0 | 1 | 0 | 0 | SDIV | Divide NOS by TOS Single Precision and result to NOS. Pop stack. |
| X | 0 | 0 | 0 | 0 | 1 | 0 | 1 | CHSS | Change sign of TOS Single Precision operand. |
| X | 0 | 0 | 0 | 0 | 1 | 1 | 0 | PTOS | Push Single Precision operand on TOS to NOS. |
| X | 0 | 0 | 0 | 0 | 1 | 1 | 1 | POPS | Pop Single Precision operand from TOS. NOS becomes TOS. |
| X | 0 | 0 | 0 | 1 | 0 | 0 | 0 | XCHS | Exchange TOS with NOS Single Precision. |
| X | 0 | 1 | 0 | 1 | 1 | 0 | 1 | CHSD | Change sign of TOS Double Precision operand. |
| X | 0 | 1 | 0 | 1 | 1 | 1 | 0 | PTOD | Push Double Precision operand on TOS to NOS. |
| X | 0 | 1 | 0 | 1 | 1 | 1 | 1 | POPD | Pop Double Precision operand from TOS. NOS becomes TOS. |
| X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CLR | CLR status. |
| X | 0 | 1 | 0 | 1 | 0 | 0 | 1 | DADD | Add TOS to NOS Double Precision and result to NOS. Pop stack. |
| X | 0 | 1 | 0 | 1 | 0 | 1 | 0 | DSUB | Subtract TOS from NOS Double Precision and result to NOS. Pop stack. |
| X | 0 | 1 | 0 | 1 | 0 | 1 | 1 | DMUL | Multiply NOS by TOS Double Precision and result to NOS. Pop stack. |
| X | 0 | 1 | 0 | 1 | 1 | 0 | 0 | DDIV | Divide NOS by TOS Double Precision and result to NOS. Pop Stack. |

Notes: X = Don't Care  Operation for bit combinations not listed above is undefined.

**Table 2. Am9512 Execution Time in Cycles.**

| | Single Precision | | | Double Precision | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| Add | 58 | 220 | 512 | 578 | 1200 | 3100 |
| Subtract | 56 | 220 | 512 | 578 | 1200 | 3100 |
| Multiply | 192 | 220 | 254 | 1720 | 1770 | 1860 |
| Divide | 228 | 240 | 264 | 4560 | 4920 | 5120 |

Note: Typical for add and subtract, assumes the operands are within six decimal orders of magnitude. Max is derived from the maximum execution time of 1000 executions with random 32-bit or 64-bit patterns.

**Table 3. Some Execution Examples.**

| Command | TOS | NOS | Result | Clock periods |
|---|---|---|---|---|
| SADD | 3F800000 | 3F800000 | 40000000 | 58 |
| SSUB | 3F800000 | 3F800000 | 00000000 | 56 |
| SMUL | 40400000 | 3FC00000 | 40900000 | 198 |
| SDIV | 40000000 | 3F800000 | 3F000000 | 228 |
| CHSS | 3F800000 | – | BF800000 | 10 |
| PTOS | 3F800000 | – | – | 16 |
| POPS | 3F800000 | – | – | 14 |
| XCHS | 3F800000 | 4000000 | – | 26 |
| CHSD | 3FF0000000000000 | – | BFF0000000000000 | 24 |
| PTOD | 3FF0000000000000 | – | – | 40 |
| POPD | 3FF0000000000000 | – | – | 26 |
| CLR | 3FF0000000000000 | – | – | 4 |
| DADD | 3FF00000A0000000 | 8000000000000000 | 3FF00000A0000000 | 578 |
| DSUB | 3FF00000A0000000 | 8000000000000000 | 3FF00000A0000000 | 578 |
| DMUL | BFF8000000000000 | 3FF8000000000000 | C002000000000000 | 1748 |
| DDIV | BFF8000000000000 | 3FF8000000000000 | BFF0000000000000 | 4560 |

Note: TOS, NOS and Result are in hexadecimal; Clock period is in decimal.

## COMMAND INITIATION

After properly positioning the required operands in the stack, a command may be issued. The procedure for initiating a command execution is as follows:

1. Establish appropriate command on the DB0-DB7 lines.
2. Establish HIGH on the C/$\overline{D}$ input.
3. Establish LOW on the $\overline{CS}$ input. Whenever $\overline{WR}$ and $\overline{RD}$ inputs are HIGH the $\overline{PAUSE}$ output follows the $\overline{CS}$ input. Hence $\overline{PAUSE}$ will become LOW.
4. Establish LOW on the $\overline{WR}$ input after an appropriate set up time (see timing diagrams).
5. Sometime after the HIGH to LOW level transition of $\overline{WR}$ input, the $\overline{PAUSE}$ output will become HIGH to acknowledge the write operation. The $\overline{WR}$ input can return to HIGH anytime after $\overline{PAUSE}$ goes HIGH. The DB0-DB7, C/$\overline{D}$ and $\overline{CS}$ inputs are allowed to change after the hold time requirements are satisfied (see timing diagram).

An attempt to issue a new command while the current command execution is in progress is allowed. Under these circumstances, the $\overline{PAUSE}$ output will not go HIGH until the current command execution is completed.

## OPERAND ENTRY

The Am9512 commands operate on the operands located at the TOS and NOS and results are returned to the stack at NOS and then popped to TOS. The operands required for the Am9512 are one of two formats – single precision floating-point (4 bytes) or double precision floating-point (8 bytes). The result of an operation has the same format as the operands. In other words, operations using single precision quantities always result in a single precision result while operations involving double precision quantities will result in double precision result.

Operands are always entered into the stack least significant byte first and most significant byte last. The following procedure must be followed to enter operands into the stack:

1. The lower significant operand byte is established on the DB0-DB7 lines.
2. A LOW is established on the C/$\overline{D}$ input to specify that data is to be entered into the stack.
3. The $\overline{CS}$ input is made LOW. Whenever the $\overline{WR}$ and $\overline{RD}$ inputs are HIGH, the $\overline{PAUSE}$ output will follow the $\overline{CS}$ input. Thus $\overline{PAUSE}$ output will become LOW.
4. After appropriate set up time (see timing diagrams), the $\overline{WR}$ input is made LOW.
5. Sometime after this event, $\overline{PAUSE}$ will return HIGH to indicate that the write operation has been acknowledged.
6. Anytime after the $\overline{PAUSE}$ output goes HIGH the $\overline{WR}$ input can be made HIGH. The DB0-DB7, C/$\overline{D}$ and $\overline{CS}$ inputs can change after appropriate hold time requirements are satisfied (see timing diagrams).

The above procedure must be repeated until all bytes of the operand are pushed into the stack. It should be noted that for single precision operands 4 bytes should be pushed and 8 bytes must be pushed for double precision. Not pushing all the bytes of a quantity will result in byte pointer misalignment.

The Am9512 stack can accommodate 4 single precision quantities or 2 double precision quantities. Pushing more quantities than the capacity of the stack will result in loss of data which is usual with any LIFO stack.

## REMOVING THE RESULTS

Result from an operation will be available at the TOS. Results can be transferred from the stack to the data bus by reading the stack.

When the stack is popped for results, the most significant byte is available first and the least significant byte last. A result is always of the same precision as the operands that produced it. Thus when the result is taken from the stack, the total number of bytes popped out should be appropriate with the precision – single precision results are 4 bytes and double precision results are 8 bytes. The following prodedure must be used for reading the result from the stack:

1. A LOW is established on the C/$\overline{D}$ input.
2. The $\overline{CS}$ input is made LOW. When $\overline{WR}$ and $\overline{RD}$ inputs are both HIGH, the $\overline{PAUSE}$ output follows the $\overline{CS}$ input, thus $\overline{PAUSE}$ will be LOW.
3. After appropriate set up time (see timing diagrams), the $\overline{RD}$ input is made LOW.
4. Sometime after this, $\overline{PAUSE}$ will return HIGH indicating that the data is available on the DB0-DB7 lines. This data will remain on the DB0-DB7 lines as long as the $\overline{RD}$ input remains LOW.
5. Anytime after $\overline{PAUSE}$ goes HIGH, the $\overline{RD}$ input can return HIGH to complete transaction.
6. The $\overline{CS}$ and C/$\overline{D}$ inputs can change after appropriate hold time requirements are satisfied (see timing diagram).
7. Repeat this procedure until all bytes appropriate for the precision of the result are popped out.

Reading of the stack does not alter its data; it only adjusts the byte pointer. If more data is popped than the capacity of the stack, the internal byte pointer will wrap around and older data will be read again, consistent with the LIFO stack.

## READING STATUS REGISTER

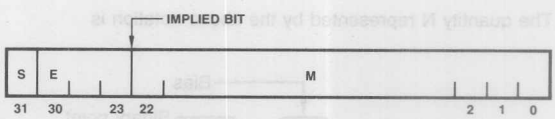
The Am9512 status register can be read without any regard to whether a command is in progress or not. The only implication that has to be considered is the effect this might have on the END and ERR outputs discussed in the signal descriptions.

The following procedure must be followed to accomplish status register reading.

1. Establish HIGH on the C/$\overline{D}$ input.
2. Establish LOW on the $\overline{CS}$ input. Whenever $\overline{WR}$ and $\overline{RD}$ inputs are HIGH, $\overline{PAUSE}$ will follow the $\overline{CS}$ input. Thus, $\overline{PAUSE}$ will go LOW.
3. After appropriate set up time (see timing diagram) $\overline{RD}$ is made LOW.
4. Sometime after the HIGH to LOW transition of $\overline{RD}$, $\overline{PAUSE}$ will become HIGH indicating that status register contents are available on the DB0-DB7 lines. These lines will contain this information as long as $\overline{RD}$ is LOW.
5. The $\overline{RD}$ input can be returned HIGH anytime after $\overline{PAUSE}$ goes HIGH.
6. The C/$\overline{D}$ input and $\overline{CS}$ input can change after satisfying appropriate hold time requirements (see timing diagram).

## DATA FORMATS

The Am9512 handles floating-point quantities in two different formats – single precision and double precision. The single precision quantities are 32-bits long as shown below.



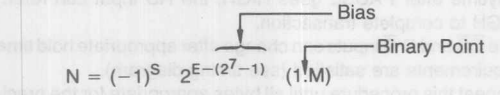

**Bit 31:**

S = Sign of the mantissa. 1 represents negative and 0 represents positive.

**Bits 0-22**

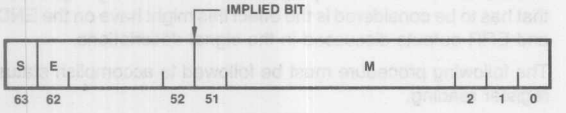
M = 23-bit mantissa. Together with the sign bit, the mantissa represents a signed fraction in sign-magitude notation. There is an implied 1 beyond the most significant bit (bit 22) of the mantissa. In other words, the mantissa is assumed to be a 24-bit normalized quantity and the most significant bit which will always be 1 due to normalization is implied. The Am9512 restores this implied bit internally before performing arithmetic; normalizes the result and strips the implied bit before returning the results to the external data bus. The binary point is between the implied bit and bit 22 of the mantissa.

The quantity N represented by the above notation is




Provided E ≠ 0 or all 1's.

A double precision quantity consists of the mantissa sign bit(s), an 11 bit biased exponent (E), and a 52-bit mantissa (M). The bias for double precision quantities is $2^{10} - 1$. The double precision format is illustrated below.




**Bit 63:**

S = Sign of the mantissa. 1 represents negative and 0 represents positive.

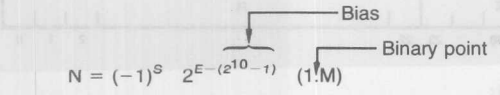
**Bits 52-62**

E = These 11 bits represent a biased exponent. The bias is $2^{10} - 1 = 1023$.

**Bit 0-51**

M = 52-bit mantissa. Together with the sign bit, the mantissa represents a signed fraction in sign-magnitude notation. There is an implied 1 beyond the most significant bit (bit 51) of the mantissa. In other words, the mantissa is assumed to a 53-bit normalized quantity and the most significant bit, which will always be a 1 due to normalization, is implied. The Am9512 restores this implied bit internally before performing arithmetic; normalizes the result and strips the implied bit before returning the result to the external data bus. The binary point is between the implied bit and bit 51 of the mantissa.

The quantity N represented by the above notation is




Provided E ≠ 0 or all 1's.

| BUSY | SIGN S | ZERO Z | RESERVED | DIVIDE EXCEPTION D | EXPONENT UNDERFLOW U | EXPONENT OVERFLOW V | RESERVED |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Bit 0 and bit 4 are reserved. Occurrence of exponent oerflow (V), exponent underflow (U) and divide exception (D) are indicated by bits 1, 2 and 3 respectively. An attempt to divide by zero is the only divide exception. Bits 5 and 6 represent a zero result and the sign of a result respectively. Bit 7 (Busy) of the status register indicates if the Am9512 is currently busy executing a command. All the bits are initialized to zero upon reset. Also, executing a CLR (Clear Status) command will result in all zero status register bits. A zero in Bit 7 indicates that the Am9512 is not busy and a new command may be initiated. As soon as a new command is issued, Bit 7 becomes 1 to indicate the device is busy and remains 1 until the command execution is complete, at which time it will become 0. As soon as a new command is issued, status register bits 0, 1, 2, 3, 4, 5 and 6 are cleared to zero. The status bits will be set as required during the command execution. Hence, as long as bit 7 is 1, the remainder of the status register bit indications should not be relied upon unless the ERR occurs. The following is a detailed status bit description.

Bit 0 Reserved

Bit 1 Exponent overflow (V): When 1, this bit indicates that exponent overflow has occurred. Cleared to zero otherwise.

Bit 2 Exponent Underflow (U): When 1, this bit indicates that exponent underflow has occurred. Cleared to zero otherwise.

Bit 3 Divide Exception (D): When 1, this bit indicates that an attempt to divide by zero is made. Cleared to zero otherwise.

Bit 4 Reserved

Bit 5 Zero (Z): When 1, this bit indicates that the result returned to TOS after a command is all zeros. Cleared to zero otherwise.

Bit 6 Sign (S): When 1, this bit indicates that the result returned to TOS is negative. Cleared to zero otherwise.

Bit 7 Busy: When 1, this bit indicates the Am9512 is in the process of executing a command. It will become zero after the command execution is complete.

All other status register bits are valid when the Busy bit is zero.

## ALGORITHMS OF FLOATING-POINT ARITHMETIC

1. Floating Point to Decimal Conversion

   As an introduction to floating-point arithmetic, a brief description of the Decimal equivalent of the Am9512 floating-point format should help the reader to understand and verify the validity of the arithmetic operations. The Am9512 single precision format is used for the following discussions. With a minor modification of the field lengths, the discussion would also apply to the double precision format.

   There are three parts in a floating point number:

   a. The sign – the sign applies to the sign of the number. Zero means the number is positive or zero. One means the number is negative.

b. The exponent – the exponent represents the magnitude of the number. The Am9512 single precision format has an excess $127_{10}$ notation which means the code representation is $127_{10}$ higher than the actual value. The following are a few examples of actual versus coded exponent.

| Actual | Coded |
|---|---|
| $+127_{10}$ | $+254_{10}$ |
| 0 | $127_{10}$ |
| $-126_{10}$ | $+1_{10}$ |

c. The mantissa – the mantissa is a 23-bit value with the binary point to the left of the most significant bit. There is a hidden 1 to the left of the binary point so the mantissa is always less than 2 and greater than or equal to 1.

To find the Decimal equivalent of the floating point number, the mantissa is multiplied by 2 to the power of the actual exponent. The number is negated if the sign bit = 1. The following are two examples of conversion:

Example 1

Floating Point No. = 0 10000011 11000000000000000000000B

Sign — Exponent — Mantissa

Coded Exponent = 10000011B
Actual Exponent = 10000011B – 01111111B = 00000100B = $4_{10}$
Mantissa = 1.1100000000000000000000B
= 1 + 1/2 + 1/4 = $1.75_{10}$
Decimal No. = $2^4$ x 1.75 = 16 x 1.75 = $28_{10}$

Example 2

Floating Point No. = 1 01111010 01100000000000000000000B

Sign — Exponent — Mantissa

Code Exponent = 01111010B
Actual Exponent = 01111010B – 01111111B = 11111011B = $-5_{10}$
Mantissa = 1.0110000000000000000000B
= 1 + 1/4 + 1/8 = $1.375_{10}$
Decimal No. = $-2^{-5}$ x 1.375 = $-.04296875_{10}$

2. Unpacking of the Floating-Point Numbers

The Am9512 unpacks the floating point number into three parts before any of the arithmetic operation. The number is divided into three parts as described in Section 1. The sign and exponent are copied from the original number as 1 and 8-bit numbers respectively. The mantissa is stored as a 24-bit number. The least significant 23 bits are copied from the original number and the MSB is set to 1. The binary point is assumed to the right of the MSB.

The abbreviations listed below are used in the following sections of algorithm description:

SIGN – Sign of Result
EXP – Exponent of Result
MAN – Mantissa of Result
SIGN (TOS) – Sign of Top of Stack
EXP (TOS) – Exponent of Top of Stack
MAN (TOS) – Mantissa of Top of Stack
SIGN (NOS) – Sign of Next on Stack
EXP (NOS) – Exponent of Next on Stack
MAN (NOS) – Mantissa of Next on Stack

3. Floating-Point Add/Subtract

The floating-point add and subtract essentially use the same algorithm. The only difference is that floating-point subtract changes the sign of the floating-point number at top of stack and then performs the floating-point add.

The following is a step by step description of a floating-point add algorithm (Figure 1):

a. Unpack TOS and NOS.
b. The exponent of TOS is compared to the exponent of NOS.
c. If the exponents are equal, go to step f.
d. Right shift the mantissa of the number with the smaller exponent.
e. Increment the smaller exponent and go to step b.
f. Set sign of result to sign of larger number.
g. Set exponent of result to exponent of larger number.
h. If sign of the two numbers are not equal, go to m.
i. Add Mantissas.
j. Right shift resultant mantissa by 1 and increment exponent of result by 1.
k. If MSB of exponent changes from 1 to 0 as a result of the increment, set overflow status.
l. Round if necessary and exit.
m. Subtract smaller mantissa from larger mantissa.
n. Left shift mantissa and decrement exponent of result.
o. If MSB of exponent changes from 0 to 1 as a result of the decrement, set underflow status and exit.
p. If the MSB of the resultant mantissa = 0, go to n.
q. Round if necessary and exit.

4. Floating-Point Multiply

Floating-point multiply basically involves the addition of the exponents and multiplication of the mantissas. The following is a step by step description of a floating multiplication algorithm (Figure 2):

a. Check if TOS or NOS = 0.
b. If either TOS or NOS = 0, Set result to 0 and exit.
c. Unpack TOS and NOS.
d. Convert EXP (TOS) and EXP (NOS) to unbiased form.
EXP (TOS) = EXP (TOS) $-127_{10}$
EXP (NOS) = EXP (NOS) $-127_{10}$
e. Add exponents.
EXP = EXP (TOS) + EXP (NOS)
f. If MSB of EXP (TOS) = MSB of EXP (NOS) = 0 and MSB of EXP = 1, then set overflow status and exit.
g. If MSB of EXP (TOS) = MSB of EXP (NOS) = 1 and MSB of EXP = 0, then set underflow status and exit.
h. Convert Exponent back to biased form.
EXP = EXP + $127_{10}$
i. If sign of TOS = sign of NOS, set sign of result to 0, else set sign of result to 1.
j. Multiply mantissa.
k. If MSB of resultant = 1, right shift mantissa by 1 and increment exponent of resultant.
l. If MSB of exponent changes from 1 to 0 as a result of the increment, set overflow status.
m. Round if necessary and exit.

5. Floating-Point Divide

The floating-point divide basically involves the subtraction of exponents and the division of mantissas. The following is a step by step description of a division algorithm (Figure 3).

a. If TOS = 0, set divide exception error and exit.
b. If NOS = 0, set result to 0 and exit.
c. Unpack TOS and NOS.
d. Convert EXP (TOS) and EXP (NOS) to unbiased form.
EXP (TOS) = EXP (TOS) – $127_{10}$
EXP (NOS) = EXP (NOS) – $127_{10}$
e. Subtract exponent of TOS from exponent of NOS.
EXP = EXP (NOS) – EXP (TOS)
f. If MSB of EXP (NOS) = 0, MSB of EXP (TOS) = 1 and MSB of EXP = 1, then set overflow status and exit.
g. If MSB of EXP (NOS) = 1, MSB of EXP (TOS) = 0, and MSB of EXP = 0, then set underflow status and exit.

7

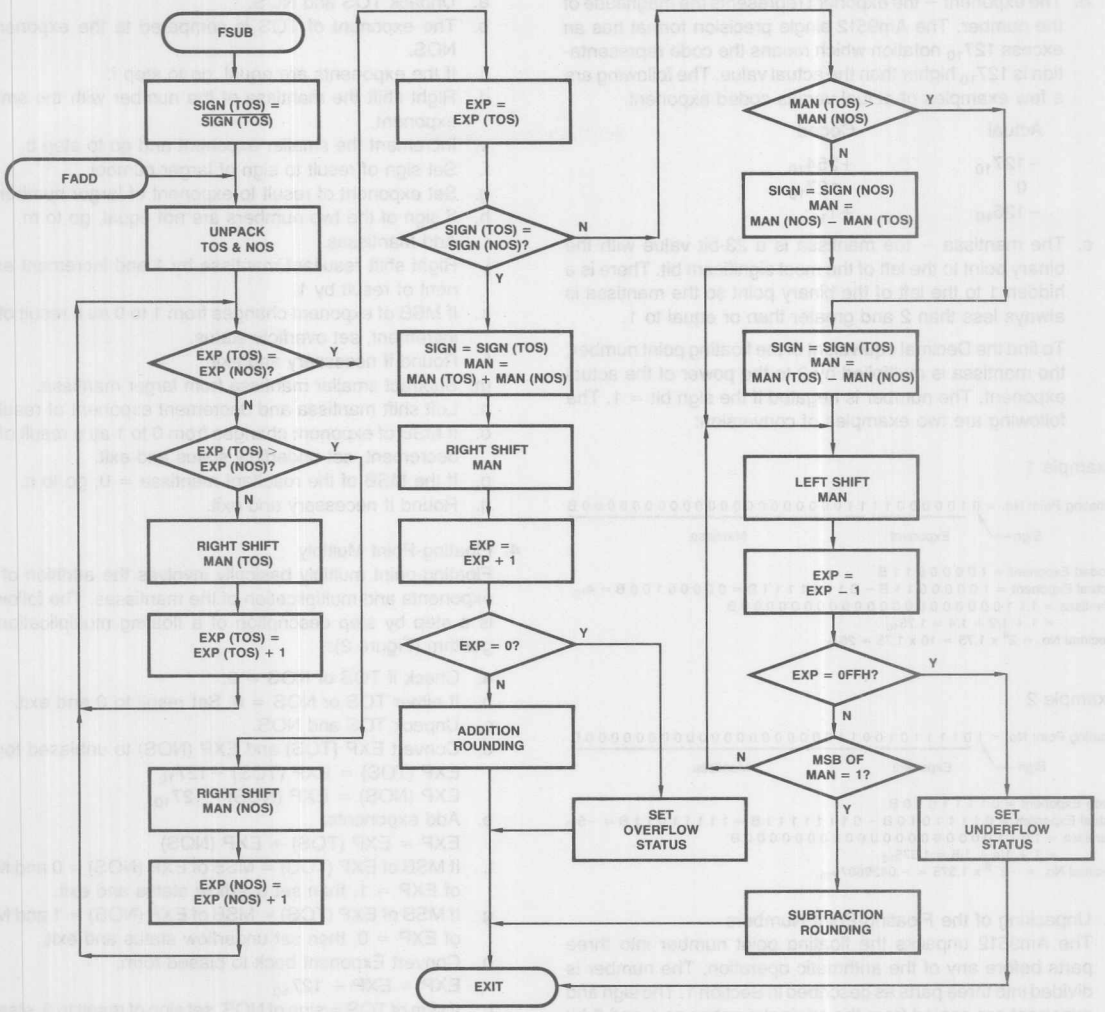



**Figure 1. Conceptual Floating-Point Addition/Subtraction.**

MOS-205

h. Add bias to exponent of result.
   $EXP = EXP + 127_{10}$
i. If sign of TOS = sign of NOS, set sign of result to 0, else set sign of result to 1.
j. Divide mantissa of NOS by mantissa of TOS.
k. If MSB = 0, left shift mantissa and decrement exponent of resultant, else go to n.
l. If MSB of exponent changes from 0 to 1 as a result of the decrement, set underflow status.
m. Go to k.
n. Round if necessary and exit.

The algorithms described above provide the user a means of verifying the validity of the result. They do not necessarily reflect the exact internal sequence of the Am9512.

6. Rounding

The Am9512 adopts a rounding algorithm that is consistent *with the Intel® standard for floating-point arithmetic.* The following description is an excerpt from the paper published in proceedings of Compsac 77, November 1977, pp. 107-112 by Dr. John F. Palmer of Intel Corporation.

The method used for doing the rounding during floating-point arithmetic is known as "Round to Even", i.e., if the resultant number is exactly halfway between two floating point numbers, the number is rounded to the nearest floating-point number whose LSB of the mantissa is 0. In order to simplify the explanation, the algorithms will be illustrated with 4-bit arithmetic. The existence of an accumulator will be assumed as shown:

| OF | B1 | B2 | B3 | B4 | G | R | ST |
|---|---|---|---|---|---|---|---|

The bit labels denote:

OF – The overflow bit
B1-B4 – The 4 mantissa bits
G – The Guard bit
R – The Rounding bit
ST – The "Sticky" bit

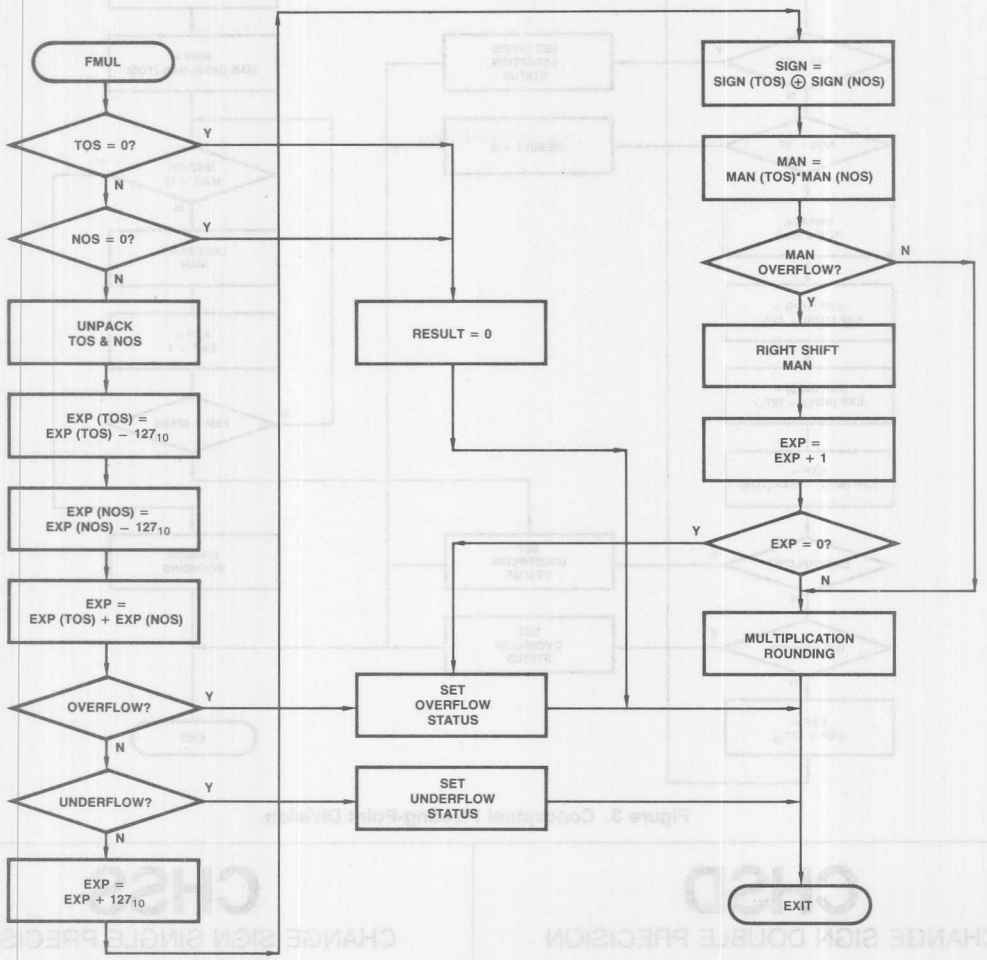



**Figure 2. Conceptual Floating-Point Multiplication.**

MOS-206

The Sticky bit is set to one if any ones are shifted right of the rounding bit in the process of denormalization. If the Sticky bit becomes set, it remains set throughout the operation. All shifting in the Accumulator involves the OF, G, R and ST bits. The ST bit is not affected by left shifts but, zeros are introduced into OF by right shifts.

Rounding during addition of magnitudes – add 1 to the G position, then if G=R=ST=0, set B4 to 0 ("Rounding to Even").

Rounding during subtraction of magnitudes – if more than one left shift was performed, no rounding is needed, otherwise round the same way as addition of magnitudes.

Rounding during multiplication – let the normalized double length product be:

| B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 |
|---|---|---|---|---|---|---|---|

Then G=B5, R=B6, ST=B7 V B8. The rounding is then performed as in addition of magnitudes.

Rounding during division – let the first six bits of the normalized quotient be

| B1 | B2 | B3 | B4 | B5 | B6 |
|---|---|---|---|---|---|

Then G=B5, R=B6, ST=0 if and only if remainder = 0. The rounding is then performed as in addition of magnitudes.

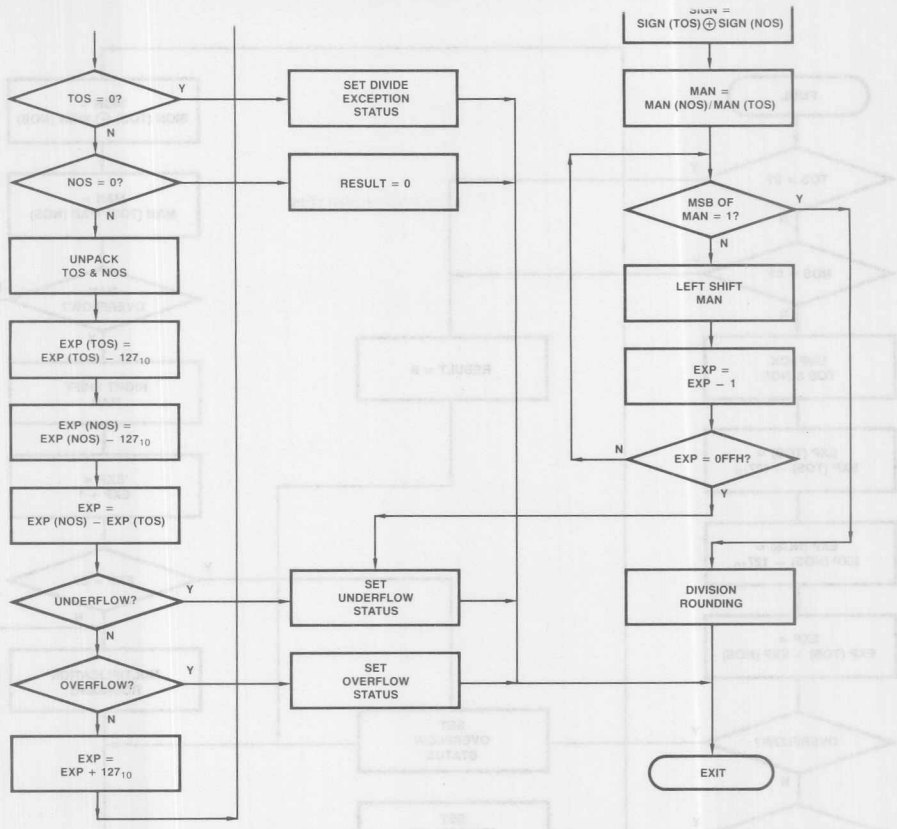



**Figure 3. Conceptual Floating-Point Division.**

MOS-207

# CHSD

## CHANGE SIGN DOUBLE PRECISION

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | SRE | 0 | 1 | 0 | 1 | 1 | 0 | 1 |

**Hex Coding:** AD IF SRE = 1
2D IF SRE = 0

**Execution Time:** See Table 2

**Description:**

The sign of the double precision TOS operand A is complemented. The double precision result R is returned to TOS. If the double precision operand A is zero, then the sign is not affected. The status bit S and Z indicate the sign of the result and if the result is zero. The status bits U, V and D are always cleared to zero.

**Status Affected:** S, Z. (U, V, D always zero.)

**STACK CONTENTS**

| BEFORE | | AFTER |
|---|---|---|
| A | TOS | R |
| B | NOS | B |

# CHSS

## CHANGE SIGN SINGLE PRECISION

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | SRE | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

**Hex Coding:** 85 IF SRE = 1
05 IF SRE = 0

**Execution Time:** See Table 2

**Description:**

The sign of the single precision operand A at TOS is complemented. The single precision result R is returned to TOS. If the exponent field of A is zero, all bits of R will be zeros. The status bits S and Z indicate the sign of the result and if the result is zero. The status bits U, V and D are cleared to zero.

**Status Affected:** S, Z. (U, V, D always zero.)

**STACK CONTENTS**

| BEFORE | | AFTER |
|---|---|---|
| A | ← TOS → | R |
| B | ← NOS → | B |
| C | | C |
| D | | D |

# CLR

## CLEAR STATUS

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | SRE | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Hex Coding:** 80 IF SRE = 1
00 IF SRE = 0

**Execution Time:** 4 clock cycles

**Description:**
The status bits S, Z, D, U, V are cleared to zero. The stack is not affected. This essentially is a no operation command as far as operands are concerned.

**Status Affected:** S, Z, D, U, V always zero.

# DADD

## DOUBLE PRECISION FLOATING-POINT ADD

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | SRE | 0 | 1 | 0 | 1 | 0 | 0 | 1 |

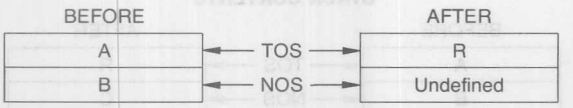
**Hex Coding:** A9 IF SRE = 1
29 IF SRE = 0

**Execution Time:** See Table 2

**Description:**
The double precision operand A from TOS is added to the double precision operand B from NOS. The result is rounded to obtain the final double precision result R which is returned to TOS. The status bits S, Z, U and V are affected to report sign of the result, if the result is zero, exponent underflow and exponent overflow respectively. The status bit D will be cleared to zero.

**Status Affected:** S, Z, U, V. (D always zero.)

**STACK CONTENTS**




# DSUB

## DOUBLE PRECISION FLOATING-POINT SUBTRACT

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | SRE | 0 | 1 | 0 | 1 | 0 | 1 | 0 |

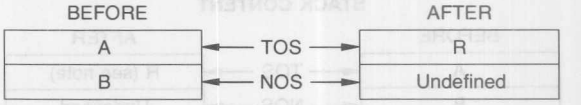
**Hex Coding:** AA IF SRE = 1
2A IF SRE = 0

**Execution Time:** See Table 2

**Description:**
The double precision operand A at TOS is subtracted from the double precision operand B at NOS. The result is rounded to obtain the final double precision result R which is returned to TOS. The status bits S, Z, U and V are affected to report sign of the result, if the result is zero, exponent underflow and exponent overflow respectively. The status bit D will be cleared to zero.

**Status Affected:** S, Z, U, V. (D always zero.)

**STACK CONTENTS**




# DMUL

## DOUBLE PRECISION FLOATING-POINT MULTIPLY

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | SRE | 0 | 1 | 0 | 1 | 0 | 1 | 1 |

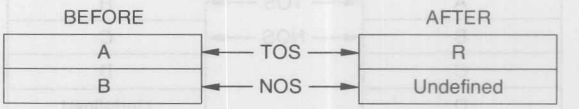
**Hex Coding:** AB IF SRE = 1
2B IF SRE = 0

**Execution Time:** See Table 2

**Description:**
The double precision operand A from TOS is multiplied by the double precision operand B from NOS. The result is rounded to obtain the final double precision result R which is returned to TOS. The status bits S, Z, U and V are affected to report sign of the result, if the result is zero, exponent underflow and exponent overflow respectively. The status bit D will be cleared to zero.

**Status Affected:** S, Z, U, V. (D always zero.)

**STACK CONTENTS**




7

# DDIV

## DOUBLE PRECISION FLOATING-POINT DIVIDE

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Code:** | SRE | 0 | 1 | 0 | 1 | 1 | 0 | 0 |

**Hex Coding:** AC IF SRE = 1
2C IF SRE = 0

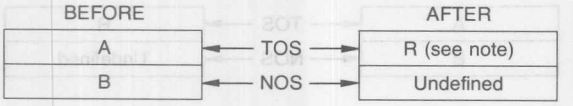
**Execution Time:** See Table 2

**Description:**

The double precision operand B from NOS is divided by the double precision operand A from TOS. The result (quotient) is rounded to obtain the final double precision result R which is returned to TOS. The status bits, S, Z, D, U and V are affected to report sign of the result, if the result is zero, attempt to divide by zero, exponent underflow and exponent overflow respectively.

**Status Affected:** S, Z, D, U, V

**STACK CONTENT**




Note: If A is zero, then R = B (Divide exception).

# SADD

## SINGLE PRECISION FLOATING-POINT ADD

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | SRE | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**Hex Coding:** 81 IF SRE = 1
01 IF SRE = 0

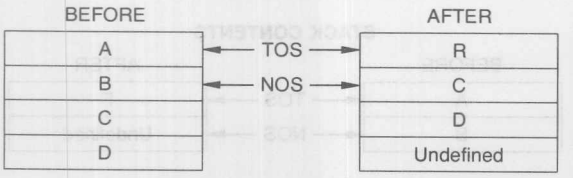
**Execution Time:** See Table 2

**Description:**

The single precision operand A from TOS is added to the single precision operand B from NOS. The result is rounded to obtain the final single precision result R which is returned to TOS. The status bits S, Z, U and V are affected to report the sign of the result, if the result is zero, exponent underflow and exponent overflow respectively. The status bit D will be cleared to zero.

**Status Affected:** S, Z, U, V. (D always zero.)

**STACK CONTENT**




# SSUB

## SINGLE PRECISION FLOATING-POINT SUBTRACT

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | SRE | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

**Hex Coding:** 82 IF SRE = 1
02 IF SRE = 0

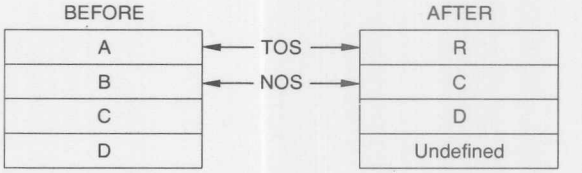
**Execution Time:** See Table 2

**Description:**

The single precision operand A at TOS is subtracted from the single precision operand B at NOS. The result is rounded to obtain the final single precision result R which is returned to TOS. The status bits S, Z, U and V are affected to report the sign of the result, if the result is zero, exponent underflow and exponent overflow respectively. The status bit D will be cleared to zero.

**Status Affected:** S, Z, U, V. (D always zero.)

**STACK CONTENTS**




# SMUL

## SINGLE PRECISION FLOATING-POINT MULTIPLY

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | SRE | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

**Hex Coding:** 83 IF SRE = 1
03 IF SRE = 0

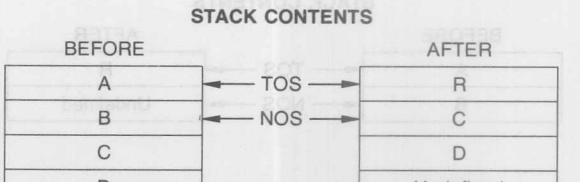
**Execution Time:** See Table 2

**Description:**

The single precision operand A from TOS is multiplied by the single precision operand B from NOS. The result is rounded to obtain the final single precision result R which is returned to TOS. The status bits S, Z, U and V are affected to report the sign of the result, if the result is zero, exponent underflow and exponent overflow respectively. The status bit D will be cleared to zero.

**Status Affected:** S, Z, U, V. (D always zero.)

**STACK CONTENTS**



# SDIV

## SINGLE PRECISION FLOATING-POINT DIVIDE

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | SRE | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

**Hex Coding:** 84 IF SRE = 1
04 IF SRE = 0

**Execution Time:** See Table 2

**Description:**
The single precision operand B from NOS is divided by the single precision operand A from TOS. The result (quotient) is rounded to obtain the final result R which is returned to TOS. The status bits S, Z, D, U and V are affected to report the sign of the result, if the result is zero, attempt to divide by zero, exponent underflow and exponent overflow respectively.

**Status Affected:** S, Z, D, U, V

**STACK CONTENTS**

| BEFORE | | AFTER |
|---|---|---|
| A | ← TOS → | R (see note) |
| B | ← NOS → | C |
| C | | D |
| D | | Undefined |

Note: If exponent field of A is zero then R = B (Divide exception).

# POPS

## POP STACK SINGLE PRECISION

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | SRE | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

**Hex Coding:** 87 IF SRE = 1
07 IF SRE = 0

**Execution Time:** See Table 2

**Description:**
The single precision operand A is popped from the stack. The internal stack control mechanism is such that A will be written at the bottom of the stack. The status bits S and Z are affected to report the sign of the new operand at TOS and if it is zero, respectively. The status bits U, V and D will be cleared to zero. Note that only the exponent field of the new TOS is checked for zero, if it is zero status bit Z will set to 1.

**Status Affected:** S, Z. (U, V, D always zero.)

**STACK CONTENTS**

| BEFORE | | AFTER |
|---|---|---|
| A | ← TOS → | B |
| B | ← NOS → | C |
| C | | D |
| D | | A |

# PTOD

## PUSH STACK DOUBLE PRECISION

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | SRE | 0 | 1 | 0 | 1 | 1 | 1 | 0 |

**Hex Coding:** AE IF SRE = 1
2E IF SRE = 0

**Execution Time:** See Table 2

**Description:**
The double precision operand A from the TOS is pushed back on to the stack. This is effectively a duplication of A into two consecutive stack locations. The status S and Z are affected to report sign of the new TOS and if the new TOS is zero respectively. The status bits U, V and D will be cleared to zero.

**Status Affected:** S, Z. (U, V, D always zero.)

**STACK CONTENTS**

| BEFORE | | AFTER |
|---|---|---|
| A | ← TOS → | A |
| B | ← NOS → | A |

# PTOS

## PUSH STACK SINGLE PRECISION

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | SRE | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

**Hex Coding:** 86 IF SRE = 1
06 IF SRE = 0

**Execution Time:** See Table 2

**Description:**
This instruction effectively pushes the single precision operand from TOS on to the stack. This amounts to duplicating the operand at two locations in the stack. However, if the operand at TOS prior to the PTOS command has only its exponent field as zero, the new content of the TOS will all be zeroes. The contents of NOS will be an exact copy of the old TOS. The status bits S and Z are affected to report the sign of the new TOS and if the content of TOS is zero, respectively. The status bits U, V and D will be cleared to zero.

**Status Affected:** S, Z. (U, V, D always zero.)

**STACK CONTENTS**

| BEFORE | | AFTER |
|---|---|---|
| A | ← TOS → | A* See note |
| B | ← NOS → | A |
| C | | B |
| D | | C |

Note: A* = A if Exponent field of A is not zero.
A* = 0 if Exponent field of A is zero.

7

# POPD

## POP STACK DOUBLE PRECISION

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | SRE | 0 | 1 | 0 | 1 | 1 | 1 | 1 |

**Hex Coding:** AF IF SRE = 1
2F IF SRE = 0

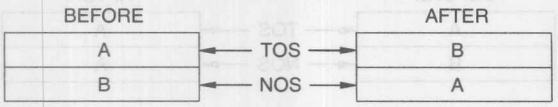
**Execution Time:** See Table 2

**Description:**

The double precision operand A is popped from the stack. The internal stack control mechanism is such that A will be written at the bottom of the stack. This operation has the same effect as exchanging TOS and NOS. The status bits S and Z are affected to report the sign of the new operand at TOS and if it is zero, respectively. The status bits U, V and D will be cleared to zero.

**Status Affected:** S, Z (U, V and D always zero.)

**STACK CONTENTS**




# XCHS

## EXCHANGE TOS AND NOS SINGLE-PRECISION

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | SRE | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

**Hex Coding:** 88 IF SRE = 1
08 IF SRE = 0

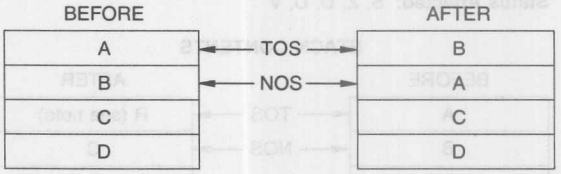
**Execution Time:** See Table 2

**Description:**

The single precision operand A at the TOS and the single precision operand B at the NOS are exchanged. After execution, B is at the TOS and A is at the NOS. All other operands are unchanged.

**Status Affected:** S, Z (U, V and D always zero.)

**STACK CONTENTS**



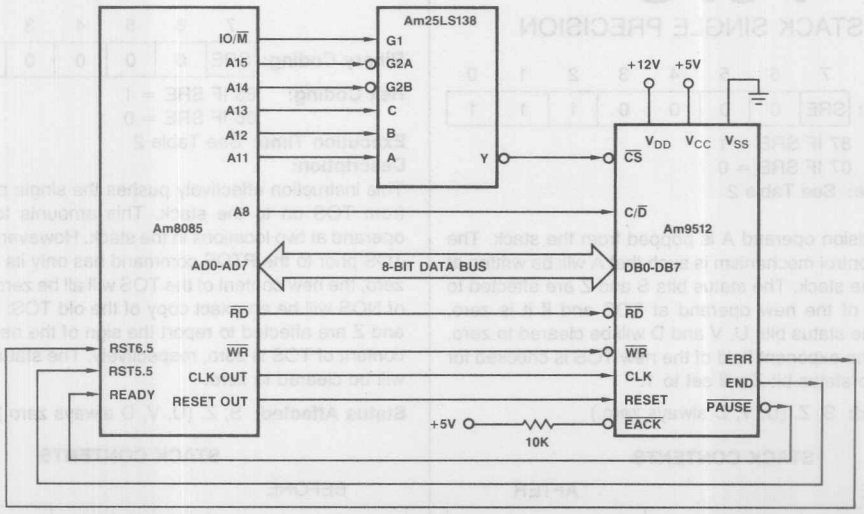




**Figure 1. Am9512 to Am8085 Interface.**

MOS-213

| | |
|---|---|
| Ambient Temperature Under Bias | −55°C to +125°C |
| VDD with Respect to VSS | −0.5V to +15.0V |
| VCC with Respect to VSS | −0.5V to +7.0V |
| All Signal Voltages with Respect to VSS | −0.5V to +7.0V |
| Power Dissipation (Package Limitation) | 2.0W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGE

| Part Number | Ambient Temperature | VSS | VCC | VDD |
|---|---|---|---|---|
| Am9512DC | $0°C \leq T_A \leq +70°C$ | 0V | +5.0V ±5% | +12V ±5% |
| Am9512DM | $-55°C \leq T_A \leq +125°C$ | 0V | +5.0V ±10% | +12V ±10% |

## ELECTRICAL CHARACTERISTICS Over Operating Range (Note 1)

| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| VOH | Output HIGH Voltage | IOH = −200μA | 3.7 | | | Volts |
| VOL | Output LOW Voltage | IOL = 3.2mA | | | 0.4 | Volts |
| VIH | Input HIGH Voltage | | 2.0 | | VCC | Volts |
| VIL | Input LOW Voltage | | −0.5 | | 0.8 | Volts |
| IIX | Input Load Current | $VSS \leq VI \leq VCC$ | | | ±10 | μA |
| IOZ | Data Bus Leakage | VO = 0.4V | | | 10 | μA |
| | | VO = VCC | | | 10 | |
| ICC | VCC Supply Current | $T_A$ = +25°C | | 50 | 90 | mA |
| | | $T_A$ = 0°C | | | 95 | |
| | | $T_A$ = −55°C | | | 100 | |
| IDD | VDD Supply Current | $T_A$ = +25°C | | 50 | 90 | mA |
| | | $T_A$ = 0°C | | | 95 | |
| | | $T_A$ = −55°C | | | 100 | |
| CO | Output Capacitance | fc = 1.0MHz, Inputs = 0V | | 8 | 10 | pF |
| CI | Input Capacitance | | | 5 | 8 | pF |
| CIO | I/O Capacitance | | | 10 | 12 | pF |

7

## SWITCHING CHARACTERISTICS

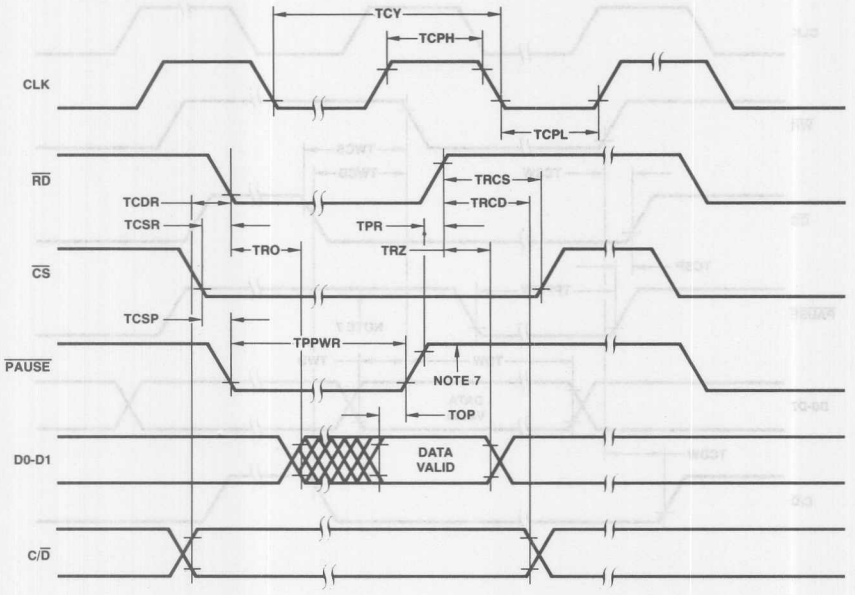
| Parameters | Description | | Am9512DC Min | Am9512DC Max | Am9512-1DC Min | Am9512-1DC Max | Units |
|---|---|---|---|---|---|---|---|
| TAPW | $\overline{EACK}$ LOW Pulse Width | | 100 | | 75 | | ns |
| TCDR | C/$\overline{D}$ to $\overline{RD}$ LOW Set-up Time | | 0 | | 0 | | ns |
| TCDW | C/$\overline{D}$ to $\overline{WR}$ LOW Set-up Time | | 0 | | 0 | | ns |
| TCPH | Clock Pulse HIGH Width | | 200 | 500 | 140 | 500 | ns |
| TCPL | Clock Pulse LOW Width | | 240 | | 160 | | ns |
| TCSP | $\overline{CS}$ LOW to $\overline{PAUSE}$ LOW Delay (Note 5) | | 150 | | 100 | | ns |
| TCSR | $\overline{CS}$ to $\overline{RD}$ LOW Set-up Time | | 0 | | 0 | | ns |
| TCSW | $\overline{CS}$ LOW to $\overline{WR}$ LOW Set-up Time | | 0 | | 0 | | ns |
| TCY | Clock Period | | 480 | 5000 | 320 | 2000 | ns |
| TDW | Data Valid to $\overline{WR}$ HIGH Delay | | 150 | | 100 | | ns |
| TEAE | $\overline{EACK}$ LOW to END LOW Delay | | | 200 | | 175 | ns |
| TEHPHR | END HIGH to $\overline{PAUSE}$ HIGH Data Read when Busy | | | 5.5TCY+300 | | 5.5TCY+200 | ns |
| TEHPHW | END HIGH to $\overline{PAUSE}$ HIGH Write when Busy | | | 200 | | 175 | ns |
| TEPW | END HIGH Pulse Width | | 400 | | 300 | | ns |
| TEX | Execution Time | | See Table 2 | | | | ns |
| TOP | Data Bus Output Valid to $\overline{PAUSE}$ HIGH Delay | | 0 | | 0 | | ns |
| TPPWR | $\overline{PAUSE}$ LOW Pulse Width Read | Data | 3.5TCY+50 | 5.5TCY+300 | 3.5TCY+50 | 5.5TCY+200 | ns |
| | | Status | 1.5TCY+50 | 3.5TCY+300 | 1.5TCY+50 | 3.5TCY+200 | |
| TPPWRB | END HIGH to $\overline{PAUSE}$ HIGH Read when Busy | Data | See Table 2 | | | | ns |
| | | Status | 1.5TCY+50 | 3.5TCY+300 | 1.5TCY+50 | 3.5TCY+200 | |
| TPPWW | $\overline{PAUSE}$ LOW Pulse Width Write when Not Busy | | | TCSW+50 | | TCSW+50 | ns |
| TPPWWB | $\overline{PAUSE}$ LOW Pulse Width Write when Busy | | See Table 2 | | | | ns |
| TPR | $\overline{PAUSE}$ HIGH to Read HIGH Hold Time | | 0 | | 0 | | ns |
| TPW | $\overline{PAUSE}$ HIGH to Write HIGH Hold Time | | 0 | | 0 | | ns |
| TRCD | $\overline{RD}$ HIGH to C/$\overline{D}$ Hold Time | | 0 | | 0 | | ns |
| TRCS | $\overline{RD}$ HIGH to $\overline{CS}$ HIGH Hold Time | | 0 | | 0 | | ns |
| TRO | $\overline{RD}$ LOW to Data Bus On Delay | | 50 | | 50 | | ns |
| TRZ | $\overline{RD}$ HIGH to Data Bus Off Delay | | 50 | 200 | 50 | 150 | ns |
| TSAPW | SVACK LOW Pulse Width | | 100 | | 75 | | ns |
| TSAR | SVACK LOW to SVREQ LOW Delay | | | 300 | | 200 | ns |
| TWCD | $\overline{WR}$ HIGH to C/D Hold Time | | 60 | | 30 | | ns |
| TWCS | $\overline{WR}$ HIGH to CS HIGH Hold Time | | 60 | | 30 | | ns |
| TWD | $\overline{WR}$ HIGH to Data Bus Hold Time | | 20 | | 20 | | ns |

NOTES:

1. Typical values are for $T_A$ = 25°C, nominal supply voltages and nominal processing parameters.
2. Switching parameters are listed in alphabetical order.
3. Test conditions assume transition times of 20ns or less, output loading of one TTL gate plus 100pF and timing reference levels of 0.8V and 2.0V.
4. END HIGH pulse width is specified for $\overline{EACK}$ tied to VSS. Otherwise TEAE applies.
5. $\overline{PAUSE}$ is pulled low for both command and data operations.
6. TEX is the execution time of the current command (see the Command Execution Times table).
7. $\overline{PAUSE}$ will go low at this point if $\overline{CS}$ is low and $\overline{RD}$ and $\overline{WR}$ are high.

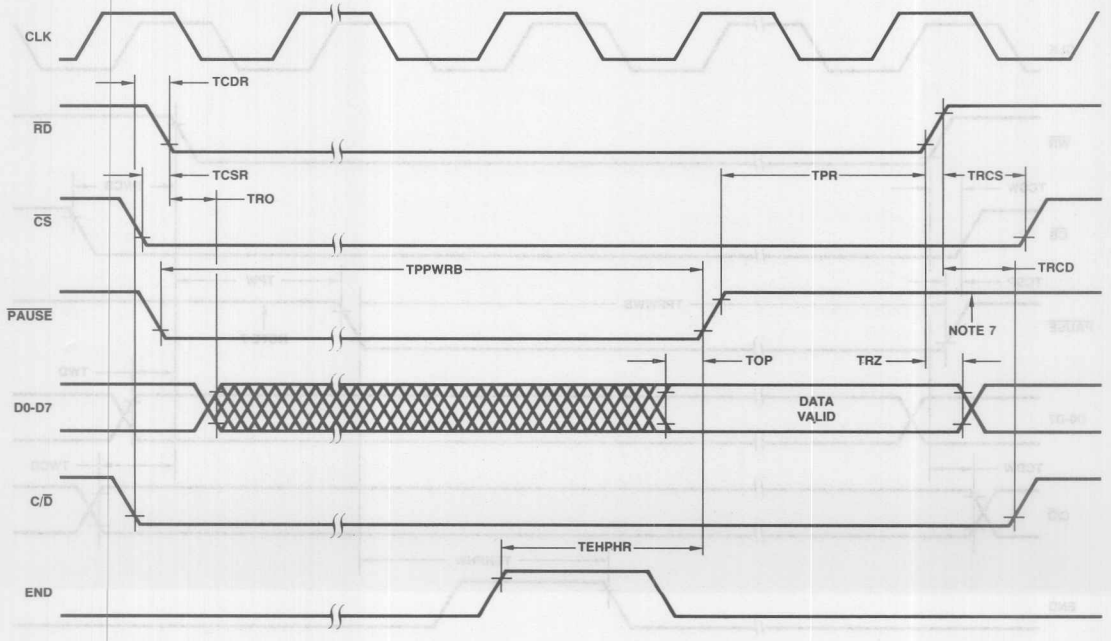
## TIMING DIAGRAMS

### READ OPERATION




MOS-208

### OPERAND READ WHEN Am9512 IS BUSY

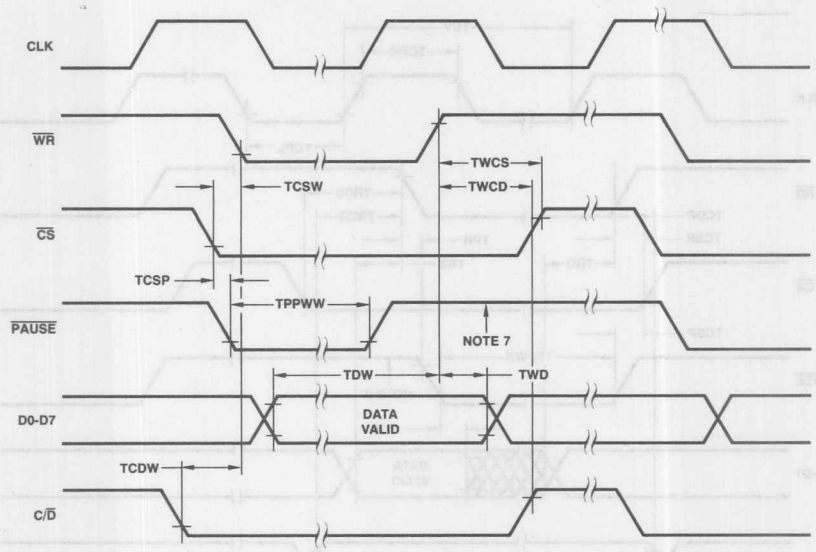



MOS-209

7

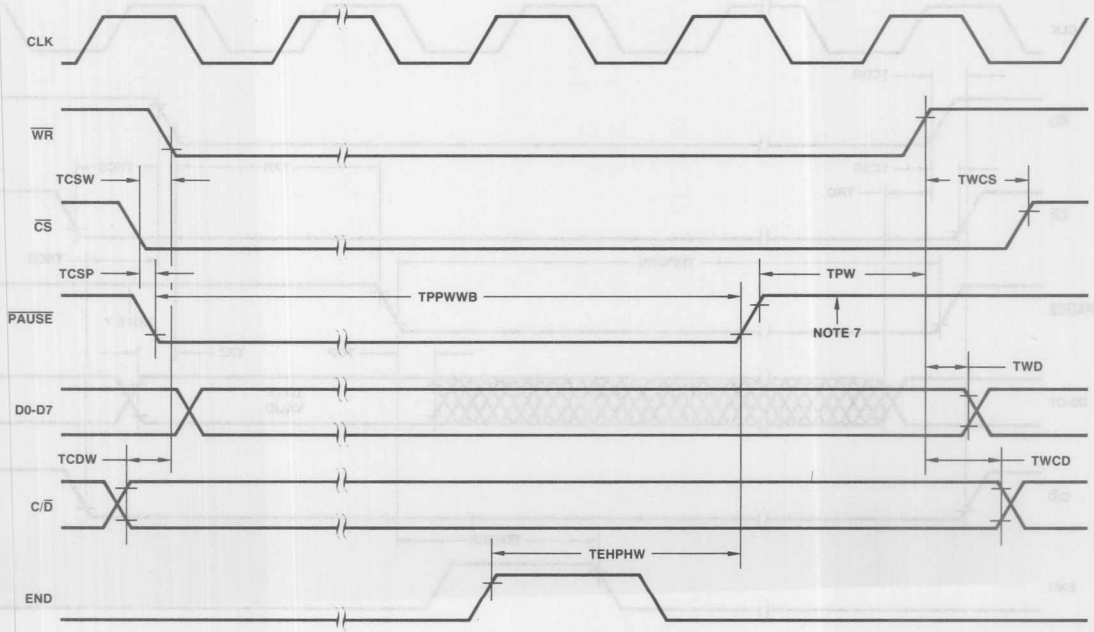
## TIMING DIAGRAMS (Cont.)

### OPERAND ENTRY



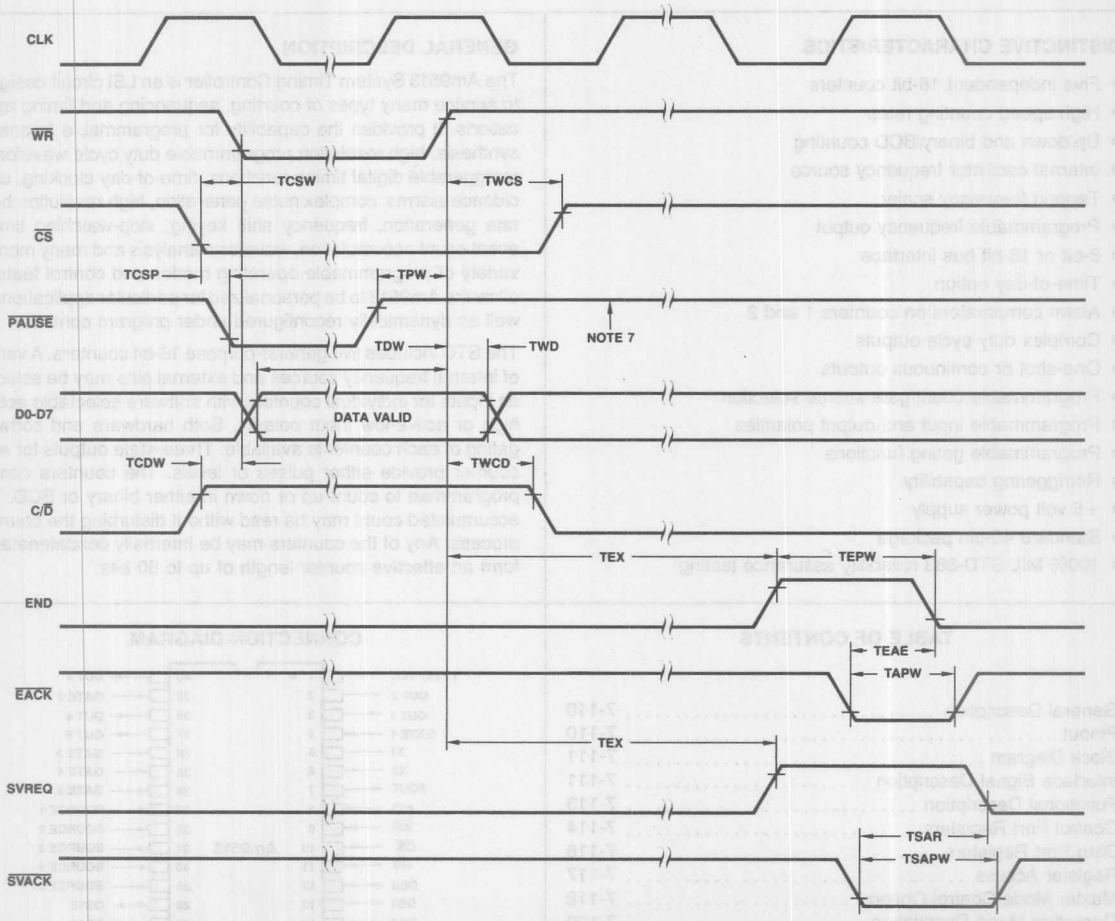

MOS-210

### COMMAND OR DATA WRITE WHEN Am9512 IS BUSY




MOS-211

## COMMAND INITIATION




MOS-212

7

# Am9513

## System Timing Controller

### DISTINCTIVE CHARACTERISTICS

- Five independent 16-bit counters
- High speed counting rates
- Up/down and binary/BCD counting
- Internal oscillator frequency source
- Tapped frequency scaler
- Programmable frequency output
- 8-bit or 16-bit bus interface
- Time-of-day option
- Alarm comparators on counters 1 and 2
- Complex duty cycle outputs
- One-shot or continuous outputs
- Programmable count/gate source selection
- Programmable input and output polarities
- Programmable gating functions
- Retriggering capability
- +5 volt power supply
- Standard 40-pin package
- 100% MIL-STD-883 reliability assurance testing

### GENERAL DESCRIPTION

The Am9513 System Timing Controller is an LSI circuit designed to service many types of courting, sequencing and timing applications. It provides the capability for programmable frequency synthesis, high resolution programmable duty cycle waveforms, retriggerable digital timing functions, time-of-day clocking, coincidence alarms, complex pulse generation, high resolution baud rate generation, frequency shift keying, stop-watching timing, event count accumulation, waveform analysis and many more. A variety of programmable operating modes and control features allow the Am9513 to be personalized for particular applications as well as dynamically reconfigured under program control.

The STC includes five general-purpose 16-bit counters. A variety of internal frequency sources and external pins may be selected as inputs for individual counters with software selectable active-high or active-low input polarity. Both hardware and software gating of each counter is available. Three-state outputs for each counter provide either pulses or levels. The counters can be programmed to count up or down in either binary or BCD. The accumulated count may be read without disturbing the counting process. Any of the counters may be internally concatenated to form an effective counter length of up to 80 bits.

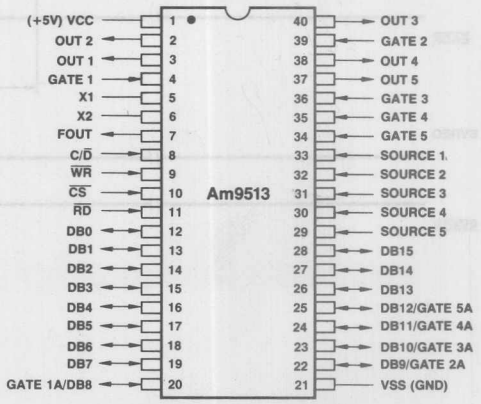
### TABLE OF CONTENTS


General Description ..... 7-110
Pinout ..... 7-110
Block Diagram ..... 7-111
Interface Signal Description ..... 7-111
Functional Description ..... 7-113
Control Port Registers ..... 7-114
Data Port Registers ..... 7-116
Register Access ..... 7-117
Master Mode Control Options ..... 7-118
Operating Mode Description ..... 7-120
Counter Mode Control Options ..... 7-124
Command Descriptions ..... 7-126
Maximum Ratings ..... 7-130
Electrical Characteristics ..... 7-130
Switching Characteristics ..... 7-132
Applications Information ..... 7-134



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### CONNECTION DIAGRAM




Top View

Pin 1 is marked for orientation. MOS-172

**Figure 1.**

### ORDERING INFORMATION

| Package Type | Temperature Range | Counting Frequency 7MHz | |
|---|---|---|---|
| Molded | $0°C \leq T_A \leq +70°C$ | AM9513PC | |
| Hermetic* | | AM9513DC | |
| | | AM9513CC | |
| Hermetic | $-55°C \leq T_A \leq +125°C$ | AM9513DM | |

*Hermetic = Ceramic = DC = CC = D-40-1.

# Am9517A

## Multimode DMA Controller

### DISTINCTIVE CHARACTERISTICS

- Four independent DMA channels, each with separate registers for Mode Control, Current Address, Base Address, Current Word Count and Base Word Count.
- Transfer modes: Block, Demand, Single Word, Cascade
- Independent autoinitialization of all channels
- Memory-to-memory transfers
- Memory block initialization
- Address increment or decrement
- Master system disable
- Enable/disable control of individual DMA requests
- Directly expandable to any number of channels
- End of Process input for terminating transfers
- Software DMA requests
- Independent polarity control for DREQ and DACK signals
- Compressed timing option speeds transfers — up to 2M words/second
- +5 volt power supply
- Advanced N-channel silicon gate MOS technology
- 40 pin Hermetic DIP package
- 100% MIL-STD-883 reliability assurance testing

### GENERAL DESCRIPTION

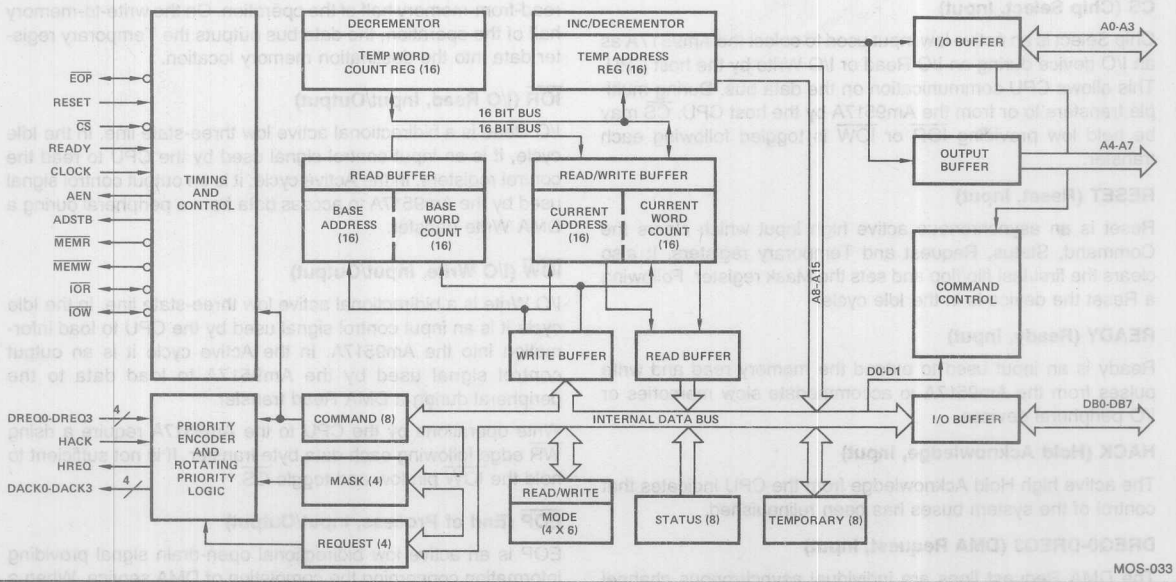
The Am9517A Multimode Direct Memory Access (DMA) Controller is a peripheral interface circuit for microprocessor systems. It is designed to improve system performance by allowing external devices to directly transfer information to or from the system memory. Memory-to-memory transfer capability is also provided. The Am9517A offers a wide variety of programmable control features to enhance data throughput and system optimization and to allow dynamic reconfiguration under program control.

The Am9517A is designed to be used in conjunction with an external 8-bit address register such as the Am74LS373. It contains four independent channels and may be expanded to any number of channels by cascading additional controller chips.

The three basic transfer modes allow programmability of the types of DMA service by the user. Each channel can be individually programmed to Autoinitialize to its original condition following an End of Process ($\overline{EOP}$).

Each channel has a full 64K address and word count capability. An external $\overline{EOP}$ signal can terminate a DMA or memory-to-memory transfer. This is useful for block search or compare operations using external comparators or for intelligent peripherals to abort erroneous services.

### BLOCK DIAGRAM

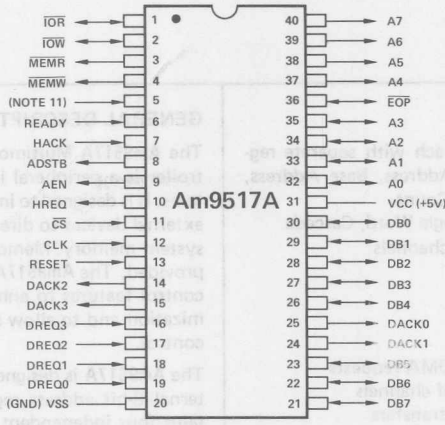



MOS-033

### ORDERING INFORMATION

| Package Type | Ambient Temperature | Maximum Clock Frequency | |
|---|---|---|---|
| | | 3MHz | 4MHz |
| Hermetic DIP/ Molded DIP | $0°C \leq T_A \leq +70°C$ | AM9517ADC/PC<br>AM9517A-1DC/PC | AM9517A-4DC/PC |
| Hermetic DIP | $-55°C \leq T_A \leq +125°C$ | AM9517ADM | |

## CONNECTION DIAGRAM




Top View
Pin 1 is marked for orientation.

**Figure 1.** MOS-034

## INTERFACE SIGNAL DESCRIPTION

**VCC:** +5 Volt Supply
**VSS:** Ground

### CLK (Clock, Input)

This input controls the internal operations of the Am9517A and its rate of data transfers. The input may be driven at up to 3MHz for the standard Am9517A and up to 4MHz for the Am9517A-4.

### $\overline{CS}$ (Chip Select, Input)

Chip Select is an active low input used to select the Am9517A as an I/O device during an I/O Read or I/O Write by the host CPU. This allows CPU communication on the data bus. During multiple transfers to or from the Am9517A by the host CPU, $\overline{CS}$ may be held low providing $\overline{IOR}$ or $\overline{IOW}$ is toggled following each transfer.

### RESET (Reset, Input)

Reset is an asynchronous active high input which clears the Command, Status, Request and Temporary registers. It also clears the first/last flip/flop and sets the Mask register. Following a Reset the device is in the Idle cycle.

### READY (Ready, Input)

Ready is an input used to extend the memory read and write pulses from the Am9517A to accommodate slow memories or I/O peripheral devices.

### HACK (Hold Acknowledge, Input)

The active high Hold Acknowledge from the CPU indicates that control of the system buses has been relinquished.

### DREQ0-DREQ3 (DMA Request, Input)

The DMA Request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In Fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. Polarity of DREQ is programmable. Reset initializes these lines to active high.

### DB0-DB7 (Data Bus, Input/Output)

The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled during the I/O Read by the host CPU, permitting the CPU to examine the contents of an Address register, the Status register, the Temporary register or a Word Count register. The Data Bus is enabled to input data during a host CPU I/O write, allowing the CPU to program the Am9517A control registers. During DMA cycles the most significant eight bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations data from the source memory location comes into the Am9517A's Temporary register on the read-from-memory half of the operation. On the write-to-memory half of the operation, the data bus outputs the Temporary register data into the destination memory location.

### $\overline{IOR}$ (I/O Read, Input/Output)

I/O Read is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to read the control registers. In the Active cycle, it is an output control signal used by the Am9517A to access data from a peripheral during a DMA Write transfer.

### $\overline{IOW}$ (I/O Write, Input/Output)

I/O Write is a bidirectional active low three-state line. In the Idle cycle it is an input control signal used by the CPU to load information into the Am9517A. In the Active cycle it is an output control signal used by the Am9517A to load data to the peripheral during a DMA Read transfer.

Write operations by the CPU to the Am9517A require a rising $\overline{WR}$ edge following each data byte transfer. It is not sufficient to hold the $\overline{IOW}$ pin low and toggle $\overline{CS}$.

### $\overline{EOP}$ (End of Process, Input/Output)

$\overline{EOP}$ is an active low bidirectional open-drain signal providing information concerning the completion of DMA service. When a channel's Word Count goes to zero, the Am9517A pulses $\overline{EOP}$ low to provide the peripheral with a completion signal. $\overline{EOP}$ may also be pulled low by the peripheral to cause premature completion. The reception of $\overline{EOP}$, either internal or external, causes the currently active channel to terminate the service, to set its TC bit in the Status register and to reset its request bit. If Autoinitialization is selected for the channel, the current registers will be updated from the base registers. Otherwise the channel's mask bit will be set and the register contents will remain unaltered.

During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs. $\overline{EOP}$ always applies to the channel with an active DACK; external $\overline{EOPS}$ are disregarded in DACK0-DACK3 are all inactive.

Because $\overline{EOP}$ is an open-drain signal, an external pullup resistor is required. Values of 3.3K or 4.7K are recommended; the $\overline{EOP}$ pin can not sink the current passed by a 1K pullup.

**A0-A3 (Address, Input/Output)**

The four least significant address lines are bidirectional 3-state signals. During DMA Idle cycles they are inputs and allow the host CPU to load or read control registers. When the DMA is active, they are outputs and provide the lower 4-bits of the output address.

**A4-A7 (Address, Output)**

The four most significant address lines are three-state outputs and provide four bits of address. These lines are enabled only during DMA service.

**HREQ (Hold Request, Output)**

The Hold Request to the CPU is used by the DMA to request control of the system bus. Software requests or unmasked DREQs cause the Am9517A to issue HREQ.

**DACK0-DACK3 (DMA Acknowledge, Output)**

The DMA Acknowledge lines indicate that a channel is active. In many systems they will be used to select a peripheral. Only one DACK will be active at a time and none will be active unless the DMA is in control of the bus. The polarity of these lines is programmable. Reset initializes them to active-low.

**AEN (Address Enable, Output)**

Address Enable is an active high signal used to disable the system bus during DMA cycles to enable the output of the external latch which holds the upper byte of the address. Note that during DMA transfers HACK and AEN should be used to deselect all other I/O peripherals which may erroneously be accessed as programmed I/O during the DMA operation. The Am9517A automatically deselects itself by disabling the $\overline{CS}$ input during DMA transfers.

**ADSTB (Address Strobe, Output)**

The active high Address Strobe is used to strobe the upper address byte from DB0-DB7 into an external latch.

**$\overline{MEMR}$ (Memory Read, Output)**

The Memory Read signal is an active low three-state output used to access data from the selected memory location during a memory-to-peripheral or a memory-to-memory transfer.

| Name | Size | Number |
|---|---|---|
| Base Address Registers | 16 bits | 4 |
| Base Word Count Registers | 16 bits | 4 |
| Current Address Registers | 16 bits | 4 |
| Current Word Count Registers | 16 bits | 4 |
| Temporary Address Register | 16 bits | 1 |
| Temporary Word Count Register | 16 bits | 1 |
| Status Register | 8 bits | 1 |
| Command Register | 8 bits | 1 |
| Temporary Register | 8 bits | 1 |
| Mode Registers | 6 bits | 4 |
| Mask Register | 4 bits | 1 |
| Request Register | 4 bits | 1 |

**Figure 2. Am9517A Internal Registers.**

**$\overline{MEMW}$ (Memory Write, Output)**

The Memory Write signal is an active low three-state output used to write data to the selected memory location during a peripheral-to-memory or a memory-to-memory transfer.

## FUNCTIONAL DESCRIPTION

The Am9517A block diagram includes the major logic blocks and all of the internal registers. The data interconnection paths are also shown. Not shown are the various control signals between the blocks. The Am9517A contains 344 bits of internal memory in the form of registers. Figure 2 lists these registers by name and shows the size of each. A detailed description of the registers and their functions can be found under Register Description.

The Am9517A contains three basic blocks of control logic. The Timing Control block generates internal timing and external control signals for the Am9517A. The Program Command Control block decodes the various commands given to the Am9517A by the microprocessor prior to servicing a DMA Request. It also decodes each channel's Mode Control word. The Priority Encoder block resolves priority contention among DMA channels requesting service simultaneously.

The Timing Control block derives internal timing from the clock input. In Am9080A systems this input will usually be the $\phi 2$ TTL clock from an Am8224. However, any appropriate system clock will suffice.

**DMA Operation**

The Am9517A is designed to operate in two major cycles. These are called Idle and Active cycles. Each device cycle is made up of a number of states. The Am9517A can assume seven separate states, each composed of one full clock period. State 1 (S1) is the inactive state. It is entered when the Am9517A has no valid DMA requests pending. While in S1, the DMA controller is inactive but may be in the Program Condition, being programmed by the processor. State 0 (S0) is the first state of a DMA service. The Am9517A has requested a hold but the processor has not yet returned an acknowledge. An acknowledge from the CPU will signal that transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted before S4 by the use of the Ready line on the Am9517A.

Memory-to-memory transfers require a read-from and a write-to-memory to complete each transfer. The states, which resemble the normal working states, use two digit numbers for identification. Eight states are required for each complete transfer. The first four states (S11, S12, S13, S14) are used for the read-from-memory half and the last four states (S21, S22, S23 and S24) for the write-to-memory half of the transfer. The Temporary Data register is used for intermediate storage of the memory byte.

**IDLE Cycle**

When no channel is requesting service, the Am9517A will enter the Idle cycle and perform "S1" states. In this cycle the Am9517A will sample the DREQ lines every clock cycle to determine if any channel is requesting a DMA service. The device will also sample $\overline{CS}$, looking for an attempt by the microprocessor to write or read the internal registers of the Am9517A. When $\overline{CS}$ is low and HACK is low the Am9517A enters the Program Condition. The CPU can now establish, change or inspect the internal definition of the part by reading from or writing to the internal registers. Address lines A0-A3 are inputs to the device and select which registers will be read or written. The $\overline{IOR}$ and $\overline{IOW}$ lines are used to select and time reads or writes. Due to the

determine the upper or lower byte of the 16-bit Address and Word Count registers. The flip/flop is reset by Master Clear or Reset. A separate software command can also reset this flip/flop.

Special software commands can be executed by the Am9517A in the Program Condition. These commands are decoded as sets of addresses when both $\overline{CS}$ and $\overline{IOW}$ are active and do not make use of the data bus. Functions include Clear First/Last Flip/Flop and Master Clear.

## ACTIVE CYCLE

When the Am9517A is in the Idle cycle and a channel requests a DMA service, the device will output a HREQ to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

**Single Transfer Mode:** In Single Transfer mode, the Am9517A will make a one-byte transfer during each HREQ/HACK handshake. When DREQ goes active, HREQ will go active. After the CPU responds by driving HACK active, a one-byte transfer will take place. Following the transfer, HREQ will go inactive, the word count will be decremented and the address will be either incremented or decremented. When the word count goes to zero a Terminal Count (TC) will cause an Autoinitialize if the channel has been programmed to do so.

To perform a single transfer, DREQ must be held active only until the corresponding DACK goes active. If DREQ is held continuously active, HREQ will go inactive following each transfer and then will go active again and a new one-byte transfer will be made following each rising edge of HACK. In 8080A/9080A systems this will ensure one full machine cycle of execution between DMA transfers. Details of timing between the Am9517A and other bus control protocols will depend upon the characteristics of the microprocessor involved.

**Block Transfer Mode:** In Block Transfer mode, the Am9517A will continue making transfers until a TC (caused by the word count going to zero) or an external End of Process ($\overline{EOP}$) is encountered. DREQ need be held active only until DACK becomes active. An autoinitialize will occur at the end of the service if the channel has been programmed for it.

**Demand Transfer Mode:** In Demand Transfer mode the device will continue making transfers until a TC or external $\overline{EOP}$ is encountered or until DREQ goes inactive. Thus, the device requesting service may discontinue transfers by bringing DREQ inactive. Service may be resumed by asserting an active DREQ once again. During the time between services when the microprocessor is allowed to operate, the intermediate values of address and word count may be read from the Am9517A Current Address and Current Word Count registers. Autoinitialization will only occur following a TC or $\overline{EOP}$ at the end of service. Following Autoinitialization, an active-going DREQ edge is required to initiate a new DMA service.

**Cascade Mode:** This mode is used to cascade more than one Am9517A together for simple system expansion. The HREQ and HACK signals from the additional Am9517A are connected to the DREQ and DACK signals of a channel of the initial Am9517A. This allows the DMA requests of the additional device to propagate through the priority network circuitry of the preceding device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests. Since the cascade channel in the initial device is used only for prioritizing the additional device, it does not output any address or control to DREQ with DACK but all other outputs except HREQ will be disabled.

Figure 3 shows two additional devices cascaded into an initial device using two of the previous channels. This forms a two level DMA system. More Am9517As could be added at the second level by using the remaining channels of the first level. Additional devices can also be added by cascading into the channels of the second level devices forming a third level.

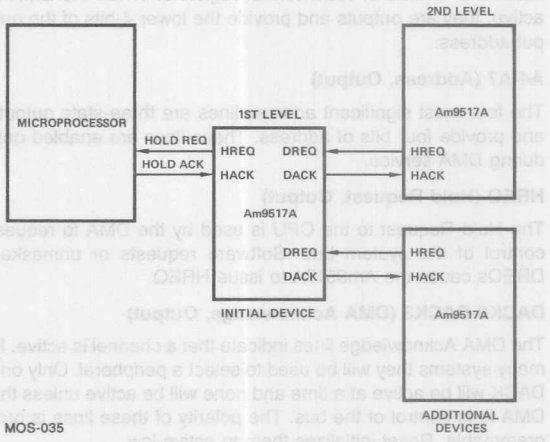



**Figure 3. Cascaded Am9517As.**

## TRANSFER TYPES

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write and Verify. Write transfers move data from an I/O device to the memory by activating $\overline{IOR}$ and $\overline{MEMW}$. Read transfers move data from memory to an I/O device by activating $\overline{MEMR}$ and $\overline{IOW}$. Verify transfers are pseudo transfers; the Am9517A operates as in Read or Write transfers generating addresses, responding to $\overline{EOP}$, etc., however, the memory and I/O control lines remain inactive.

**Memory-to-Memory:** The Am9517A includes a block move capability that allows blocks of data to be moved from one memory address space to another. When Bit C0 in the Command register is set to a logical 1, channels 0 and 1 will operate as memory-to-memory transfer channels. Channel 0 forms the source address and channel 1 forms the destination address. The channel 1 word count is used. A memory-to-memory transfer is initiated by setting a software DMA request for channel 0. Block Transfer Mode should be used for memory-to-memory. When channel 0 is programmed for a fixed source address, a single source word may be written into a block of memory.

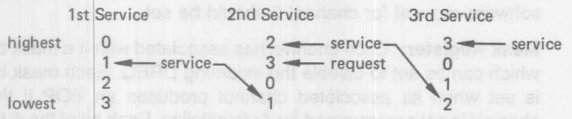
When setting up the Am9517A for memory-to-memory operation, it is suggested that both channels 0 and 1 be masked out. Further, the channel 0 word count should be initialized to the same value used in channel 1. No DACK outputs will be active during memory-to-memory transfers.

The Am9517A will respond to external $\overline{EOP}$ signals during memory-to-memory transfers. Data comparators in block search schemes may use this input to terminate the service when a match is found. The timing of memory-to-memory transfers may be found in Timing Diagram 4.

**Autointialize:** By programming a bit in the Mode register a channel may be set up for an Autoinitialize operation. During Autoinitialization, the original values of the Current Address and Current Word Count registers are automatically restored from the Base Address and Base Word Count registers of that channel following $\overline{EOP}$. The base registers are loaded simultaneously with the current registers by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not set by $\overline{EOP}$ when the channel is in Autoinitialize. Following Autoinitialize the channel is ready to repeat its service without CPU intervention.

**Priority:** The Am9517A has two types of priority encoding available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon the descending value of their number. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel, 0.

The second scheme is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly. With Rotating Priority in a single chip DMA system, any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. This prevents any one channel from monopolizing the system.




The priority encoder selects the highest priority channel requesting service on each active-going HACK edge. Once a channel is started, its operation will not be suspended if a request is received by a higher priority channel. The high priority channel will only gain control after the lower priority channel releases HREQ. When control is passed from one channel to another, the CPU will always gain bus control. This ensures generation of rising HACK edge to be used to initiate selection of the new highest-priority requesting channel.

**Compressed Timing:** In order to achieve even greater throughput where system characteristics permit, the Am9517A can compress the transfer time to two clock cycles. From Timing Diagram 3 it can be seen that state S3 is used to extend the access time of the read pulse. By removing state S3 the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. S1 states will still occur when A8-A15 need updating (see Address Generation). Timing for compressed transfers is found in Timing Diagram 6.

**Address Generation:** In order to reduce pin count, the Am9517A multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a 3-state enable. The lower order address bits are output by the Am9517A directly. Lines A0-A7 should be connected to the address bus. Timing Diagram 3 shows the time relationships between CLK, AEN, ADSTB, DB0-DB7 and A0-A7.

During Block and Demand Transfer mode services which include multiple transfers, the addresses generated will be sequential. For many transfers the data held in the external address latch will remain the same. This data need only change when a carry or borrow from A7 to A8 takes place in the normal sequence of addresses. To save time and speed transfers, the Am9517A executes S1 states only when updating of A8-A15 in the latch is necessary. This means for long services, S1 states may occur only once every 256 transfers, a savings of 255 clock cycles for each 256 transfers.

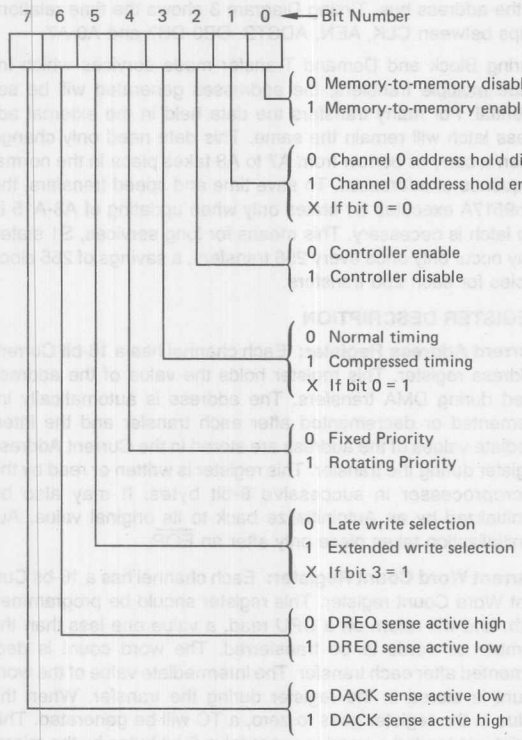
## REGISTER DESCRIPTION

**Current Address Register:** Each channel has a 16-bit Current Address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address register during the transfer. This register is written or read by the microprocessor in successive 8-bit bytes. It may also be reinitialized by an Autoinitialize back to its original value. Autoinitialization takes place only after an $\overline{EOP}$.

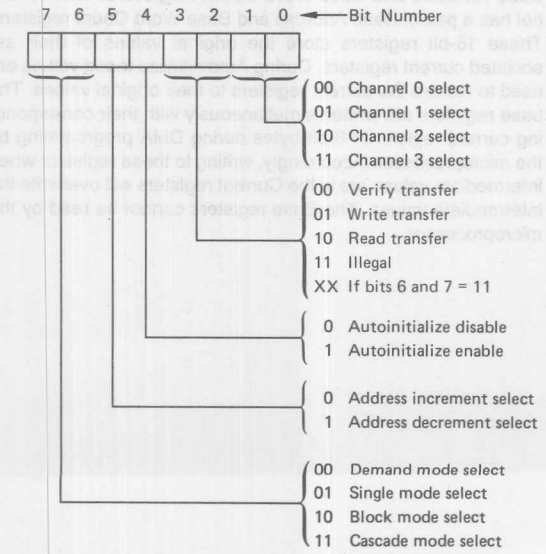
**Current Word Count Register:** Each channel has a 16-bit Current Word Count register. This register should be programmed with, and will return on a CPU read, a value one less than the number of words to be transferred. The word count is decremented after each transfer. The intermediate value of the word count is stored in the register during the transfer. When the value in the register goes to zero, a TC will be generated. This register is loaded or read in successive 8-bit bytes by the microprocessor in the Program Condition. Following the end of a DMA service it may also be reinitialized by an Autoinitialize back to its original value. Autoinitialize can occur only when an $\overline{EOP}$ occurs. Note that the contents of the Word Count register will be FFFF (hex) following on internally generated $\overline{EOP}$.

**Base Address and Base Word Count Registers:** Each channel has a pair of Base Address and Base Word Count registers. These 16-bit registers store the original values of their associated current registers. During Autoinitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in 8-bit bytes during DMA programming by the microprocessor. Accordingly, writing to these registers when intermediate values are in the Current registers will overwrite the intermediate values. The Base registers cannot be read by the microprocessor.

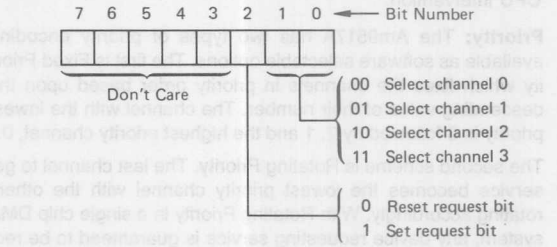
**Command Register:** This 8-bit register controls the operation of the Am9517A. It is programmed by the microprocessor in the Program Condition and is cleared by Reset. The following table lists the function of the command bits. See Figure 4 for address coding.




**Mode Register:** Each channel has a 6-bit Mode register associated with it. When the register is being written to by the microprocessor in the Program Condition, bits 0 and 1 determine which channel Mode register it to be written.

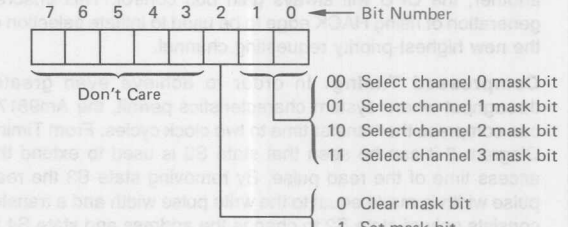



**Request Register:** The Am9517A can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit Request register. These are nonmaskable and subject to prioritization by the Priority Encoder network. Each register bit is set or reset separately under software control or is cleared upon generation of a TC or external EOP. The entire register is cleared by a Reset. To set or reset a bit, the software loads the proper form of the data word. See Figure 4 for address coding.

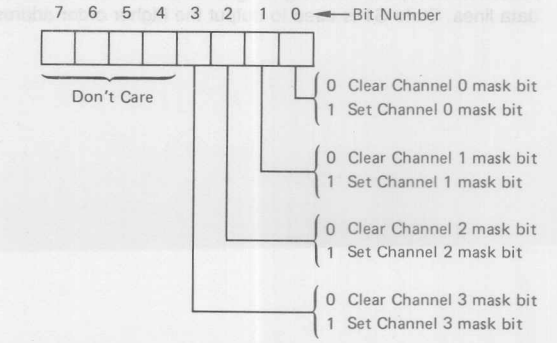



Software requests will be serviced only if the channel is in Block mode. When initiating a memory-to-memory transfer, the software request for channel 0 should be set.

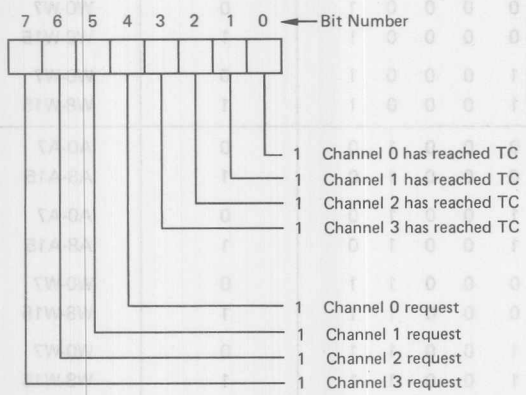
**Mask Register:** Each channel has associated with it a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an EOP if the channel is not programmed for Autoinitialize. Each bit of the 4-bit Mask register may also be set or cleared separately under software control. The entire register is also set by a Reset. This disables all DMA requests until a clear Mask register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the Request register. See Figure 4 for instruction addressing.




All four bits of the Mask Register may also be written with a single command.



**Status Register:** The Status registers may be read out of the Am9517A by the microprocessor. It indicates which channels have reached a terminal count and which channels have pending DMA requests. Bits 0-3 are set each time a TC is reached by that channel, including after each Autoinitialization. These bits are cleared by Reset and each Status Read. Bits 4-7 are set whenever their corresponding channel is requesting service.




**Temporary Register:** The Temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the microprocessor in the Program Condition. The Temporary register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a Reset.

**Software Commands:** There are two special software commands which can be executed in the Program Condition. They do not depend on any specific bit pattern on the data bus. The two software commands are:

Clear First/Last Flip/Flop: This command may be issued prior to writing or reading Am9517A address or word count information. This initializes the flip/flop to a known state so that subsequent accesses to register contents by the microprocessor will address lower and upper bytes in the correct sequence.

Master Clear: This software instruction has the same effect as the hardware Reset. The Command, Status, Request, Temporary and Internal First/Last Flip/Flop registers are cleared and the Mask register is set. The Am9517A will enter the Idle cycle.

Figure 4 lists the address codes for the software commands.

| Interface Signals | | | | | | Operation |
|---|---|---|---|---|---|---|
| A3 | A2 | A1 | A0 | $\overline{IOR}$ | $\overline{IOW}$ | |
| 1 | 0 | 0 | 0 | 0 | 1 | Read Status Register |
| 1 | 0 | 0 | 0 | 1 | 0 | Write Command Register |
| 1 | 0 | 0 | 1 | 0 | 1 | Illegal |
| 1 | 0 | 0 | 1 | 1 | 0 | Write Request Register |
| 1 | 0 | 1 | 0 | 0 | 1 | Illegal |
| 1 | 0 | 1 | 0 | 1 | 0 | Write Single Mask Register Bit |
| 1 | 0 | 1 | 1 | 0 | 1 | Illegal |
| 1 | 0 | 1 | 1 | 1 | 0 | Write Mode Register |
| 1 | 1 | 0 | 0 | 0 | 1 | Illegal |
| 1 | 1 | 0 | 0 | 1 | 0 | Clear Byte Pointer Flip/Flop |
| 1 | 1 | 0 | 1 | 0 | 1 | Read Temporary Register |
| 1 | 1 | 0 | 1 | 1 | 0 | Master Clear |
| 1 | 1 | 1 | 0 | 0 | 1 | Illegal |
| 1 | 1 | 1 | 0 | 1 | 0 | Illegal |
| 1 | 1 | 1 | 1 | 0 | 1 | Illegal |
| 1 | 1 | 1 | 1 | 1 | 0 | Write All Mask Register Bits |

**Figure 4. Register and Function Addressing.**

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Current Address | Read | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | A0-A7 |
| | | | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | A8-A15 |
| | Base & Current Word Count | Write | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | W0-W7 |
| | | | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | W8-W15 |
| | Current Word Count | Read | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | W0-W7 |
| | | | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | W8-W15 |
| 1 | Base & Current Address | Write | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | A0-A7 |
| | | | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | A8-A15 |
| | Current Address | Read | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | A0-A7 |
| | | | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | A8-A15 |
| | Base & Current Word Count | Write | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | W0-W7 |
| | | | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | W8-W15 |
| | Current Word Count | Read | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | W0-W7 |
| | | | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | W8-W15 |
| 2 | Base & Current Address | Write | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | A0-A7 |
| | | | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | A8-A15 |
| | Current Address | Read | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | A0-A7 |
| | | | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | A8-A15 |
| | Base & Current Word Count | Write | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | W0-W7 |
| | | | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | W8-W15 |
| | Current Word Count | Read | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | W0-W7 |
| | | | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | W8-W15 |
| 3 | Base & Current Address | Write | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | A0-A7 |
| | | | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | A8-A15 |
| | Current Address | Read | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | A0-A7 |
| | | | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | A8-A15 |
| | Base & Current Word Count | Write | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | W0-W7 |
| | | | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | W8-W15 |
| | Current Word Count | Read | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | W0-W7 |
| | | | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | W8-W15 |

**Figure 5. Word Count and Address Register Command Codes.**

## MAXIMUM RATINGS above which useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature Under Bias | −55°C to +125°C |
| VCC with Respect to VSS | −0.5V to +7.0V |
| All Signal Voltages with Respect to VSS | −0.5V to +7.0V |
| Power Dissipation (Package Limitation) | 1.5W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGE

| Part Number | $T_A$ | VCC |
|---|---|---|
| Am9517ADC/PC | 0°C to +70°C | 5.0V ±5% |
| Am9517A-1DC/PC | 0°C to +70°C | 5.0V ±5% |
| Am9517A-4DC/PC | 0°C to +70°C | 5.0V ±5% |
| Am9517ADM | −55°C to +125°C | 5.0V ±10% |

## ELECTRICAL CHARACTERISTICS over operating range (Note 1)

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VOH | Output HIGH Voltage | IOH = −200μA | 2.4 | | | Volts |
| | | IOH = −100μA, (HREQ Only) | 3.3 | | | |
| VOL | Output LOW Voltage | IOL = 3.2mA | | | 0.4 | Volts |
| VIH | Input HIGH Voltage | | 2.0 | | VCC+0.5 | Volts |
| VIL | Input LOW Voltage | | −0.5 | | 0.8 | Volts |
| IIX | Input Load Current | VSS ≤ VI ≤ VCC | −10 | | +10 | μA |
| IOZ | Output Leakage Current | VCC ≤ VO ≤ VSS+.40 | −10 | | +10 | μA |
| ICC | VCC Supply Current | $T_A$ = +25°C | | 65 | 130 | mA |
| | | $T_A$ = 0°C | | 75 | 150 | |
| | | $T_A$ = −55°C | | | 175 | |
| CO | Output Capacitance | fc = 1.0MHz, Inputs = 0V | | 4 | 8 | pF |
| CI | Input Capacitance | | | 8 | 15 | pF |
| CIO | I/O Capacitance | | | 10 | 18 | pF |

**NOTES:**

1. Typical values are for $T_A$ = 25°C, nominal supply voltage and nominal processing parameters.
2. Input timing parameters assume transition times of 20ns or less. Waveform measurement points for both input and output signals are 2.0V for High and 0.8V for Low, unless otherwise noted.
3. Output loading is 1 Standard TTL gate plus 50pF capacitance unless noted otherwise.
4. The new $\overline{IOW}$ or $\overline{MEMW}$ pulse width for normal write will be TCY-100ns and for extended write will be 2TCY-100ns. The net $\overline{IOR}$ or $\overline{MEMR}$ pulse width for normal read will be 2TCY-50ns and for compressed read will be TCY-50ns.
5. TDQ is specified for two different output HIGH levels. TDQ1 is measured at 2.0V. TDQ2 is measured at 3.3V. The value for TDQ2 assumes an external 3.3kΩ pull-up resistor connected from HREQ to VCC.
6. DREQ should be held active until DACK is returned.
7. DREQ and DACK signals may be active high or active low. Timing diagrams assume the active high mode.
8. Output loading on the data bus is 1 Standard TTL gate plus 15pF for the minimum value and 1 Standard TTL gate plus 100pF for the maximum value.
9. Successive read and/or write operations by the external processor to program or examine the controller must be timed to allow at least 600ns for the Am9517A or Am9517A-1 and at least 450ns for the Am9517A-4 as recovery time between active read or write pulses.
10. Parameters are listed in alphabetical order.
11. Pin 5 is an input that should always be at a logic high level. An internal pull-up resistor will establish a logic high when the pin is left floating. Alternatively, pin 5 may be tied to VCC.
12. Signals $\overline{READ}$ and $\overline{WRITE}$ refer to $\overline{IOR}$ and $\overline{MEMW}$ respectively for peripheral-to-memory DMA operations and to $\overline{MEMR}$ and $\overline{IOW}$ respectively for memory-to-peripheral DMA operations.
13. If N wait states are added during the write-to-memory half of a memory-to-memory transfer, this parameter will increase by N (TCY).

## SWITCHING CHARACTERISTICS

**ACTIVE CYCLE** (Notes 2, 3, 10, 11 and 12)

| Parameter | Description | Am9517A Min | Am9517A Max | Am9517A-1 Min | Am9517A-1 Max | Am9517A-4 Min | Am9517A-4 Max | Unit |
|---|---|---|---|---|---|---|---|---|
| TAEL | AEN HIGH from CLK LOW (S1) Delay Time | | 300 | | 300 | | 225 | ns |
| TAET | AEN LOW from CLK HIGH (S1) Delay Time | | 200 | | 200 | | 150 | ns |
| TAFAB | ADR Active to Float Delay from CLK HIGH | | 150 | | 150 | | 120 | ns |
| TAFC | $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ Float from CLK HIGH | | 150 | | 150 | | 120 | ns |
| TAFDB | DB Active to Float Delay from CLK HIGH | | 250 | | 250 | | 190 | ns |
| TAHR | ADR from $\overline{\text{READ}}$ HIGH Hold Time | TCY-100 | | TCY-100 | | TCY-100 | | ns |
| TAHS | DB from ADSTB LOW Hold Time | 50 | | 50 | | 40 | | ns |
| TAHW | ADR from $\overline{\text{WRITE}}$ HIGH Hold Time | TCY-50 | | TCY-50 | | TCY-50 | | ns |
| TAK | DACK Valid from CLK LOW Delay Time | | 280 | | 280 | | 220 | ns |
| | $\overline{\text{EOP}}$ HIGH from CLK HIGH Delay Time | | 250 | | 250 | | 190 | ns |
| | $\overline{\text{EOP}}$ LOW to CLK HIGH Delay Time | | 250 | | 250 | | 190 | ns |
| TASM | ADR Stable from CLK HIGH | | 250 | | 250 | | 190 | ns |
| TASS | DB to ADSTB LOW Setup Time | 100 | | 100 | | 100 | | ns |
| TCH | Clock High Time (Transitions ≤ 10ns) | 120 | | 120 | | 100 | | ns |
| TCL | Clock Low Time (Transitions ≤ 10ns) | 150 | | 150 | | 110 | | ns |
| TCY | CLK Cycle Time | 320 | | 320 | | 250 | | ns |
| TDCL | CLK HIGH to $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ LOW Delay (Note 4) | | 270 | | 270 | | 200 | ns |
| TDCTR | $\overline{\text{READ}}$ HIGH from CLK HIGH (S4) Delay Time (Note 4) | | 270 | | 270 | | 210 | ns |
| TDCTW | $\overline{\text{WRITE}}$ HIGH from CLK HIGH (S4) Delay Time (Note 4) | | 200 | | 200 | | 150 | ns |
| TDQ1 | HREQ Valid from CLK HIGH Delay Time (Note 5) | | 160 | | 160 | | 120 | ns |
| TDQ2 | | | 250 | | 250 | | 190 | ns |
| TEPS | $\overline{\text{EOP}}$ LOW from CLK LOW Setup Time | 60 | | 60 | | 45 | | ns |
| TEPW | $\overline{\text{EOP}}$ Pulse Width | 300 | | 300 | | 225 | | ns |
| TFAAB | ADR Float to Active Delay from CLK HIGH | | 250 | | 250 | | 190 | ns |
| TFAC | $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ Active from CLK HIGH | | 200 | | 200 | | 150 | ns |
| TFADB | DB Float to Active Delay from CLK HIGH | | 300 | | 300 | | 225 | ns |
| THS | HACK valid to CLK HIGH Setup Time | 100 | | 100 | | 75 | | ns |
| TIDH | Input Data from $\overline{\text{MEMR}}$ HIGH Hold Time | 0 | | 0 | | 0 | | ns |
| TIDS | Input Data to $\overline{\text{MEMR}}$ HIGH Setup Time | 250 | | 250 | | 190 | | ns |
| TODH | Output Data from $\overline{\text{MEMW}}$ HIGH Hold Time | 20 | | 20 | | 20 | | ns |
| TODV | Output Data Valid to $\overline{\text{MEMW}}$ HIGH (Note 13) | 200 | | 200 | | 125 | | ns |
| TQS | DREQ to CLK LOW (S1, S4) Setup Time | 120 | | 120 | | 90 | | ns |
| TRH | CLK to READY LOW Hold Time | 20 | | 20 | | 20 | | ns |
| TRS | READY to CLK LOW Setup Time | 100 | | 100 | | 60 | | ns |
| TSTL | ADSTB HIGH from CLK HIGH Delay Time | | 200 | | 200 | | 150 | ns |
| TSTT | ADSTB LOW from CLK HIGH Delay Time | | 140 | | 140 | | 110 | ns |

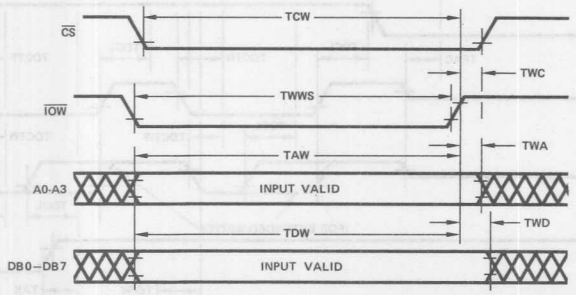
## SWITCHING CHARACTERISTICS

### PROGRAM CONDITION (IDLE CYCLE)

(Notes 2, 3, 10, 11 and 12)

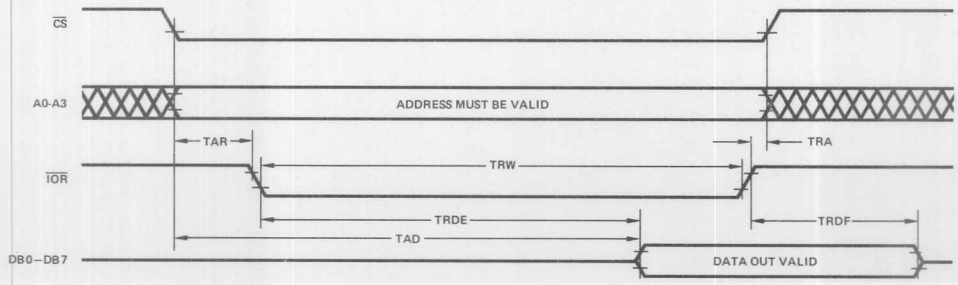
| Parameter | Description | Am9517A Min. | Am9517A Max. | Am9517A-1 Min. | Am9517A-1 Max. | Am9517A-4 Min. | Am9517A-4 Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| TAR | ADR Valid or $\overline{CS}$ LOW to $\overline{READ}$ LOW | 50 | | 50 | | 50 | | ns |
| TAW | ADR Valid to $\overline{WRITE}$ HIGH Setup Time | 200 | | 200 | | 150 | | ns |
| TCW | $\overline{CS}$ LOW to $\overline{WRITE}$ HIGH Setup Time | 200 | | 200 | | 150 | | ns |
| TDW | Data Valid to $\overline{WRITE}$ HIGH Setup Time | 200 | | 200 | | 150 | | ns |
| TRA | ADR or $\overline{CS}$ Hold from $\overline{READ}$ HIGH | 0 | | 0 | | 0 | | ns |
| TRDE | Data Access from $\overline{READ}$ LOW (Note 8) | | 300 | | 200 | | 200 | ns |
| TDRF | DB Float Delay from $\overline{READ}$ HIGH | 20 | 150 | 20 | 100 | 20 | 100 | ns |
| TRSTD | Power Supply HIGH to RESET LOW Setup Time | 500 | | 500 | | 500 | | μs |
| TRSTS | RESET to First $\overline{IOWR}$ | 2 | | 2 | | 2 | | TCY |
| TRSTW | RESET Pulse Width | 300 | | 300 | | 300 | | ns |
| TRW | $\overline{READ}$ Width | 300 | | 300 | | 250 | | ns |
| TWA | ADR from $\overline{WRITE}$ HIGH Hold Time | 20 | | 20 | | 20 | | ns |
| TWC | $\overline{CS}$ HIGH from $\overline{WRITE}$ HIGH Hold Time | 20 | | 20 | | 20 | | ns |
| TWD | Data from $\overline{WRITE}$ HIGH Hold Time | 30 | | 30 | | 30 | | ns |
| TWWS | Write Width | 200 | | 200 | | 200 | | ns |
| TAD | Data Access from ADR Valid, $\overline{CS}$ LOW | | 350 | | 300 | | 300 | ns |

## SWITCHING WAVEFORMS



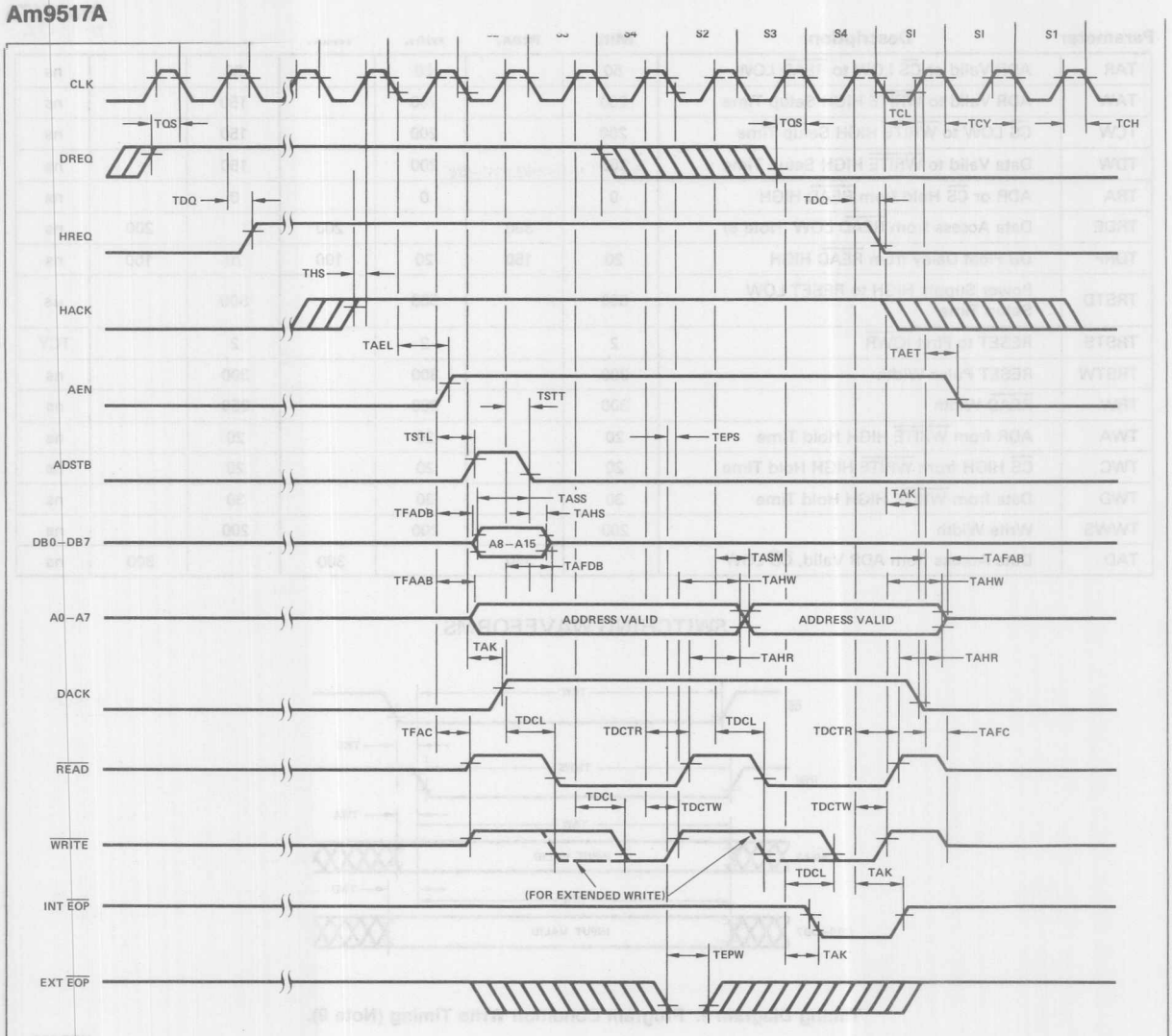

**Timing Diagram 1. Program Condition Write Timing (Note 9).**

MOS-036




**Timing Diagram 2. Program Condition Read Cycle (Note 9).**

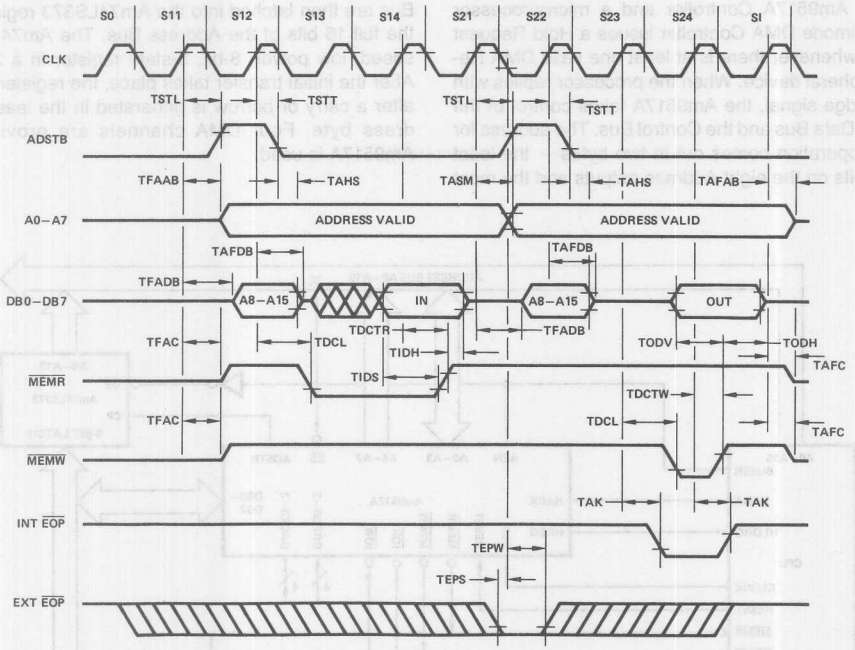
MOS-037




**Timing Diagram 3. Active Cycle Timing Diagram.**

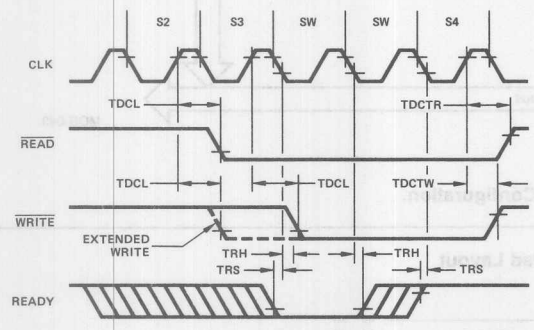
MOS-038

## SWITCHING WAVEFORMS (Cont.)



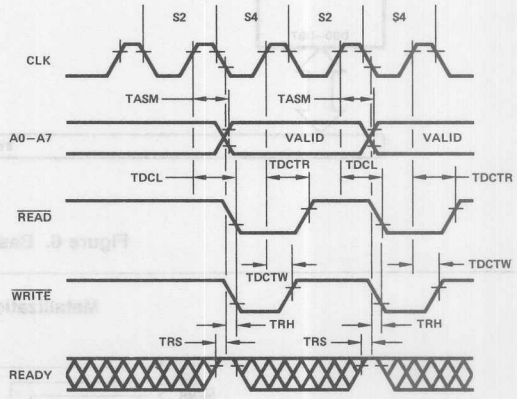

Timing Diagram 4. Memory-to-Memory.

MOS-039



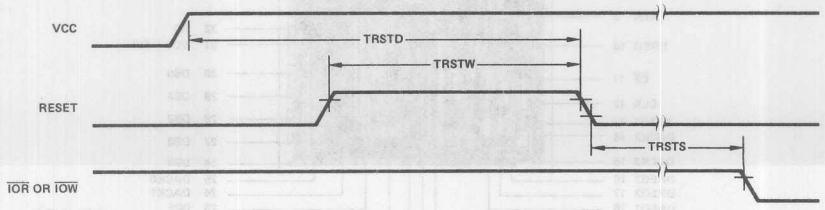

Timing Diagram 5. Ready Timing.

MOS-040




Timing Diagram 6. Compressed Timing.

MOS-041




Timing Diagram 7. Reset Timing.

MOS-042

## APPLICATION INFORMATION

Figure 6 shows a convenient method for configuring a DMA system with the Am9517A Controller and a microprocessor system. The Multimode DMA Controller issues a Hold Request to the processor whenever there is at least one valid DMA Request from a peripheral device. When the processor replies with a Hold Acknowledge signal, the Am9517A takes control of the Address Bus, the Data Bus and the Control Bus. The address for the first transfer operation comes out in two bytes – the least significant eight bits on the eight Address outputs and the most significant eight bits on the Data Bus. The contents of the Data Bus are then latched into the Am74LS373 register to complete the full 16 bits of the Address Bus. The Am74LS373 is a high speed, low power, 8-bit, 3-state register in a 20-pin package. After the initial transfer takes place, the register is updated only after a carry or borrow is generated in the least significant address byte. Four DMA channels are provided when one Am9517A is used.

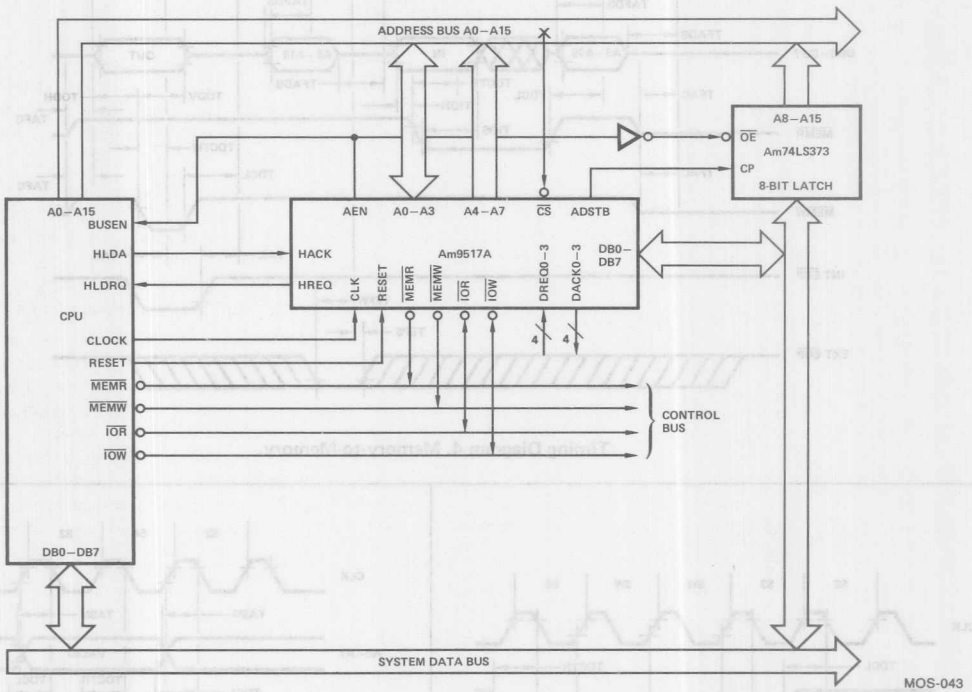
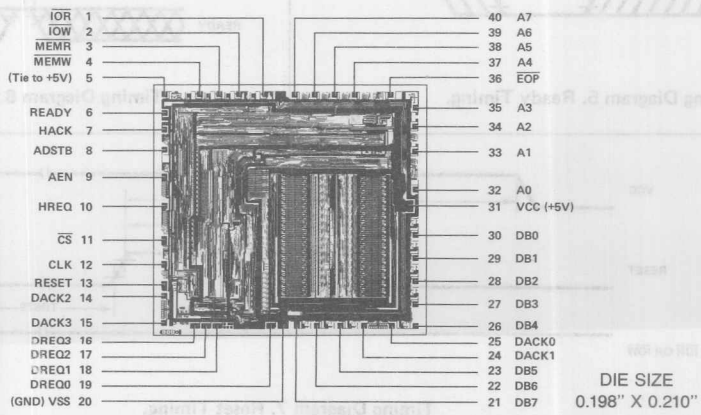



**Figure 6. Basic DMA Configuration.**

### Metallization and Pad Layout



# Am9519A

## Universal Interrupt Controller

### DISTINCTIVE CHARACTERISTICS

- Eight individually maskable interrupt inputs
- Software interrupt request capability
- Fully programmable 1, 2, 3 or 4 byte responses
- Unlimited daisy-chain expansion capability
- Fixed or rotating priority resolution
- Common vector option
- Polled mode option
- Optional automatic clearing of acknowledged interrupts
- Bit set/reset capability for Mask register
- Master Mask bit disables all interrupts
- Pulse-catching interrupt input circuitry
- Polarity control of interrupt inputs and output
- Various timing options including 8085A compatible Am9519A-1
- Single +5V supply
- 100% MIL-STD-883 reliability assurance testing

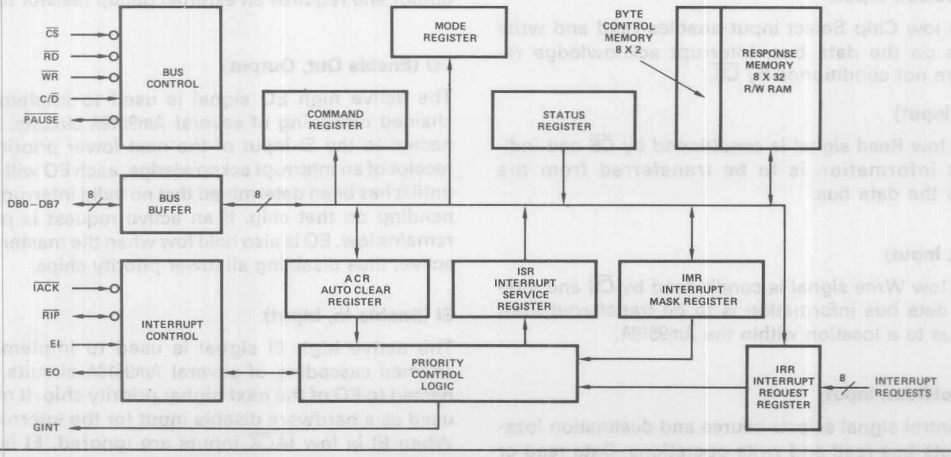
### GENERAL DESCRIPTION

The Am9519A Universal Interrupt Controller is a processor support circuit that provides a powerful interrupt structure to increase the efficiency and versatility of microcomputer-based systems. A single Am9519A manages up to eight maskable interrupt request inputs, resolves priorities and supplies up to four bytes of fully programmable response for each interrupt. It uses a simple expansion structure that allows many units to be cascaded for control of large numbers of interrupts. Several programmable control features are provided to enhance system flexibility and optimization.

The Universal Interrupt Controller is designed with a general purpose interface to facilitate its use with a wide range of digital systems, including most popular 8-bit microprocessors. Since the response bytes are fully programmable, any instruction or vectoring protocol appropriate for the host processor may be used.

When the Am9519A controller receives an unmasked Interrupt Request, it issues a Group Interrupt output to the CPU. When the interrupt is acknowledged, the controller outputs the one-to-four byte response associated with the highest priority unmasked interrupt request. The ability of the CPU to set interrupt requests under software control permits hardware prioritization of software tasks and aids system diagnostic and maintenance procedures.

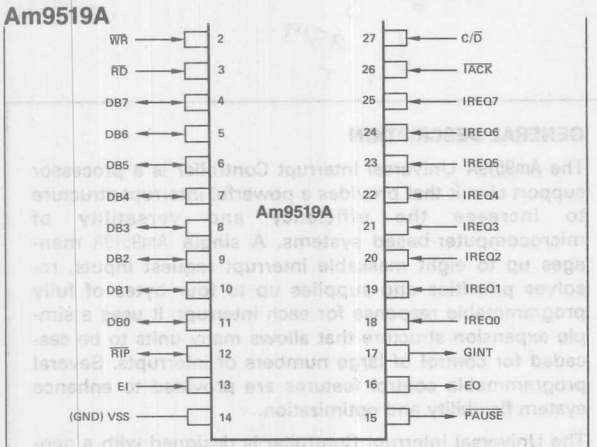
### BLOCK DIAGRAM




### ORDERING INFORMATION

| Package Type | Ambient Temperature | Timing Options | |
|---|---|---|---|
| | | Am9519A | Am9519A-1 |
| Hermetic DIP* | $0°C \leq T_A \leq +70°C$ | AM9519ADC/CC | AM9519A-1DC/CC |
| | $-55°C \leq T_A \leq +125°C$ | AM9519ADM | |
| Molded DIP | $0°C \leq T_A \leq +70°C$ | AM9519APC | AM9519A-1PC |

*DC = Side-Brazed Ceramic CC = Cerdip




Top View

Pin 1 is marked for orientation.

MOS-019

## INTERFACE SIGNAL DESCRIPTION

**VCC:** +5 Volt Power Supply
**VSS:** Ground

**DB0 – DB7 (Data Bus, Input/Output)**

The eight bidirectional data bus signals are used to transfer information between the Am9519A and the system data bus. The direction of transfer is controlled by the $\overline{IACK}$, $\overline{WR}$ and $\overline{RD}$ input signals. Programming and control information are written into the device; status and response data are output by it.

**$\overline{CS}$ (Chip Select, Input)**

The active low Chip Select input enables read and write operations on the data bus. Interrupt acknowledge responses are not conditioned by $\overline{CS}$.

**$\overline{RD}$ (Read, Input)**

The active low Read signal is conditioned by $\overline{CS}$ and indicates that information is to be transferred from the Am9519A to the data bus.

**$\overline{WR}$ (Write, Input)**

The active low Write signal is conditioned by $\overline{CS}$ and indicates that data bus information is to be transferred from the data bus to a location within the Am9519A.

**C/$\overline{D}$ (Control/Data, Input)**

The C/$\overline{D}$ control signal selects source and destination locations for data bus read and write operations. Data read or write transfers are made to or from preselected internal registers or memory locations. Control write operations load the command register and control read operations output the status register.

**IREQ0 – IREQ7 (Interrupt Request, Input)**

The Interrupt Request signals are used by external devices to indicate that service by the host CPU is desired. IREQ inputs are accepted asynchronously and they may be programmed for either a high-to-low or low-to-high initiate another request.

**$\overline{RIP}$ (Response In Process, Input/Output)**

Response In Process is a bidirectional signal used when two or more Am9519A circuits are cascaded. It permits multibyte response transfers to be completed without interference from higher priority interrupts. An Am9519A that is responding to an acknowledged interrupt will treat $\overline{RIP}$ as an output and hold it low until the acknowledge response is finished. An Am9519A without an acknowledged interrupt will treat $\overline{RIP}$ as an input and will ignore $\overline{IACK}$ pulses as long as $\overline{RIP}$ is low. The $\overline{RIP}$ output is open drain and requires an external pullup resistor to VCC.

**$\overline{IACK}$ (Interrupt Acknowledge, Input)**

The active low Interrupt Acknowledge line indicates that the external system is asking for interrupt response information. Depending on the programmed state of the Am9519A, it will accept 1, 2, 3 or 4 $\overline{IACK}$ pulses; one response byte is transferred per pulse. The first $\overline{IACK}$ pulse causes selection of the highest priority unmasked pending interrupt request and generates a $\overline{RIP}$ output signal.

**$\overline{PAUSE}$ (Pause, Output)**

The active-low Pause signal is used to coordinate interrupt responses with data bus and control timing. Pause goes low when the first $\overline{IACK}$ is received and remains low until $\overline{RIP}$ goes low. The external system can use Pause to stretch the acknowledge cycle and allow the control timing to automatically adjust to the actual priority resolution delays in the interrupt system. Second, third and fourth response bytes do not cause Pause to go low. Pause is an open drain output and requires an external pullup resistor to VCC.

**EO (Enable Out, Output)**

The active high EO signal is used to implement daisy-chained cascading of several Am9519A circuits. EO is connected to the EI input of the next lower priority chip. On receipt of an interrupt acknowledge, each EO will go inactive until it has been determined that no valid interrupt request is pending on that chip. If an active request is present, EO remains low. EO is also held low when the master mask bit is active, thus disabling all lower priority chips.

**EI (Enable In, Input)**

The active high EI signal is used to implement daisy-chained cascading of several Am9519A circuits. EI is connected to EO of the next higher priority chip. It may also be used as a hardware disable input for the interrupt system. When EI is low $\overline{IACK}$ inputs are ignored. EI is internally pulled up to VCC so that no external pullup is needed when EI is not used.

**GINT (Group Interrupt, Output)**

The Group Interrupt output signal indicates that at least one unmasked interrupt request is pending. It may be programmed for active high or active low polarity. When active low, the output is open drain and requires an external pull up resistor to VCC.

## REGISTER DESCRIPTION

**Interrupt Request Register (IRR):** The 8-bit IRR is used to store pending interrupt requests. A bit in the IRR is set whenever the corresponding IREQ input goes active. Bits may also be set under program control from the CPU, thus permitting software generated interrupts. IRR bits may be cleared under program control. An IRR bit is automatically cleared when its interrupt is acknowledged. All IRR bits are cleared by a reset function.

**Interrupt Service Register (ISR):** The 8-bit ISR contains one bit for each IREQ input. It is used to indicate that a pending interrupt has been acknowledged and to mask all lower priority interrupts. When a bit is set by the acknowledge logic in the ISR, the corresponding IRR bit is cleared. If an acknowledged interrupt is not programmed to be automatically cleared, its ISR bit must be cleared by the CPU under program control when it is desired to permit interrupts from lower priority devices. When the interrupt is programmed for automatic clearing, the ISR bit is automatically reset during the acknowledge sequence. All ISR bits are cleared by a reset function.

**Interrupt Mask Register (IMR):** The 8-bit IMR is used to enable or disable the individual interrupt inputs. The IMR bits correspond to the IREQ inputs and all eight may be loaded, set or cleared in parallel under program control. In addition, individual IMR bits may be set or cleared by the CPU. A reset function will set all eight mask bits, disabling all requests. A mask bit that is set does not disable the IRR, and an IREQ that arrives while a corresponding mask bit is set will cause an interrupt later when the mask bit is cleared. Only unmasked interrupt inputs can generate a Group Interrupt output.

**Response Memory:** An 8 x 32 read/write response memory is included in the Am9519A. It is used to store up to four bytes of response information for each of the eight interrupt request inputs. All bits in the memory are programmable, allowing any desired vector, opcode, instruction or other data to be entered. The Am9519A transfers the interrupt response information for the highest priority unmasked interrupt from the memory to the data bus when the $\overline{IACK}$ input is active.

**Auto Clear Register:** The 8-bit Auto Clear register contains one bit for each IREQ input and specifies the operating mode for each of the ISR bits. When an auto clear bit is off, the corresponding ISR bit is set when that interrupt is acknowledged and is cleared by software command. When an auto clear bit is on, the corresponding ISR bit is cleared by the hardware at the end of the acknowledge sequence. A reset function clears all auto clear bits.

**Status Register:** The 8-bit Status register contains information concerning the internal state of the chip. It is especially useful when operating in the polled mode in order to identify interrupting devices. Figure 1 shows the status register bit assignments. The polarity of the GINT bit 7 is not affected by the GINT polarity control (Mode bit status register bit assignments. Bits S0-S2 are set asynchronously to a status register read operation. It is recommended to read the register twice and to compare the binary vectors for equality prior to the proceeding with device service in polled mode. The polarity of the GINT bit 7 is not affected by the GINT polarity control (Mode bit 3). The Status register is read by executing a read operation ($\overline{CS} = 0, RS = 0$) with the control location selected ($C/\overline{D} = 1$).

**Mode Register:** The 8-bit Mode register controls the operating options of the Am9519A. Figure 2 shows the bit assignments for the Mode register. The five low order mode bits (0 through 4) are loaded in parallel by command. Bits 5, 6 and 7 are controlled by separate commands. (See Figure 4.) The Mode register cannot be read out directly to the data bus, but Mode bits 0, 2 and 7 are available as part of the Status register.

**Command Register:** The 8-bit Command register stores the last command entered. Depending upon the command opcode, it may initiate internal actions or precondition the part for subsequent data bus transfers. The Command register is loaded by executing a write operation ($\overline{WR} = 0$) with the control location selected ($C/\overline{D} = 1$), as shown in Figure 3.

**Byte Count Register:** The length in bytes of the response associated with each interrupt is independently programmed so that different interrupts may have different length responses. The byte count for each response is stored in eight 2-bit Byte Count registers. For a given interrupt the Am9519A will expect to receive a number of $\overline{IACK}$ pulses that equals the corresponding byte count, and will hold $\overline{RIP}$ low until the count is satisfied.

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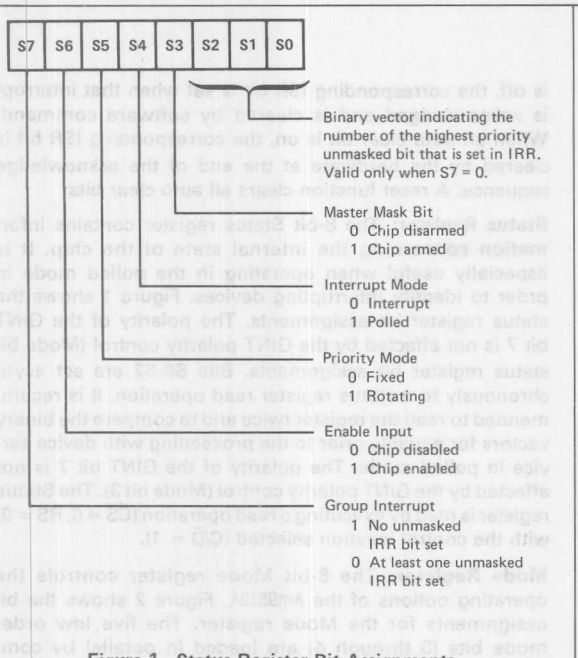



Figure 1. Status Register Bit Assignments. MOS-025

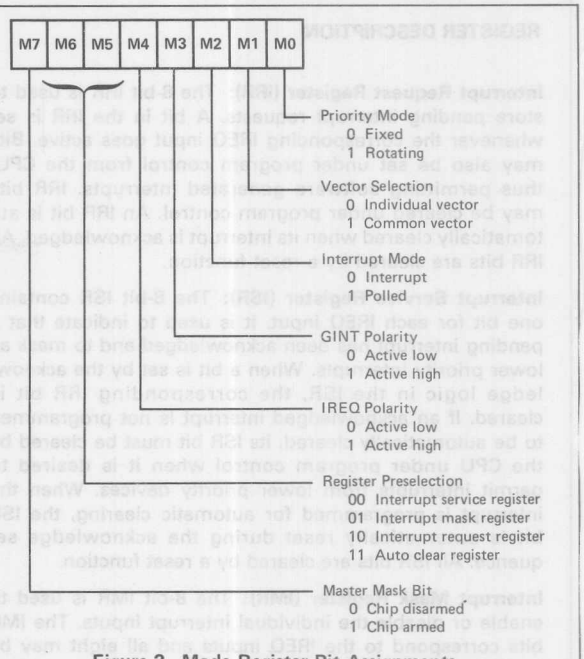



Figure 2. Mode Register Bit Assignments. MOS-026

## FUNCTIONAL DESCRIPTION

Interrupts are used to improve system throughput and response time by eliminating heavy dependence on software polling procedures. Interrupts allow external devices to asynchronously modify the instruction sequence of a program being executed. In systems with multiple interrupts, vectoring can further improve performance by allowing direct identification of the interrupting device and its associated service routine. The Am9519A Universal Interrupt Controller contains, on one chip, all of the circuitry necessary to detect, prioritize and manage eight vectored interrupts. It includes many options and operating modes that permit the design of sophisticated interrupt systems.

### Reset

The reset function is accomplished by software command or automatically during power-up. The reset command may be issued by the CPU at any time. Internal power up circuitry is triggered when VCC reaches a predetermined threshold, causing a brief internal reset pulse. In both cases, the resulting internal state of the machine is that all registers are cleared except the Mask register which is set. Thus no Group Interrupt will be generated and no interrupt requests will be recognized. The response memory and Byte Count registers are not affected by reset. Their contents after power-up are unpredictable and must be established by the host CPU during initialization.

### Operating Sequence

A brief description of a typical sequence of events in an operating interrupt system will illustrate the general interactions among the host CPU, the interrupt controller and the interrupting peripheral.

1. The Am9519A controller is initialized by the CPU in order to customize its configuration and operation for the application at hand. Both the controller and the CPU are then enabled to accept interrupts.
2. One (or more) of the interrupt request inputs to the controller becomes active indicating that peripheral equipment is asking for service. The controller asynchronously accepts and latches the request(s).
3. If the request is masked, no further action takes place. If the request is not masked, a Group Interrupt output is generated by the controller.
4. The GINT signal is recognized by the CPU which normally will complete the execution of the current instruction, insert an interrupt acknowledge sequence into its instruction execution stream, and disable its internal interrupt structure. The controller expects to receive one or more $\overline{IACK}$ signals from the CPU during the acknowledge sequence.
5. When the controller receives the $\overline{IACK}$ signal, it brings $\overline{PAUSE}$ low and selects the highest priority unmasked pending request. When selection is complete, the $\overline{RIP}$ output is brought low and the first byte in the response memory associated with the selected request is output on the data bus. $\overline{PAUSE}$ stays low until RIP goes low. $\overline{RIP}$ stays low until the last byte of the response has been transferred.
6. During the acknowledge sequence, the IRR bit corresponding to the selected request is automatically cleared, and the corresponding ISR bit is set. When the ISR bit is set, the Group Interrupt output is disabled until a higher priority request arrives or the ISR bit is cleared. The ISR bit will be cleared by either hardware or software.
7. If a higher priority request arrives while the current request is being serviced, GINT will be output by the controller, but will be recognized and acknowledged only if the CPU has its interrupt input enabled. If acknowledged, the corresponding higher priority ISR bit will be set and the requests nested.

### Information Transfers

Figure 3 shows the control signal configurations for all information transfer operations between the Am9519 and the data bus. The following conventions are assumed: $\overline{RD}$ and $\overline{WR}$ active are mutually exclusive; $\overline{RD}$, $\overline{WR}$ and C/$\overline{D}$ have no meaning unless $\overline{CS}$ is low; active $\overline{IACK}$ pulses occur only when $\overline{CS}$ is high.

For reading, the Status register is selected directly by the C/$\overline{D}$ control input. Other internal registers are read by preselecting the desired register with mode bits 5 and 6, and then executing a data read. The response memory can be read only with $\overline{IACK}$ pulses. For writing, the Command register is selected directly by the C/$\overline{D}$ control input. The Mask and Auto Clear registers are loaded following specific commands to that effect. To load each level of the response memory, the response preselect command is issued to select the desired level. An appropriate number of data write operations are then executed to load that level.

| CONTROL INPUT | | | | | DATA BUS OPERATION |
|---|---|---|---|---|---|
| $\overline{CS}$ | C/$\overline{D}$ | $\overline{RD}$ | $\overline{WR}$ | $\overline{IACK}$ | |
| 0 | 0 | 0 | 1 | 1 | Transfer contents of preselected data register to data bus |
| 0 | 0 | 1 | 0 | 1 | Transfer contents of data bus to preselected data register |
| 0 | 1 | 0 | 1 | 1 | Transfer contents of status register to data bus |
| 0 | 1 | 1 | 0 | 1 | Transfer contents of data bus to command register |
| 1 | X | X | X | 0 | Transfer contents of selected response memory location to data bus |
| 1 | X | X | X | 1 | No information transferred |

Figure 3. Summary of Data Bus Transfers.

The Pause output may be used by the host CPU to ensure that proper timing relationships are maintained with the Am9519A when $\overline{IACK}$ is active. The $\overline{IACK}$ pulse width required depends on several variables, including: operating temperature, internal logic delays, number of interrupt controllers chained together, and the priority level of the interrupt being acknowledged. When delays in these variables combine to delay selection of a request following the falling edge of the first $\overline{IACK}$, the Pause output may be used to extend the $\overline{IACK}$ pulse, if necessary. Pause will remain low until a request has been selected, as indicated by the falling edge of $\overline{RIP}$. Typically, the internal interrupt selection process is quite fast, especially for systems with a single Am9519A and Pause will consequently remain low for only a very brief interval and will not cause extension of the $\overline{IACK}$ timing.

### Operating Options

The Mode register specifies the various combinations of operating options that may be selected by the CPU. It is cleared by power-up or by a reset command.

Mode bit 0 specifies the rotating/fixed priority mode (see Figure 2). In the fixed mode, priority is assigned to the request inputs based upon their physical location at the chip interface, with IREQ0 the highest and IREQ7 the lowest. In the rotating mode, relative priority is the same as for the fixed mode and the most recently serviced request is assigned the lowest priority. In the fixed mode, a lower priority request might never receive service if enough higher priority requests are active. In the rotating mode, any request will receive service within a maximum of seven other service cycles no matter what pattern the request inputs follow.

Mode bit 1 selects the individual/common vector option. Individual vectoring provides a unique location in the response memory for each interrupt request. The common vector option always supplies the response associated with IREQ0 no matter which request is being acknowledged.

Mode bit 2 specifies interrupt or polled operation. In the polled mode the Group Interrupt output is disabled. The CPU may read the Status register to determine if a request is pending. Since $\overline{IACK}$ pulses are not normally supplied in polled mode, the IRR bit is not automatically cleared, but may be cleared by command. With no $\overline{IACK}$ input the ISR and the response memory are not used. An Am9519A in the polled mode has EI connected to EO so that in multichip interrupt systems the polled chip is functionally removed from the priority hierarchy.

Mode bit 3 specifies the sense of the GINT output. When active high polarity is selected the output is a two-state configuration. For active low polarity, the output is open drain and requires an external pull-up resistor to provide the high logic level. The open drain output allows wired-or configurations with other similar output signals.

Mode bit 4 specifies the sense of the IREQ inputs. When active low polarity is selected, the IRR responds to falling edges on the request inputs. When active high is selected, the IRR responds to rising edges.

Mode bits 5 and 6 specify the register that will be read on subsequent data read operations (C/$\overline{D}$ = 0, $\overline{RD}$ = 0). This preselection remains valid until changed by a reset or a command.

Mode bit 7 is the master mask bit that disables all request inputs. It is used to disable all interrupts without modifying the IMR so that the previous IMR contents are valid when interrupts are re-enabled. When the master mask bit is low, it causes the EO line to remain disabled (low). Thus, for multiple-chip interrupt systems, one master mask bit can disable the whole interrupt structure. Alternatively, portions of the structure may be disabled. The state of the master mask bit is available as bit S3 of the Status register.

### Programming

After reset, the Am9519A must be initialized by the CPU in order to perform useful work. At a minimum, the master mask bit and at least one of the IMR bits should be enabled. If vectoring is to be used, the response memory must be loaded; if not, the mode must be changed to a non-vectored configuration. Normally, the first step will be to modify the Mode register and the Auto clear register in order to establish the configuraton desired for the application. Then the response memory and byte count will be loaded for those request levels that will be in use. Finally, the master mask bit and at least portions of the IMR will be enabled to allow interrupt processing to proceed.

in Figure 4. An "X" entry in the table indicates a "don't care" state. All commands are entered by directly loading the Command register as shown in Figure 3 (C/$\overline{D}$ = 1, $\overline{WR}$ = 0). Figure 5 shows the coding assignments for the Byte Count registers. A detailed description of each command is contained in the Am9519A Application Note AMPUB-071.

| | | |
|---|---|---|
| 0 | 1 | 2 |
| 1 | 0 | 3 |
| 1 | 1 | 4 |

Figure 5. Byte Count Coding.

| COMMAND CODE | | | | | | | | COMMAND DESCRIPTION |
|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| 0 | 0 | 0 | 1 | 0 | X | X | X | Clear all IRR and all IMR bits |
| 0 | 0 | 0 | 1 | 1 | B2 | B1 | B0 | Clear IRR and IMR bit specified by B2, B1, B0 |
| 0 | 0 | 1 | 0 | 0 | X | X | X | Clear all IMR bits |
| 0 | 0 | 1 | 0 | 1 | B2 | B1 | B0 | Clear IMR bit specified by B2, B1, B0 |
| 0 | 0 | 1 | 1 | 0 | X | X | X | Set all IMR bits |
| 0 | 0 | 1 | 1 | 1 | B2 | B1 | B0 | Set IMR bit specified by B2, B1, B0 |
| 0 | 1 | 0 | 0 | 0 | X | X | X | Clear all IRR bits |
| 0 | 1 | 0 | 0 | 1 | B2 | B1 | B0 | Clear IRR bit specified by B2, B1, B0 |
| 0 | 1 | 0 | 1 | 0 | X | X | X | Set all IRR bits |
| 0 | 1 | 0 | 1 | 1 | B2 | B1 | B0 | Set IRR bit specified by B2, B1, B0 |
| 0 | 1 | 1 | 0 | X | X | X | X | Clear highest priority ISR bit |
| 0 | 1 | 1 | 1 | 0 | X | X | X | Clear all ISR bits |
| 0 | 1 | 1 | 1 | 1 | B2 | B1 | B0 | Clear ISR bit specified by B2, B1, B0 |
| 1 | 0 | 0 | M4 | M3 | M2 | M1 | M0 | Load Mode register bits 0–4 with specified pattern |
| 1 | 0 | 1 | 0 | M6 | M5 | 0 | 0 | Load Mode register bits 5, 6 with specified pattern |
| 1 | 0 | 1 | 0 | M6 | M5 | 0 | 1 | Load Mode register bits 5, 6 and set mode bit 7 |
| 1 | 0 | 1 | 0 | M6 | M5 | 1 | 0 | Load Mode register bits 5, 6 and clear mode bit 7 |
| 1 | 0 | 1 | 1 | X | X | X | X | Preselect IMR for subsequent loading from data bus |
| 1 | 1 | 0 | 0 | X | X | X | X | Preselect Auto Clear register for subsequent loading from data bus |
| 1 | 1 | 1 | BY1 | BY0 | L2 | L1 | L0 | Load BY1, BY0 into byte count register and preselect response memory level specified by L2, L1, L0 for subsequent loading from data bus |

Figure 4. Am9519A Command Summary.

| | |
|---|---|
| Ambient Temperature Under Bias | −55°C to +125°C |
| VCC with Respect to VSS | −0.5V to +7.0V |
| All Signal Voltages with Respect to VSS | −0.5V to +7.0V |
| Power Dissipation (Package Limitation) | 1.5W |

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGE

| Part Number | Ambient Temperature | VCC | VSS |
|---|---|---|---|
| Am9519ADC/CC<br>Am9519A-1DC | $0°C \leq T_A \leq +70°C$ | +5.0V ±5% | 0V |
| Am9519ADM | $-55°C \leq T_A \leq +125°C$ | +5.0V ±10% | 0V |

## ELECTRICAL CHARACTERISTICS Over Operating Range (Note 1)

| Parameter | Description | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| VOH | Output High Voltage (Note 12) | IOH = −200μA | | 2.4 | | | Volts |
| | | IOH = −100μA (EO only) | | 2.4 | | | |
| VOL | Output Low Voltage | IOL = 3.2mA | | | | 0.4 | Volts |
| | | IOL = 1.0mA (EO only) | | | | 0.4 | |
| VIH | Input High Voltage | | | 2.0 | | VCC | Volts |
| VIL | Input Low Voltage | | | −0.5 | | 0.8 | Volts |
| IIX | Input Load Current | $VSS \leq VIN \leq VCC$ | EI Input | −60 | | 10 | μA |
| | | | Other Inputs | −10 | | 10 | |
| IOZ | Output Leakage Current | $VSS \leq VOUT \leq VCC$, Output off | | −10 | | 10 | μA |
| ICC | VCC Supply Current | $T_A = +25°C$ | | | 80 | 125 | mA |
| | | $T_A = 0°C$ | | | 100 | 145 | |
| CO | Output Capacitance | fc = 1.0MHz | | | | 15 | pF |
| CI | Input Capacitance | $T_A = 25°C$ | | | | 10 | |
| CIO | I/O Capacitance | All pins at 0V | | | | 20 | |

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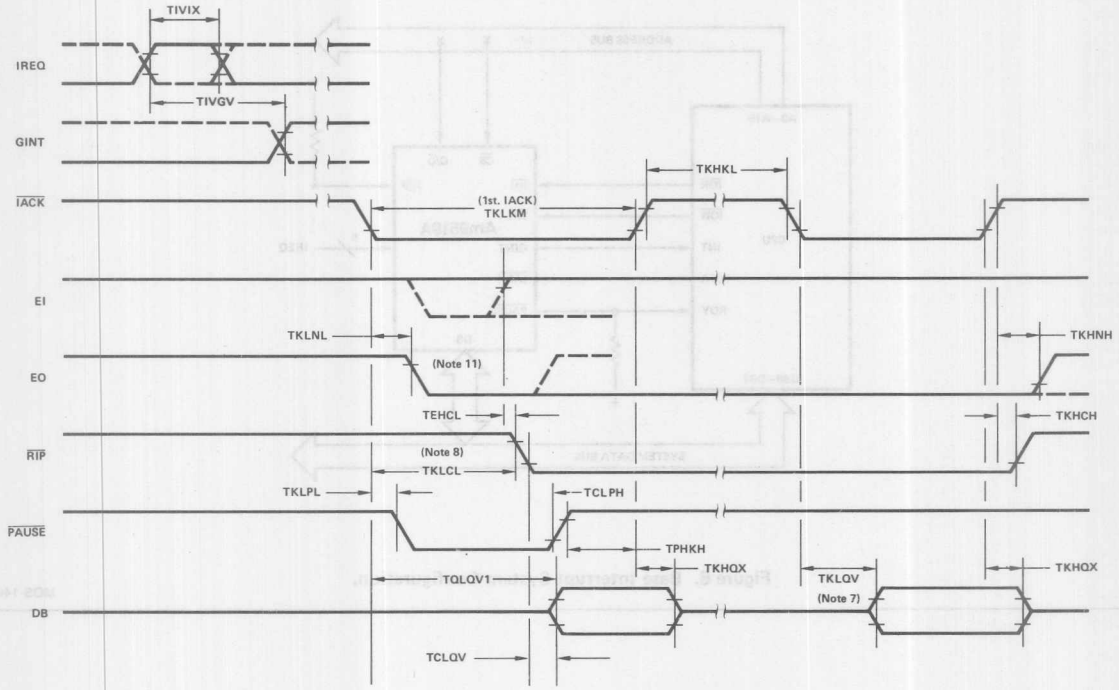
## SWITCHING CHARACTERISTICS Over Operating Range (Notes 2, 3, 4, 5)

| Parameters | Description | Am9519A Min | Am9519A Max | Am9519A-1 Min | Am9519A-1 Max | Units |
|---|---|---|---|---|---|---|
| TAVRL | C/$\overline{D}$ Valid and $\overline{CS}$ LOW to Read LOW | 0 | | 0 | | ns |
| TAVWL | C/$\overline{D}$ Valid and $\overline{CS}$ LOW to Write LOW | 0 | | 0 | | ns |
| TCLPH | $\overline{RIP}$ LOW to $\overline{PAUSE}$ HIGH (Note 6) | 75 | 300 | 75 | 300 | ns |
| TCLQV | $\overline{RIP}$ LOW to Data Out Valid (Note 7) | | 50 | | 40 | ns |
| TDVWH | Data In Valid to Write HIGH | 250 | | 200 | | ns |
| TEHCL | Enable in HIGH to $\overline{RIP}$ LOW (Notes 8, 9) | 30 | 300 | 30 | 300 | ns |
| TIVGV | Interrupt Request Valid to Group Interrupt Valid | | 800 | | 650 | ns |
| TIVIX | Interrupt Request Valid to Interrupt Request Don't Care (IREQ Pulse Duration) | 250 | | 250 | | ns |
| TKHCH | $\overline{IACK}$ HIGH to $\overline{RIP}$ HIGH (Note 8) | | 400 | | 350 | ns |
| TKHKL | $\overline{IACK}$ HIGH to $\overline{IACK}$ LOW ($\overline{IACK}$ Recovery) | | 500 | | 500 | ns |
| TKHNH | $\overline{IACK}$ HIGH to EO HIGH (Notes 10, 11) | | 800 | | 700 | ns |
| TKHQX | $\overline{IACK}$ HIGH to Data Out Invalid | 20 | 200 | 20 | 100 | ns |
| TKLCL | $\overline{IACK}$ LOW to $\overline{RIP}$ LOW (Note 8) | 75 | 600 | 75 | 450 | ns |
| TKLKH | $\overline{IACK}$ LOW to $\overline{IACK}$ HIGH (1st IACK) | 975 | | 800 | | ns |
| TKLNL | $\overline{IACK}$ LOW to EO LOW (Notes 10, 11) | | 125 | | 100 | ns |
| TKLPL | $\overline{IACK}$ LOW to $\overline{PAUSE}$ LOW | 25 | 175 | 25 | 125 | ns |
| TKLQV | $\overline{IACK}$ LOW to Data Out Valid (Note 7) | 25 | 300 | 25 | 200 | ns |
| TKLQV1 | 1st $\overline{IACK}$ LOW to Data Out Valid | 75 | 650 | 75 | 490 | ns |
| TPHKH | $\overline{PAUSE}$ HIGH to $\overline{IACK}$ HIGH | 0 | | 0 | | ns |
| TRHAX | Read HIGH to C/$\overline{D}$ and $\overline{CS}$ Don't Care | 0 | | 0 | | ns |
| TRHQX | Read HIGH to Data Out Invalid | 20 | 200 | 20 | 100 | ns |
| TRLQV | Read LOW to Data Out Valid | | 300 | | 200 | ns |
| TRLQX | Read LOW to Data Out Unknown | 50 | | 50 | | ns |
| TRLRH | Read LOW to Read HIGH ($\overline{RD}$ Pulse Duration) | 300 | | 250 | | ns |
| TWHAX | Write HIGH to C/$\overline{D}$ and $\overline{CS}$ Don't Care | 0 | | 0 | | ns |
| TWHDX | Write HIGH to Data In Don't Care | 0 | | 0 | | ns |
| TWHRW | Write HIGH to Read or Write LOW (Write Recovery) | 600 | | 400 | | ns |
| TWLWH | Write LOW to Write HIGH ($\overline{WR}$ Pulse Duration) | 300 | | 250 | | ns |

**NOTES:**

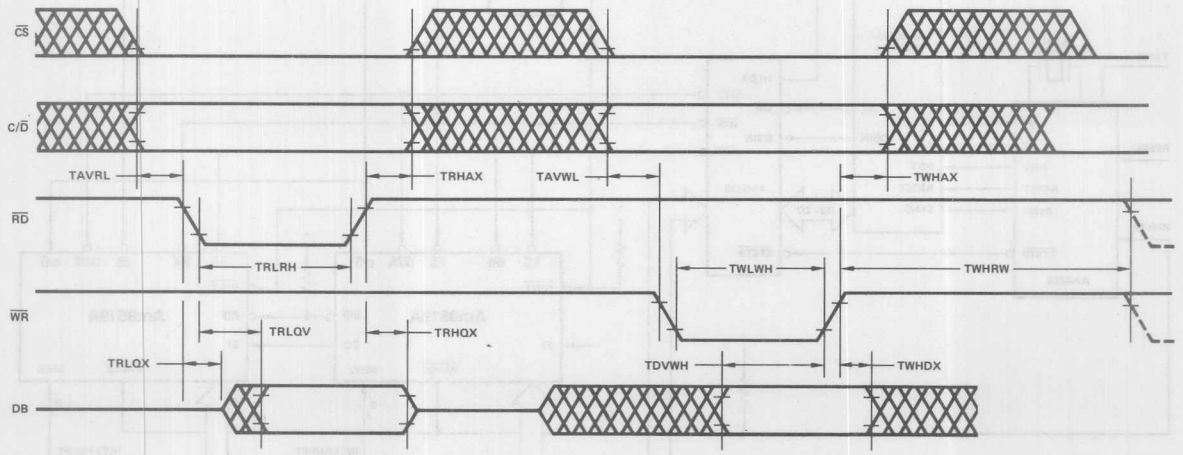
1. Typical values for $T_A$ = 25°C, nominal supply voltage and nominal processing parameters.
2. Test conditions assume transition times of 20ns or less, timing reference levels of 0.8V and 2.0V and output loading of one TTL gate plus 100pF, unless otherwise noted.
3. Transition abbreviations used for the switching parameter symbols include: H = High, L = Low, V = Valid, X = unknown or don't care, Z = high impedance.
4. Signal abbreviations used for the switching parameter symbols include: R = Read, W = Write, Q = Data Out, D = Data In, A = Address ($\overline{CS}$ and C/$\overline{D}$), K = Interrupt Acknowledge, N = Enable Out, E = Enable In, P = Pause, C = $\overline{RIP}$.
5. Switching parameters are listed in alphabetical order.
6. During the first $\overline{IACK}$ pulse, $\overline{PAUSE}$ will be low long enough to allow for priority resolution and will not go high until after RIP goes low (TCLPH).
7. TKLQV applies only to second, third and fourth $\overline{IACK}$ pulses while $\overline{RIP}$ is low. During the first $\overline{IACK}$ pulse, Data Out will be valid following the falling edge of $\overline{RIP}$ (TCLQV).
8. $\overline{RIP}$ is pulled low to indicate that an interrupt request has been selected. $\overline{RIP}$ cannot be pulled low until EI is high following an internal delay. TKLCL will govern the falling edge of $\overline{RIP}$ when EI is always high or is high early in the acknowledge cycle. TEHCL will govern when EI goes high later in the cycle. The rising edge of EI will be determined by the length of the preceding priority resolution chain. $\overline{RIP}$ remains low until after the rising edge of the $\overline{IACK}$ pulse that transfers the last response byte for the selected IREQ.
9. Test conditions for the EI line assume timing reference levels of 0.8V and 2.0V with transition times of 10ns or less.
10. Test conditions for the EO line assume output loading of two LS TTL gates plus 30pF and timing reference levels of 0.8V and 2.0V. Since EO normally only drives EI of another Am9519A, higher speed operation can be specified with this more realistic test condition.
11. The arrival of $\overline{IACK}$ will cause EO to go low, disabling additional circuits that may be connected to EO. If no valid interrupt is pending, EO will return high when EI is high. If a pending request is selected. EO will stay low until after the last $\overline{IACK}$ pulse for that interrupt is complete and $\overline{RIP}$ goes high.
12. VOH specifications do not apply to $\overline{RIP}$ or to $\overline{GINT}$ when active-low. These outputs are open-drain and VOH levels will be determined by external circuitry.

## SWITCHING WAVEFORMS




MOS-144

Interrupt Operations




MOS-145

Data Bus Transfers

7

## APPLICATIONS

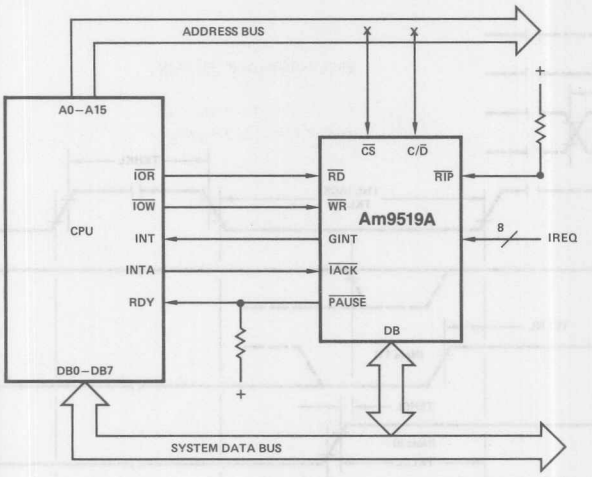



Figure 6. Base Interrupt System Configuration.

MOS-146

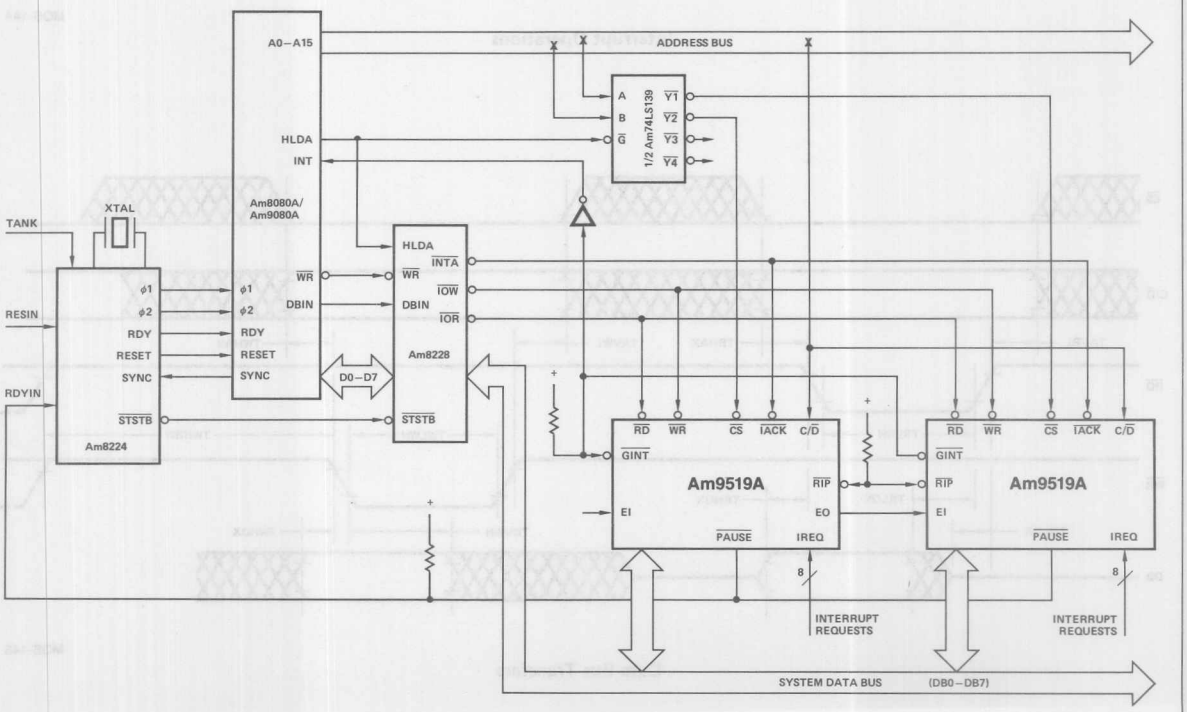



Figure 7. Expanded Interrupt System Configuration.

MOS-147

# Bipolar Support Products for MOS Microprocessor and Memory Systems

## NUMERICAL INDEX


| | | Page |
|---|---|---|
| Am3212 | 8-Bit Input/Output Port | 8-58 |
| Am3216 | 4-Bit Bidirectional Bus Driver | 8-65 |
| Am3226 | 4-Bit Bidirectional Bus Driver | 8-65 |
| Am3448A | IEEE-488 Quad Bidirectional Bus Transceiver | 8-1 |
| AmZ8103 | Octal Bus Transceiver (Inverting) | 8-6 |
| AmZ8104 | Octal Bus Transceiver (Non-Inverting) | 8-6 |
| AmZ8107 | Octal Bus Transceiver (Inverting) | 8-12 |
| AmZ8108 | Octal Bus Transceiver (Non-Inverting) | 8-12 |
| AmZ8120 | Octal Register | 8-14 |
| AmZ8121 | 8-Bit Comparator | 8-18 |
| AmZ8127 | Clock Generator | 8-22 |
| AmZ8133 | Octal Latch (Inverting) | 8-23 |
| AmZ8136 | 8-Bit Decoder w/Storage | 8-28 |
| AmZ8140 | Octal 3-State Buffer (Inverting ) | 8-32 |
| AmZ8144 | Octal 3-State Buffer (Non-Inverting) | 8-32 |
| AmZ8148 | Address Decoder w/Acknowledge | 8-36 |
| AmZ8160 | Error Detection and Correction Unit | 8-41 |
| AmZ8161 | EDC Bus Buffer (Inverting to Bus) | 8-49 |
| AmZ8162 | EDC Bus Buffer (Non-Inverting to Bus) | 8-49 |
| AmZ8163 | Refresh and EDC Controller | 8-50 |
| AmZ8164 | Dynamic Memory Controller | 8-51 |
| AmZ8165 | Dynamic RAM Driver (Inverting) | 8-52 |
| AmZ8166 | Dynamic RAM Driver (Non-Inverting) | 8-52 |
| AmZ8173 | Octal Latch (Non-Inverting) | 8-23 |
| Am8212 | 8-Bit Input/Output Port | 8-58 |
| Am8216 | 4-Bit Bidirectional Bus Driver (Non-Inverting) | 8-65 |
| Am8224 | Clock Generator | 8-70 |
| Am8226 | 4-Bit Bidirectional Bus Driver (Inverting) | 8-65 |
| Am8228 | System Controller/Bus Driver for Am9080A | 8-77 |
| Am8238 | System Controller/Bus Driver for Am9080A | 8-77 |

# Bipolar Support Circuits for MOS Microprocessor and Memory Systems

## NUMERICAL INDEX


| | | Page |
|---|---|---|
| Am3212 | 8-Bit Input/Output Port | 8-58 |
| Am3216 | 4-Bit Bidirectional Bus Driver | 8-65 |
| Am3226 | 4-Bit Bidirectional Bus Driver | 8-65 |
| Am3446A | IEEE-488 Quad Bidirectional Bus Transceiver | 8-1 |
| Am28T03 | Octal Bus Transceiver (Inverting) | 8-8 |
| Am28T04 | Octal Bus Transceiver (Non-Inverting) | 8-8 |
| Am28T07 | Octal Bus Transceiver (Inverting) | 8-12 |
| Am28T08 | Octal Bus Transceiver (Non-Inverting) | 8-12 |
| Am28T20 | Octal Register | 8-14 |
| Am28T21 | 8-Bit Comparator | 8-18 |
| Am28T27 | Clock Generator | 8-22 |
| Am28T33 | Octal Latch (Inverting) | 8-25 |
| Am28T38 | 8-Bit Decoder w/Storage | 8-28 |
| Am28T40 | Octal 3-State Buffer (Inverting) | 8-32 |
| Am28T44 | Octal 3-State Buffer (Non-Inverting) | 8-32 |
| Am28T48 | Address Decoder w/Acknowledge | 8-35 |
| Am28T60 | Error Detection and Correction Unit | 8-41 |
| Am28T61 | EDC Bus Buffer (Inverting to Bus) | 8-46 |
| Am28T62 | EDC Bus Buffer (Non-Inverting to Bus) | 8-49 |
| Am28T63 | Refresh and EDC Controller | 8-50 |
| Am28T64 | Dynamic Memory Controller | 8-61 |
| Am28T65 | Dynamic RAM Driver (Inverting) | 8-62 |
| Am28T66 | Dynamic RAM Driver (Non-Inverting) | 8-62 |
| Am28T73 | Octal Latch (Non-Inverting) | 8-23 |
| Am8212 | 8-Bit Input/Output Port | 8-58 |
| Am8216 | 4-Bit Bidirectional Bus Driver (Non-Inverting) | 8-65 |
| Am8224 | Clock Generator | 8-70 |
| Am8226 | 4-Bit Bidirectional Bus Driver (Inverting) | 8-65 |
| Am8228 | System Controller/Bus Driver for Am8080A | 8-77 |
| Am8238 | System Controller/Bus Driver for Am8080A | 8-77 |


8

# Am3448A

## IEEE-488 Quad Bidirectional Transceiver

### DISTINCTIVE CHARACTERISTICS

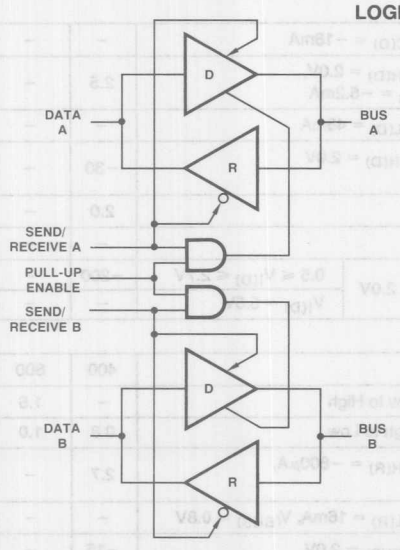
- Four independent driver/receiver pairs
- Three-state outputs
- High impedance inputs
- Receiver hysteresis – 600mV (Typ.)
- Fast Propagation Times – 15-20ns (Typ.)
- TTL compatible receiver outputs
- Single +5 volt supply
- Open collector driver output option with internal passive pull up
- Power up/power down protection (No invalid information transmitted to bus)
- No bus loading when power is removed from device
- Required termination characteristics provided
- Advanced Schottky processing
- 100% product assurance screening to MIL-STD-883 requirements

### GENERAL DESCRIPTION

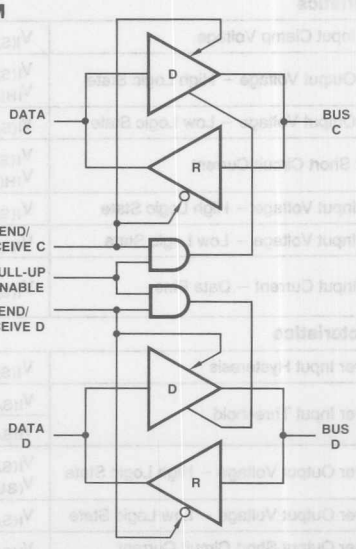
The Am3448A is a quad bidirectional transceiver meeting the requirement of IEEE-488 standard digital interface for programmable instrumentation for the driver, receiver, and composite device load. One pull-up enable input is provided for each pair of transceivers which controls the operating mode of the driver outputs as either an open collector or active pull-up configuration.

The receivers feature input hysteresis for improved noise immunity in system applications. The device bus (receiver input) changes from standard bus loading to a high impedance load when power is removed. In addition no spurious noise is generated on the bus during power-up or power-down.

### LOGIC DIAGRAM




LIC-446



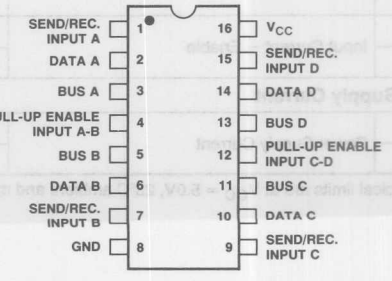

LIC-447

### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Hermetic DIP | 0°C to +70°C | MC3448AL |
| Molded DIP | 0°C to +70°C | MC3448AP |
| Dice | 0°C to +70°C | AM3448AX |

### CONNECTION DIAGRAM

Top View




Note: Pin 1 is marked for orientation.

LIC-448

8

## ABSOLUTE MAXIMUM RATINGS above which the useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Supply Voltage | 7.0V |
| Input Voltage | 5.5V |
| Driver Output Current | 150mA |

## ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am3448A $T_A$ = 0°C to 70°C $V_{CC}$ MIN. = 4.75V $V_{CC}$ MAX. = 5.25V

## DC ELECTRICAL CHARACTERISTICS over operating temperature range

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| **Bus Characteristics** | | | | | | | |
| $V_{(BUS)}$ | Bus Voltage | Bus Pin Open, $V_{I(S/R)}$ = 0.8V | | 2.75 | – | 3.7 | Volts |
| $V_{IC(BUS)}$ | | $I_{(BUS)}$ = −12mA | | – | – | −1.5 | |
| $I_{(BUS)}$ | Bus Current | 5.0V ≤ $V_{(BUS)}$ ≤ 5.5V | | 0.7 | – | 2.5 | mA |
| | | $V_{(BUS)}$ = 0.5V | | −1.3 | – | −3.2 | |
| | | $V_{CC}$ = 0V, 0V ≤ $V_{(BUS)}$ ≤ 2.75V | | – | – | 0.04 | |
| **Driver Characteristics** | | | | | | | |
| $V_{IC(D)}$ | Driver Input Clamp Voltage | $V_{I(S/R)}$ = 2.0V, $I_{IC(D)}$ = −18mA | | – | – | −1.5 | Volts |
| $V_{OH(D)}$ | Driver Output Voltage – High Logic State | $V_{I(S/R)}$ = 2.0V, $V_{IH(D)}$ = 2.0V, $V_{IH(E)}$ = 2.0V, $I_{OH}$ = −5.2mA | | 2.5 | – | – | Volts |
| $V_{OL(D)}$ | Driver Output Voltage – Low Logic State | $V_{I(S/R)}$ = 2.0V, $I_{OL(D)}$ = 48mA | | – | – | 0.5 | Volts |
| $I_{OS(D)}$ | Output Short Circuit Current | $V_{I(S/R)}$ = 2.0V, $V_{IH(D)}$ = 2.0V $V_{IH(E)}$ = 2.0V | | −30 | – | −120 | mA |
| $V_{IH(D)}$ | Driver Input Voltage – High Logic State | $V_{I(S/R)}$ = 2.0V | | 2.0 | – | – | Volts |
| $V_{IL(D)}$ | Driver Input Voltage – Low Logic State | $V_{I(S/R)}$ = 2.0V | | – | – | 0.8 | Volts |
| $I_{I(D)}$ | Driver Input Current – Data Pins | $V_{I(S/R)}$ = $V_{I(E)}$ = 2.0V | 0.5 ≤ $V_{I(D)}$ ≤ 2.7V | −200 | – | 40 | µA |
| $I_{IB(D)}$ | | | $V_{I(D)}$ = 5.5V | – | – | 200 | |
| **Receiver Characteristics** | | | | | | | |
| $V_{HYS(R)}$ | Receiver Input Hysteresis | $V_{I(S/R)}$ = 0.8V | | 400 | 600 | – | mV |
| $V_{ILH(R)}$ | Receiver Input Threshold | $V_{I(S/R)}$ = 0.8V, Low to High | | – | 1.6 | 1.8 | Volts |
| $V_{IHL(R)}$ | | $V_{I(S/R)}$ = 0.8V, High to Low | | 0.8 | 1.0 | – | |
| $V_{OH(R)}$ | Receiver Output Voltage – High Logic State | $V_{I(S/R)}$ = 0.8V, $I_{OH(R)}$ = −800µA, $V_{(BUS)}$ = 2.0V | | 2.7 | – | – | Volts |
| $V_{OL(R)}$ | Receiver Output Voltage – Low Logic State | $V_{I(S/R)}$ = 0.8V, $I_{OL(R)}$ = 16mA, $V_{(BUS)}$ = 0.8V | | – | – | 0.5 | Volts |
| $I_{OS(R)}$ | Receiver Output Short Circuit Current | $V_{I(S/R)}$ = 0.8V, $V_{(BUS)}$ = 2.0V | | −15 | – | −75 | mA |
| **Enable, Send/Receive Characteristics** | | | | | | | |
| $I_{I(S/R)}$ | Input Current – Send/Receive | 0.5 ≤ $V_{I(S/R)}$ ≤ 2.7V | | −100 | – | 20 | µA |
| $I_{IB(S/R)}$ | | $V_{I(S/R)}$ = 5.5V | | – | – | 100 | |
| $I_{I(E)}$ | Input Current – Enable | 0.5 ≤ $V_{I(E)}$ ≤ 2.7V | | −200 | – | 20 | µA |
| $I_{IB(E)}$ | | $V_{I(E)}$ = 5.5V | | – | – | 100 | |
| **Power Supply Current** | | | | | | | |
| $I_{CCL}$ | Power Supply Current | Listening Mode – All Receivers On | | – | 63 | 85 | mA |
| $I_{CCH}$ | | Talking Mode – All Drivers On | | – | 106 | 125 | |

Note 1. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.

## SWITCHING CHARACTERISTICS ($V_{CC}$ = 5.0V, $T_A$ = 25°C unless otherwise noted)

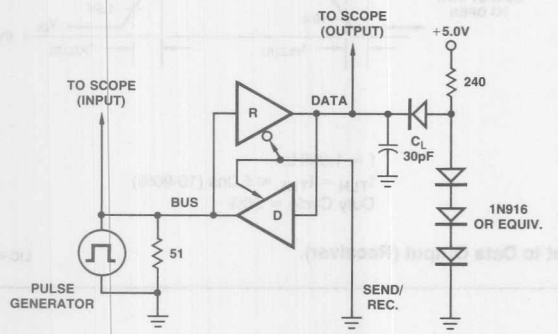
| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{PLH(D)}$ | Propagation Delay of Driver (Fig. 2) | Output Low to High | – | | 15 | ns |
| $t_{PHL(D)}$ | | Output High to Low | | | 17 | |
| $t_{PLH(R)}$ | Propagation Delay of Receiver (Fig. 1) | Output Low to High | – | | 25 | ns |
| $t_{PHL(R)}$ | | Output High to Low | – | | 23 | |
| $t_{PHZ(R)}$ | Propagation Delay Time – Send/Receiver to Data (Fig. 4) | Logic High to Third State | – | | 30 | ns |
| $t_{PZH(R)}$ | | Third State to Logic High | – | | 30 | |
| $t_{PLZ(R)}$ | | Logic Low to Third State | – | | 30 | |
| $t_{PZL(R)}$ | | Third State to Logic Low | | | 30 | |
| $t_{PHZ(D)}$ | Propagation Delay Time – Send/Receiver to Bus (Fig. 3) | Logic High to Third State | – | | 30 | ns |
| $t_{PZH(D)}$ | | Third State to Logic High | – | | 30 | |
| $t_{PLZ(D)}$ | | Logic Low to Third State | – | | 30 | |
| $t_{PZL(D)}$ | | Third State to Logic Low | | | 30 | |
| $t_{POFF(E)}$ | Turn-On Time – Enable to Bus (Fig. 5) | Pull-Up Enable to Open Collector | – | | 30 | ns |
| $t_{PON(E)}$ | | Open Collector to Pull-Up Enable | – | | 20 | |

### TRUTH TABLE

| Send/Rec. | Enable | Into Flow | Comments |
|---|---|---|---|
| 0 | X | Bus → Data | |
| 1 | 1 | Data → Bus | Active Pull-Up |
| 1 | 0 | Data → Bus | Open Collector |

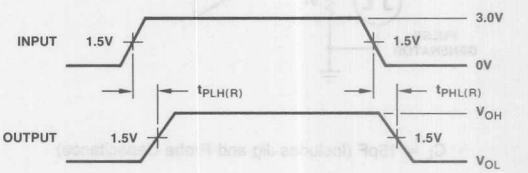
X = Don't Care

### PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS




*Includes Jig and Probe Capacitance.

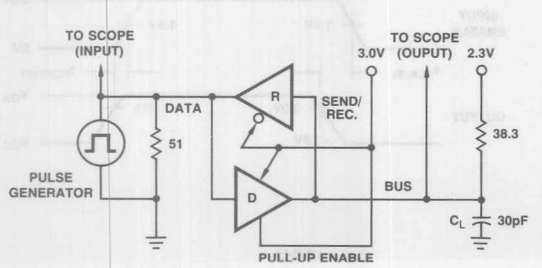
LIC-449




f = 1.0MHz
$t_{TLH} = t_{THL} \leq 5.0$ns (10-90%)
Duty Cycle = 50%

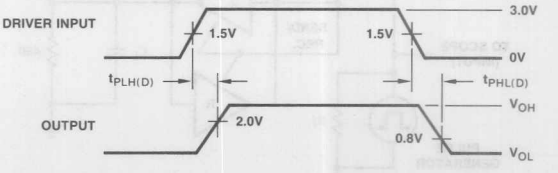
LIC-450

**Figure 1. Bus Input to Data Output (Receiver).**




*Includes Jig and Probe Capacitance.

LIC-451



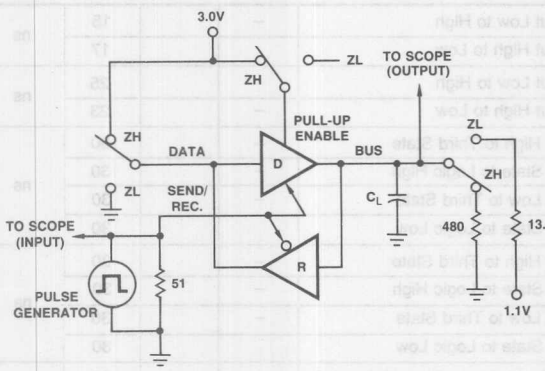

f = 1.0MHz
$t_{TLH} = t_{THL} \leq 5.0$ns (10-90%)
Duty Cycle = 50%

LIC-452

**Figure 2. Data Input to Bus Output (Driver).**

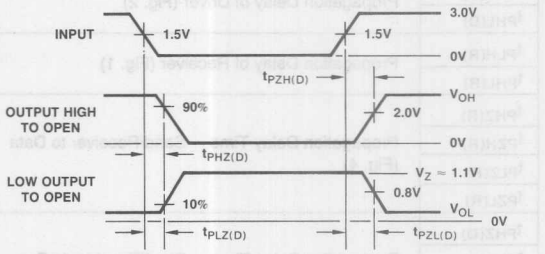
8

## PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS (Cont.)




$C_L$ = 15pF (Includes Jig and Probe Capacitance)

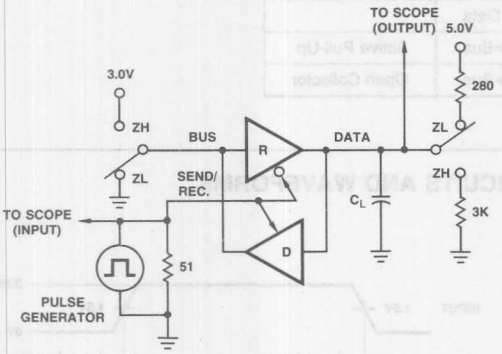
LIC-453




f = 1.0MHz
$t_{TLH} = t_{THL} \leq 5.0$ns (10-90%)
Duty Cycle = 50%

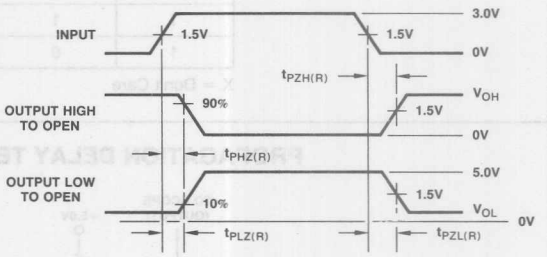
LIC-454

**Figure 3. Send/Receive Input to Bus Output (Driver).**




$C_L$ = 15pF (Includes Jig and Probe Capacitance)

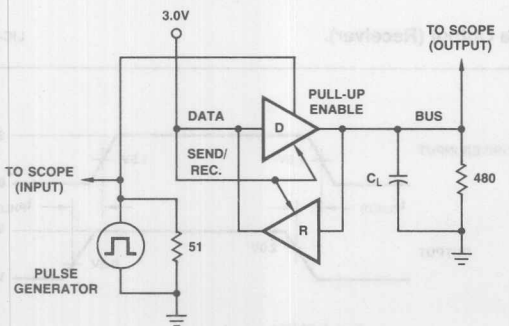
LIC-455




f = 1.0MHz
$t_{TLH} = t_{THL} \leq 5.0$ns (10-90%)
Duty Cycle = 50%

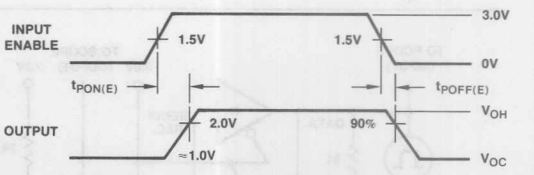
LIC-456

**Figure 4. Send/Receive Input to Data Output (Receiver).**




$C_L$ = 15pF (Includes Jig and Probe Capacitance)

LIC-457



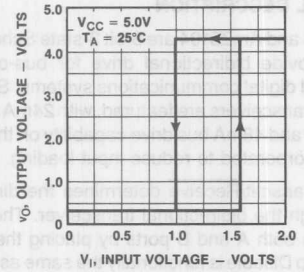

f = 1.0MHz
$t_{TLH} = t_{THL} \leq 5.0$ns (10-90%)
Duty Cycle = 50%

LIC-458

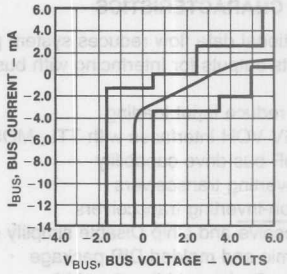
**Figure 5. Enable Input to Bus Output (Driver).**

## PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS (Cont.)

### TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

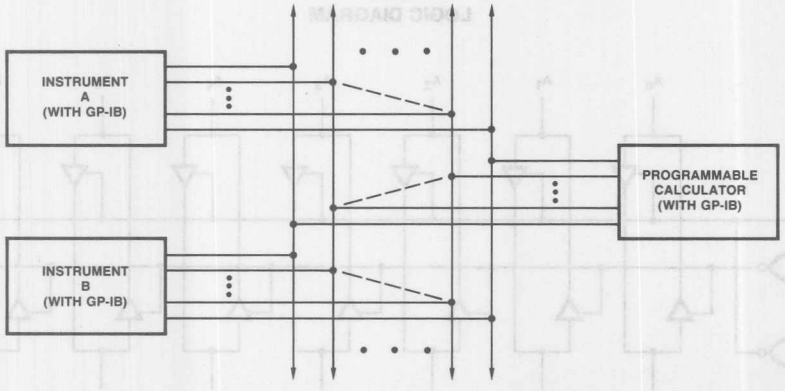



### TYPICAL BUS LOAD LINE




LIC-459

## TYPICAL APPLICATION




LIC-460

### TYPICAL MEASUREMENT SYSTEM APPLICATION

8

# AmZ8103 • AmZ8104

## Octal Three-State Bidirectional Bus Transceivers

### DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- 3-state inputs/outputs for interfacing with bus-oriented systems
- PNP inputs reduce input loading
- VCC – 1.15V VOH interfaces with TTL, MOS and CMOS
- 48mA, 300pF bus drive capability
- AmZ8103 inverting transceivers
- AmZ8104 non-inverting transceivers
- Transmit/$\overline{\text{Receive}}$ and Chip Disable simplify control logic
- 20-pin ceramic and molded DIP package
- Low power – 8mA per bidirectional bit
- Advanced Schottky processing
- Bus port stays in hi-impedance state during power up/down
- 100% product assurance screening to MIL-STD-883 requirements

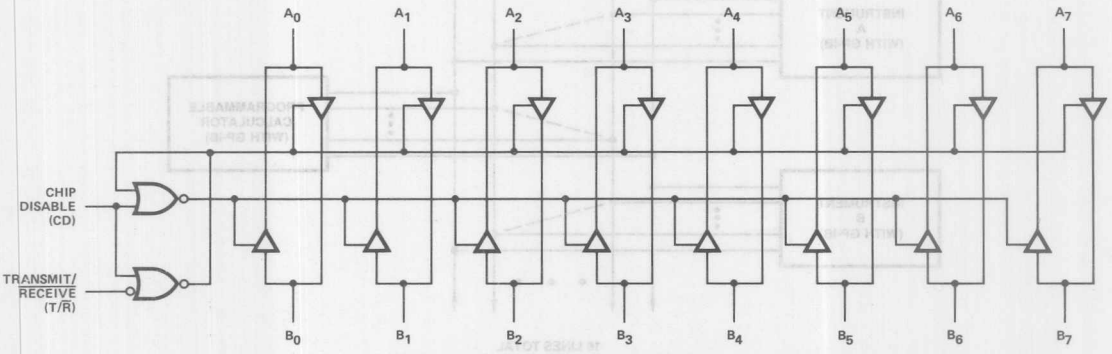
### FUNCTIONAL DESCRIPTION

The AmZ8103 and AmZ8104 are 8-bit 3-state Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

One input, Transmit/$\overline{\text{Receive}}$ determines the direction of logic signals through the bidirectional transceiver. The Chip Disable input disables both A and B ports by placing them in a 3-state condition. Chip Disable is functionally the same as an active LOW chip select.

The output high voltage (VOH) is specified at VCC – 1.15V minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM, or microprocessors.

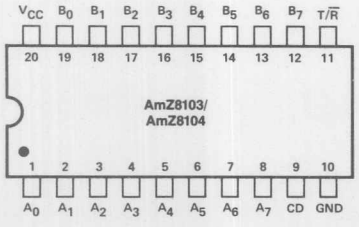
### AmZ8104 LOGIC DIAGRAM




AmZ8103 has inverting transceivers.

BLI-216

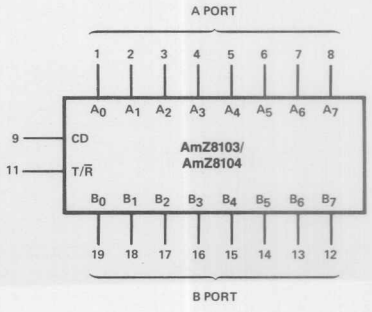
### CONNECTION DIAGRAM Top View




BLI-169

Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL




BLI-170

VCC = Pin 20
GND = Pin 10

AmZ8103 • AmZ8104

## ABSOLUTE MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65 to +150°C |
| Supply Voltage | 7.0V |
| Input Voltage | 5.5V |
| Output Voltage | 5.5V |
| Lead Temperature (Soldering, 10 seconds) | 300°C |

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Noted:

MIL $T_A$ = −55 to +125°C VCC MIN = 4.5V VCC MAX = 5.5V
COM'L $T_A$ = 0 to 70°C VCC MIN = 4.75V VCC MAX = 5.25V

## DC ELECTRICAL CHARACTERISTICS over operating temperature range

| Parameters | Description | Test Conditions | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|
| | | **A PORT (A0-A7)** | | | | | |
| VIH | Logical "1" Input Voltage | CD = VIL MAX, T/R = 2.0V | | 2.0 | | | Volts |
| VIL | Logical "0" Input Voltage | CD = VIL MAX, T/R = 2.0V | COM'L | | | 0.8 | Volts |
| | | | MIL | | | 0.7 | |
| VOH | Logical "1" Output Voltage | CD = VIL MAX, T/R = 0.8V | IOH = −0.4mA | VCC−1.15 | VCC−0.7 | | Volts |
| | | | IOH = −3.0mA | 2.7 | 3.95 | | |
| VOL | Logical "0" Output Voltage | CD = VIL MAX, T/R = 0.8V | IOL = 12mA | | 0.3 | 0.4 | Volts |
| | | | COM'L, IOL = 24mA | | 0.35 | 0.50 | |
| IOS | Output Short Circuit Current | CD = VIL MAX, T/R = 0.8V, VO = 0V, VCC = MAX, Note 2 | | −10 | −38 | −75 | mA |
| IIH | Logical "1" Input Current | CD = VIL MAX, T/R = 2.0V, VI = 2.7V | | | 0.1 | 80 | μA |
| II | Input Current at Maximum Input Voltage | CD = 2.0V, VCC = MAX, VI = VCC MAX | | | | 1 | mA |
| IIL | Logical "0" Input Current | CD = VIL MAX, T/R = 2.0V, VI = 0.4V | | | −70 | −200 | μA |
| VC | Input Clamp Voltage | CD = 2.0V, IIN = −12mA | | | −0.7 | −1.5 | Volts |
| IOD | Output/Input 3-State Current | CD = 2.0V | VO = 0.4V | | | −200 | μA |
| | | | VO = 4.0V | | | 80 | |
| | | **B PORT (B0-B7)** | | | | | |
| VIH | Logical "1" Input Voltage | CD = VIL MAX, T/R = VIL MAX | | 2.0 | | | Volts |
| VIL | Logical "0" Input Voltage | CD = VIL MAX, T/R = VIL MAX | COM'L | | | 0.8 | Volts |
| | | | MIL | | | 0.7 | |
| VOH | Logical "1" Output Voltage | CD = VIL MAX, T/R = 2.0V | IOH = −0.4mA | VCC−1.15 | VCC−0.8 | | Volts |
| | | | IOH = −5mA | 2.7 | 3.9 | | |
| | | | IOH = −10mA | 2.4 | 3.6 | | |
| VOL | Logical "0" Output Voltage | CD = VIL MAX, T/R = 2.0V | IOL = 20mA | | 0.3 | 0.4 | Volts |
| | | | IOL = 48mA | | .4 | 0.5 | |
| IOS | Output Short Circuit Current | CD = VIL MAX, T/R = 2.0V, VO = 0V, VCC = MAX, Note 2 | | −25 | −50 | −150 | mA |
| IIH | Logical "1" Input Current | CD = VIL MAX, T/R = VIL MAX, VI = 2.7V | | | 0.1 | 80 | μA |
| II | Input Current at Maximum Input Voltage | CD = 2.0V, VCC = MAX, VI = VCC MAX | | | | 1 | mA |
| IIL | Logical "0" Input Current | CD = VIL MAX, T/R = VIL MAX, VI = 0.4V | | | −70 | −200 | μA |
| VC | Input Clamp Voltage | CD = 2.0V, IIN = −12mA | | | −0.7 | −1.5 | Volts |
| IOD | Output/Input 3-State Current | CD = 2.0V | VO = 0.4V | | | −200 | μA |
| | | | VO = 4.0V | | | 200 | |
| | | **CONTROL INPUTS CD, T/R** | | | | | |
| VIH | Logical "1" Input Voltage | | | 2.0 | | | Volts |
| VIL | Logical "0" Input Voltage | | COM'L | | | 0.8 | Volts |
| | | | MIL | | | 0.7 | |
| IIH | Logical "1" Input Current | VI = 2.7V | | | 0.5 | 20 | μA |
| II | Input Current at Maximum Input Voltage | VCC = MAX, VI = VCC MAX | | | | 1.0 | mA |
| IIL | Logical "0" Input Current | VI = 0.4V | T/R | | −0.1 | −.25 | mA |
| | | | CD | | −0.1 | −0.25 | |
| VC | Input Clamp Voltage | IIN = −12mA | | | −0.8 | −1.5 | Volts |
| | | **POWER SUPPLY CURRENT** | | | | | |
| ICC | Power Supply Current | AmZ8103 | CD =, VI = 2.0V, VCC = MAX | | 70 | 100 | mA |
| | | | CD = 0.4V, VINA = T/R = 2V, VCC = MAX | | 100 | 150 | |
| | | AmZ8104 | CD = 2.0V, VI = 0.4V, VCC = MAX | | 70 | 100 | |
| | | | CD = VINA = 0.4V, T/R = 2V, VCC = MAX | | 90 | 140 | |

8

## AmZ8103

## AC ELECTRICAL CHARACTERISTICS (VCC = 5.0V, $T_A$ = 25°C)

| Parameters | Description | Test Conditions | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|
| **A PORT DATA/MODE SPECIFICATIONS** | | | | | | |
| tPDHLA | Propagation Delay to a Logical "0" from B Port to A Port | CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1)<br>R1 = 1k, R2 = 5k, C1 = 30pF | | 8 | 12 | ns |
| tPDLHA | Propagation Delay to a Logical "1" from B Port to A Port | CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1)<br>R1 = 1k, R2 = 5k, C1 = 30pF | | 11 | 16 | ns |
| tPLZA | Propagation Delay from a Logical "0" to 3-State from CD to A Port | B0 to B7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>S3 = 1, R5 = 1k, C4 = 15pF | | 10 | 15 | ns |
| tPHZA | Propagation Delay from a Logical "1" to 3-State from CD to A Port | B0 to B7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>S3 = 0, R5 = 1k, C4 = 15pF | | 8 | 15 | ns |
| tPZLA | Propagation Delay from 3-State to a Logical "0" from CD to A Port | B0 to B7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>S3 = 1, R5 = 1k, C4 = 30pF | | 20 | 30 | ns |
| tPZHA | Propagation Delay from 3-State to a Logical "1" from CD to A Port | B0 to B7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>S3 = 0, R5 = 5k, C4 = 30pF | | 19 | 30 | ns |
| **B PORT DATA/MODE SPECIFICATIONS** | | | | | | |
| tPDHLB | Propagation Delay to a Logical "0" from A Port to B Port | CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1)<br>R1 = 100Ω, R2 = 1k, C1 = 300pF | | 12 | 18 | ns |
| | | R1 = 667Ω, R2 = 5k, C1 = 45pF | | 7 | 12 | |
| tPDLHB | Propagation Delay to a Logical "1" from A Port to B Port | CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1)<br>R1 = 100Ω, R2 = 1k, C1 = 300pF | | 15 | 20 | ns |
| | | R1 = 667Ω, R2 = 5k, C1 = 45pF | | 9 | 14 | |
| tPLZB | Propagation Delay from a Logical "0" to 3-State from CD to B Port | A0 to A7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3)<br>S3 = 1, R5 = 1k, C4 = 15pF | | 13 | 18 | ns |
| tPHZB | Propagation Delay from A Logical "1" to 3-State from CD to B Port | A0 to A7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3)<br>S3 = 0, R5 = 1k, C4 = 15pF | | 8 | 15 | ns |
| tPZLB | Propagation Delay from 3-State to a Logical "0" from CD to B Port | A0 to A7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3)<br>S3 = 1, R5 = 100Ω, C4 = 300pF | | 25 | 35 | ns |
| | | S3 = 1, R5 = 667Ω, C4 = 45pF | | 16 | 25 | |
| tPZHB | Propagation Delay from 3-State to a Logical "1" from CD to B Port | A0 to A7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3)<br>S3 = 0, R5 = 1k, C4 = 300pF | | 22 | 35 | ns |
| | | S3 = 0, R5 = 5kΩ, C4 = 45pF | | 14 | 25 | |
| **TRANSMIT RECEIVE MODE SPECIFICATIONS** | | | | | | |
| tTRL | Propagation Delay from Transmit Mode to Receive a Logical "0," T/R to A Port | CD = 0.4V (Figure 2)<br>S1 = 1, R4 = 100Ω, C3 = 5pF<br>S2 = 1, R3 = 1k, C2 = 30pF | | 23 | 35 | ns |
| tTRH | Propagation Delay from Transmit Mode to Receive a Logical "1," T/R to A Port | CD = 0.4V (Figure 2)<br>S1 = 0, R4 = 100Ω, C3 = 5pF<br>S2 = 0, R3 = 5k, C2 = 30pF | | 22 | 35 | ns |
| tRTL | Propagation Delay from Receive Mode to Transmit a Logical "0," T/R to B Port | CD = 0.4V (Figure 2)<br>S1 = 1, R4 = 100Ω, C3 = 300pF<br>S2 = 1, R3 = 300Ω, C2 = 5pF | | 26 | 35 | ns |
| tRTH | Propagation Delay from Receive Mode to Transmit a Logical "1," T/R to B Port | CD = 0.4V (Figure 2)<br>S1 = 0, R4 = 1k, C3 = 300pF<br>S2 = 0, R3 = 300Ω, C2 = 5pF | | 27 | 35 | ns |

Notes: 1. All typical values given are for VCC = 5.0V and $T_A$ = 25°C.
2. Only one output at a time should be shorted.

### FUNCTIONAL TABLE

| Inputs | Conditions | | |
|---|---|---|---|
| Chip Disable | 0 | 0 | 1 |
| Transmit/$\overline{\text{Receive}}$ | 0 | 1 | X |
| A Port | Out | In | HI-Z |
| B Port | In | Out | HI-Z |

## AmZ8104
## AC ELECTRICAL CHARACTERISTICS (VCC = 5.0V, $T_A$ = 25°C)

| Parameters | Description | Test Conditions | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|
| | | **A PORT DATA/MODE SPECIFICATIONS** | | | | |
| tPDHLA | Propagation Delay to a Logical "0" from B Port to A Port | CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1)<br>R1 = 1k, R2 = 5k, C1 = 30pF | | 14 | 18 | ns |
| tPDLHA | Propagation Delay to a Logical "1" from B Port to A Port | CD =0.4V, T/$\overline{R}$ = 0.4V (Figure 1)<br>R1 = 1k, R2 = 5k, C1 = 30pF | | 13 | 18 | ns |
| tPLZA | Propagation Delay from a Logical "0" to 3-State from CD to A Port | B0 to B7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>S3 = 1, R5 = 1k, C4 = 15pF | | 11 | 15 | ns |
| tPHZA | Propagation Delay from a Logical "1" to 3-State from CD to A Port | B0 to B7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>S3 = 0, R5 = 1k, C4 = 15pF | | 8 | 15 | ns |
| tPZLA | Propagation Delay from 3-State to a Logical "0" from CD to A Port | B0 to B7 = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>S3 = 1, R5 = 1k, C4 = 30pF | | 27 | 35 | ns |
| tPZHA | Propagation Delay from 3-State to a Logical "1" from CD to A Port | B0 to B7 = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>S3 = 0, R5 = 5k, C4 = 30pF | | 19 | 25 | ns |
| | | **B PORT DATA/MODE SPECIFICATIONS** | | | | |
| tPDHLB | Propagation Delay to Logical "0" from A Port to B Port | CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1)<br>R1 = 100Ω, R2 = 1k, C1 = 300pF | | 18 | 23 | ns |
| | | R1 = 667Ω, R2 = 5k, C1 = 45pF | | 11 | 18 | |
| tPDLHB | Propagation Delay to Logical "1" from A Port to B Port | CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1)<br>R1 = 100Ω, R2 = 1k, C1 = 300pF | | 16 | 23 | ns |
| | | R1 = 667Ω, R2 = 5k, C1 = 45pF | | 11 | 18 | |
| tPLZB | Propagation Delay from a Logical "0" to 3-State from CD to B Port | A0 to A7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3)<br>S3 = 1, R5 = 1k, C4 = 15pF | | 13 | 18 | ns |
| tPHZB | Propagation Delay from a Logical "1" to 3-State from CD to B Port | A0 to A7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3)<br>S3 = 0, R5 = 1k, C4 = 15pF | | 8 | 15 | ns |
| tPZLB | Propagation Delay from 3-State to a Logical "0" from CD to B Port | A0 to A7 = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3)<br>S3 = 1, R5 = 100Ω, C4 = 300pF | | 32 | 40 | ns |
| | | S3 = 1, R5 = 667Ω, C4 = 45pF | | 16 | 22 | |
| tPZHB | Propagation Delay from 3-State to a Logical "1" from CD to B Port | A0 to A7 = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3)<br>S3 = 0, R5 = 1k, C4 = 300pF | | 26 | 35 | ns |
| | | S3 = 0, R5 = 5kΩ, C4 = 45pF | | 14 | 22 | |
| | | **TRANSMIT RECEIVE MODE SPECIFICATIONS** | | | | |
| tTRL | Propagation Delay from Transmit Mode to Receive a Logical "0," T/$\overline{R}$ to A Port | CD = 0.4V (Figure 2)<br>S1 = 0, R4 = 100Ω, C3 = 5pF<br>S2 = 1, R3 = 1k, C2 = 30pF | | 30 | 40 | ns |
| tTRH | Propagation Delay from Transmit Mode to Receive a Logical "1," T/$\overline{R}$ to A Port | CD = 0.4V (Figure 2)<br>S1 = 1, R4 = 100Ω, C3 =5pF<br>S2 = 0, R3 = 5k, C2 = 30pF | | 28 | 40 | ns |
| tRTL | Propagation Delay from Receive Mode to Transmit a Logical "0," T/$\overline{R}$ to B Port | CD = 0.4V (Figure 2)<br>S1 = 1, R4 = 100Ω, C3 = 300pF<br>S2 = 0, R3 = 300Ω, C2 = 5pF | | 31 | 40 | ns |
| tRTH | Propagation Delay from Receive Mode to Transmit a Logical "1," T/$\overline{R}$ to B Port | CD = 0.4V (Figure 2)<br>S1 = 0, R4 = 1k, C3 = 300pF<br>S2 = 1, R3 = 300Ω, C2 = 5pF | | 28 | 40 | ns |

Notes: 1. All typical values given are for VCC = 5.0V and $T_A$ = 25°C.
2. Only one output at a time should be shorted.

**DEFINITION OF FUNCTIONAL TERMS**

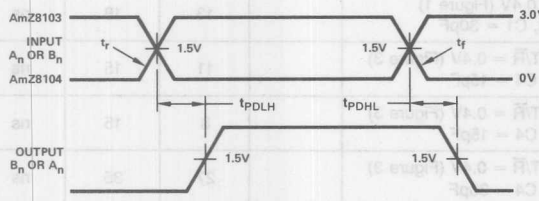
**A0-A7** A port inputs/outputs are receiver output drivers when T/$\overline{R}$ is LOW and are transmit inputs when T/$\overline{R}$ is HIGH.

**B0-B7** B port inputs/outputs are transmit output drivers when T/$\overline{R}$ is HIGH and receiver inputs when T/$\overline{R}$ is LOW.

**CD** Chip Disable forces all output drivers into 3-state when HIGH (same function as active LOW chip select, $\overline{CS}$).

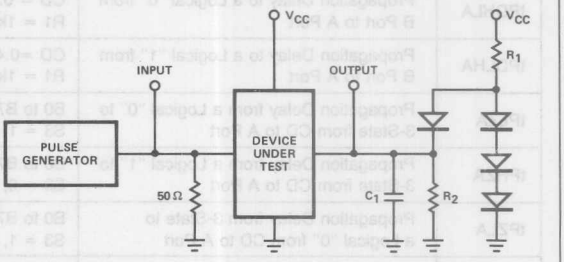
**T/$\overline{R}$** Transmit/$\overline{Receive}$ direction control determines whether A port or B port drivers are in 3-state. With T/$\overline{R}$ HIGH A port is the input and B port is the output. With T/$\overline{R}$ LOW A port is the output and B port is the input.

8




$t_r = t_f < 10ns$
10% to 90%

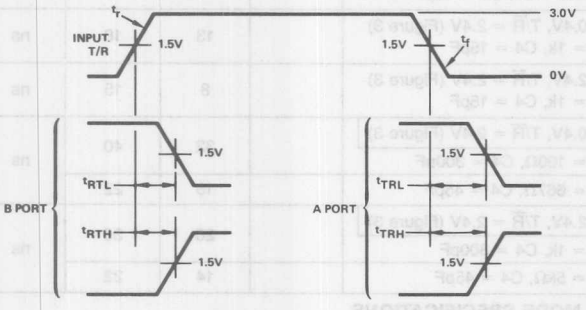
BLI-171




Note: $C_1$ includes test fixture capacitance.

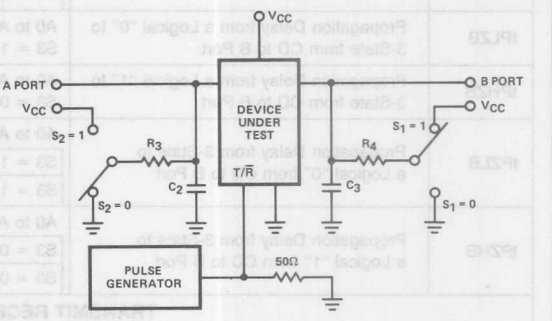
BLI-172

**Figure 1. Propagation Delay from A Port to B Port or from B Port to A Port.**




$t_r = t_f < 10ns$
10% to 90%

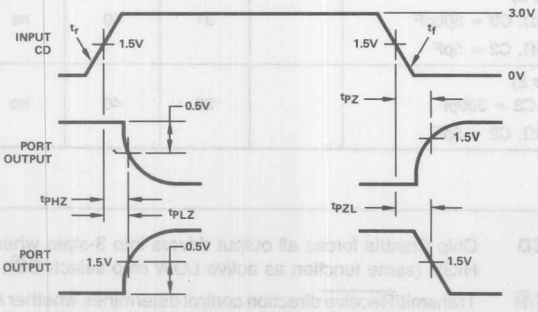
BLI-173




Note: $C_2$ and $C_3$ include test fixture capacitance.

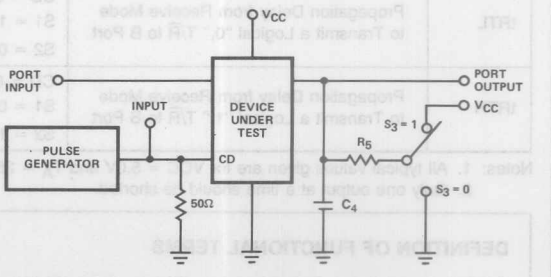
BLI-174

**Figure 2. Propagation Delay from T/$\overline{R}$ to A Port or B Port.**




$t_r = t_f < 10ns$
10% to 90%

BLI-175



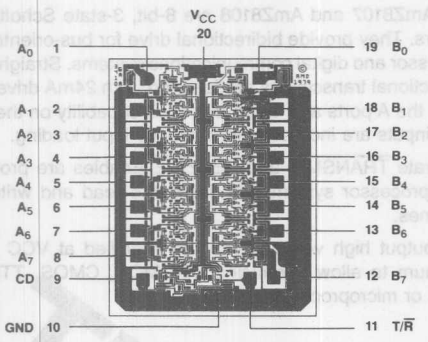

Note: $C_4$ includes test fixture capacitance.
Port input is in a fixed logical condition.

BLI-176

**Figure 3. Propagation Delay from CD to A Port or B Port.**

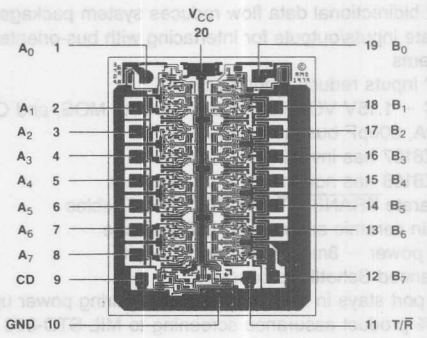
## Metallization and Pad Layouts

### AmZ8103




DIE SIZE .069" X .089"

### AmZ8104




DIE SIZE .069" X .089"

## ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range and screening level.

| AmZ8103 Order Number | AmZ8104 Order Number | Package Type (Note 1) | Operating Range (Note 2) | Screening Level (Note 3) |
|---|---|---|---|---|
| AMZ8103DC | AMZ8104DC | D-20 | C | C-1 |
| AMZ8103DCB | AMZ8104DCB | D-20 | C | B-1 |
| AMZ8103DM | AMZ8104DM | D-20 | M | C-3 |
| AMZ8103DMB | AMZ8104DMB | D-20 | M | B-3 |
| AMZ8103PC | AMZ8104PC | P-20 | C | C-1 |
| AMZ8103PCB | AMZ8104PCB | P-20 | C | C-1 |

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flatpak. Number following letter is number of leads.
2. C = 0 to 70°C, VCC = 4.75V to 5.25V, M = −55 to +125°C, VCC = 4.50V to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

8

# AmZ8107 • AmZ8108

## Octal Three-State Bidirectional Bus Transceivers

### DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- 3-state inputs/outputs for interfacing with bus-oriented systems
- PNP inputs reduce input loading
- VCC – 1.15V VOH interfaces with TTL, MOS, and CMOS
- 48mA, 300pF bus drive capability
- AmZ8107 has inverting tranceivers
- AmZ8108 has non-inverting transceivers
- Separate $\overline{\text{TRANSMIT}}$ and $\overline{\text{RECEIVE}}$ Enables
- 20 pin ceramic and molded DIP package
- Low power – 8mA per bidirectional bit
- Advanced Schottky processing
- Bus port stays in hi-impedance state during power up/down
- 100% product assurance screening to MIL-STD-883 requirements

### GENERAL DESCRIPTION

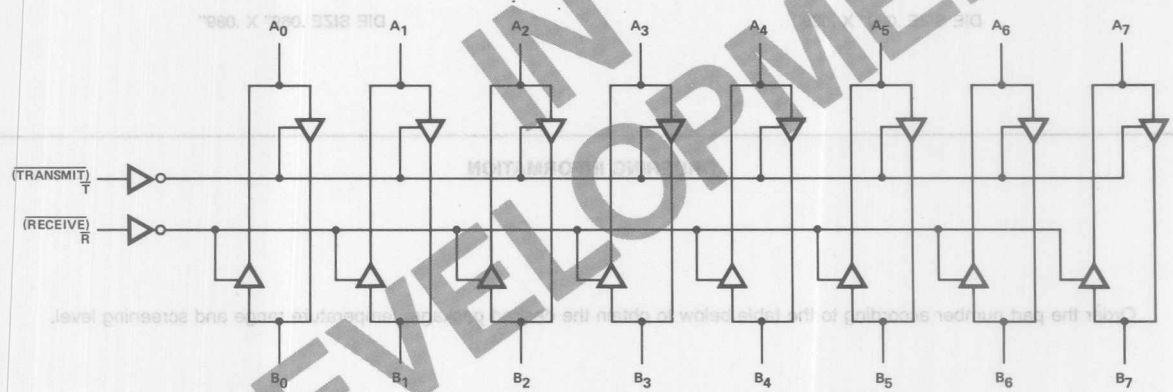
The AmZ8107 and AmZ8108 are 8-bit, 3-state Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

Separate $\overline{\text{TRANSMIT}}$ and $\overline{\text{RECEIVE}}$ Enables are provided for microprocessor system with separated read and write control bus lines.

The output high voltage (VOH) is specified at VCC – 1.15V minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM, or microprocessors.

IN DEVELOPMENT

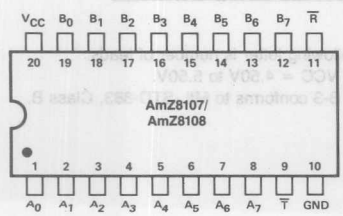
### AmZ8108 LOGIC DIAGRAM




AmZ8107 has inverting transceivers

BLI-177

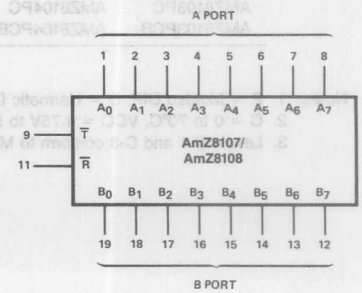
### CONNECTION DIAGRAM Top View




Note: Pin 1 is marked for orientation.
AmZ8107 is inverting from Ai to Bi

BLI-178

### LOGIC SYMBOL

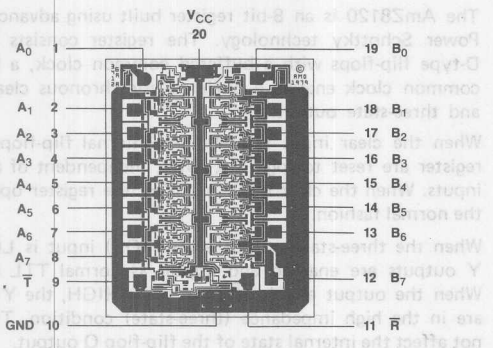



VCC = Pin 20
GND = Pin 10

BLI-179

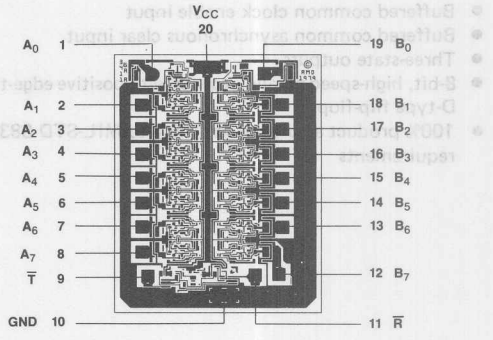
## Metallization and Pad Layouts

### AmZ8107




DIE SIZE .069" X .089"

### AmZ8108




DIE SIZE .069" X .089"

8

# AmZ8120

## Octal D-Type Flip-Flop with Clear, Clock Enable and 3-State Control

### DISTINCTIVE CHARACTERISTICS

- Buffered common clock enable input
- Buffered common asynchronous clear input
- Three-state outputs
- 8-bit, high-speed parallel register with positive edge-triggered, D-type flip-flops
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

The AmZ8120 is an 8-bit register built using advanced Low-Power Schottky technology. The register consists of eight D-type flip-flops with a buffered common clock, a buffered common clock enable, a buffered asynchronous clear input, and three-state outputs.

When the clear input is LOW, the internal flip-flops of the register are reset to logic 0 (LOW), independent of all other inputs. When the clear input is HIGH, the register operates in the normal fashion.

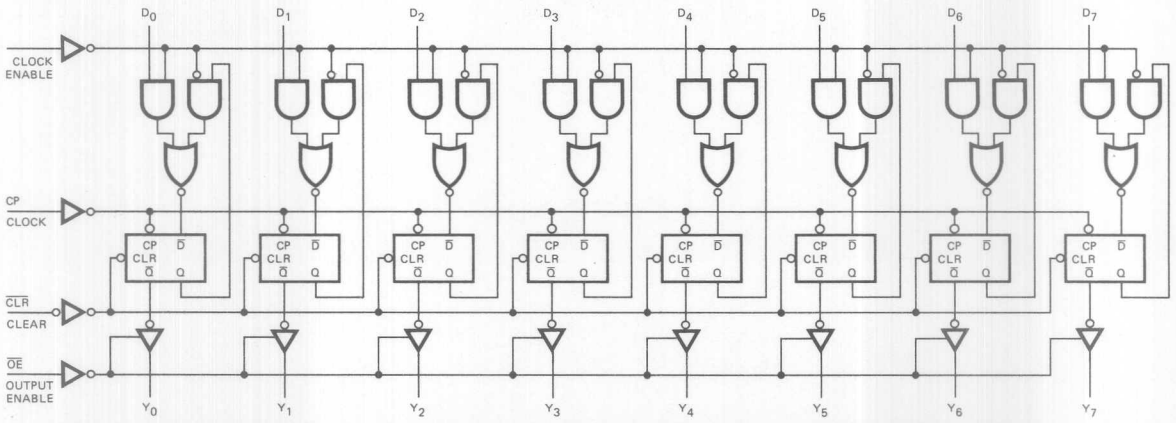
When the three-state output enable ($\overline{OE}$) input is LOW, the Y outputs are enabled and appear as normal TTL outputs. When the output enable ($\overline{OE}$) input is HIGH, the Y outputs are in the high impedance (three-state) condition. This does not affect the internal state of the flip-flop Q output.

The clock enable input ($\overline{E}$) is used to selectively load data into the register. When the $\overline{E}$ input is HIGH, the register will retain its current data. When the $\overline{E}$ is LOW, new data is entered into the register on the LOW-to-HIGH transition of the clock input.

This device is packaged in a slim 24-pin package (0.3 inch row spacing).

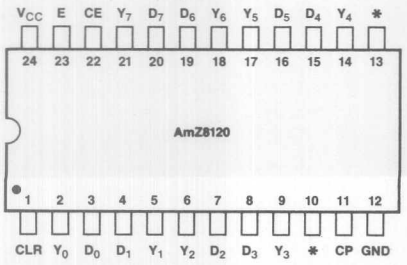
BLI-180

### LOGIC DIAGRAM



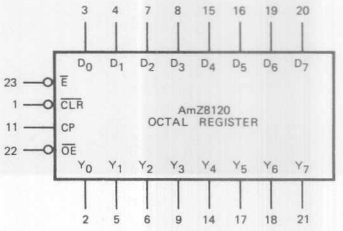

BLI-181

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation. *Reserved – do not use.

### LOGIC SYMBOL




$V_{CC}$ = Pin 24
GND = Pin 12

BLI-182

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | MIL, $I_{OH} = -1.0mA$ | 2.4 | 3.4 | | Volts |
| | | | COM'L, $I_{OH} = -2.6mA$ | 2.4 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 4.0mA$ | | | 0.4 | Volts |
| | | | $I_{OL} = 8.0mA$ | | | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | -1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | -0.36 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | 0.1 | mA |
| $I_O$ | Off-State (High-Impedance) Output Current | $V_{CC}$ = MAX. | $V_O = 0.4V$ | | | -20 | μA |
| | | | $V_O = 2.4V$ | | | 20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | -15 | | -85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | 24 | 37 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All outputs open, $\overline{E}$ = GND, Di inputs = CLR = $\overline{OE}$ = 4.5V. Apply momentary ground, then 4.5V to clock input.

8

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | -65°C to +150°C |
| Temperature (Ambient) Under Bias | -55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | -0.5 V to +7.0 V |
| DC Voltage Applied to Outputs for High Output State | -0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | -0.5 V to +7.0 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | -30 mA to +5.0 mA |

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0 V)

| Parameters | Description | | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to $Y_i$ ($\overline{OE}$ LOW) | | | 18 | 27 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | 24 | 36 | | |
| $t_{PHL}$ | Clear to Y | | | 22 | 35 | ns | |
| $t_s$ | Data ($D_i$) | | 10 | 3 | | ns | |
| $t_h$ | Data ($D_i$) | | 10 | 3 | | ns | |
| $t_s$ | Enable ($\overline{E}$) | Active | 15 | 10 | | ns | |
| | | Inactive | 20 | 12 | | | |
| $t_h$ | Enable ($\overline{E}$) | | 0 | 0 | | ns | |
| $t_s$ | Clear Recovery (In-Active) to Clock | | 11 | 7 | | ns | |
| $t_{pw}$ | Clock | HIGH | 20 | 14 | | ns | |
| | | LOW | 25 | 13 | | | |
| $t_{pw}$ | Clear | | 20 | 13 | | ns | |
| $t_{ZH}$ | $\overline{OE}$ to $Y_i$ | | | 9 | 13 | ns | |
| $t_{ZL}$ | | | | 14 | 21 | | |
| $t_{HZ}$ | $\overline{OE}$ to $Y_i$ | | | 20 | 30 | ns | $C_L$ = 5.0pF, $R_L$ = 2.0kΩ |
| $t_{LZ}$ | | | | 24 | 36 | | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | | | 40 | | MHz | |

Note 1. Per industry convention, $f_{max}$ is the worst case value of the maximum device operating frequency with no constraints on $t_r$, $t_f$, pulse width or duty cycle.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | | COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ± 5% Min. | COM'L Max. | MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ± 10% Min. | MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Clock to $Y_i$ ($\overline{OE}$ LOW) | | | 33 | | 39 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | | 45 | | 54 | | |
| $t_{PHL}$ | Clear to Y | | | 43 | | 51 | ns | |
| $t_s$ | Data ($D_i$) | | 12 | | 15 | | ns | |
| $t_h$ | Data ($D_i$) | | 12 | | 15 | | ns | |
| $t_s$ | Enable ($\overline{E}$) | Active | 17 | | 20 | | ns | |
| | | Inactive | 20 | | 23 | | | |
| $t_h$ | Enable ($\overline{E}$) | | 0 | | 0 | | ns | |
| $t_s$ | Clear Recovery (In-Active) to Clock | | 13 | | 15 | | ns | |
| $t_{pw}$ | Clock | HIGH | 25 | | 30 | | ns | |
| | | LOW | 30 | | 35 | | | |
| $t_{pw}$ | Clear | | 22 | | 25 | | ns | |
| $t_{ZH}$ | $\overline{OE}$ to $Y_i$ | | | 19 | | 25 | ns | |
| $t_{ZL}$ | | | | 30 | | 39 | | |
| $t_{HZ}$ | $\overline{OE}$ to $Y_i$ | | | 35 | | 40 | ns | $C_L$ = 5.0 pF, $R_L$ = 2.0 kΩ |
| $t_{LZ}$ | | | | 39 | | 42 | | |
| $f_{max}$ | Maximum Clock Frequency (Note 1) | | 25 | | 20 | | MHz | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## DEFINITION OF FUNCTIONAL TERMS

**$D_i$** The D flip-flop data inputs.

**$\overline{CLR}$** When the clear input is LOW, the $Q_i$ outputs are LOW, regardless of the other inputs. When the clear input is HIGH, data can be entered into the register.

**CP** Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.

**$Y_i$** The register three-state outputs.

**$\overline{E}$** Clock Enable, When the clock enable is LOW, data on the $D_i$ input is transferred to the $Q_i$ output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the $Q_i$ outputs do not change state, regardless of the data or clock input transitions.

**$\overline{OE}$** Output Control. When the $\overline{OE}$ input is HIGH, the $Y_i$ outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the $Y_i$ outputs.

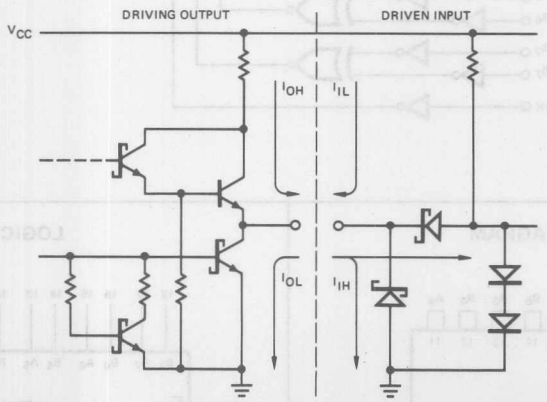
## FUNCTION TABLE

| | Inputs | | | | | Internal | Outputs |
|---|---|---|---|---|---|---|---|
| Function | $\overline{OE}$ | $\overline{CLR}$ | $\overline{E}$ | $D_i$ | CP | $Q_i$ | $Y_i$ |
| Hi-Z | H | X | X | X | X | X | Z |
| Clear | H | L | X | X | X | L | Z |
| | L | L | X | X | X | L | L |
| Hold | H | H | H | X | X | NC | Z |
| | L | H | H | X | X | NC | NC |
| Load | H | H | L | L | ↑ | L | Z |
| | H | H | L | H | ↑ | H | Z |
| | L | H | L | L | ↑ | L | L |
| | L | H | L | H | ↑ | H | H |

H = HIGH
L = LOW
X = Don't Care

NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

## LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

BLI-183

8

# AmZ8121

## Eight-Bit Equal-To Comparator

### DISTINCTIVE CHARACTERISTICS

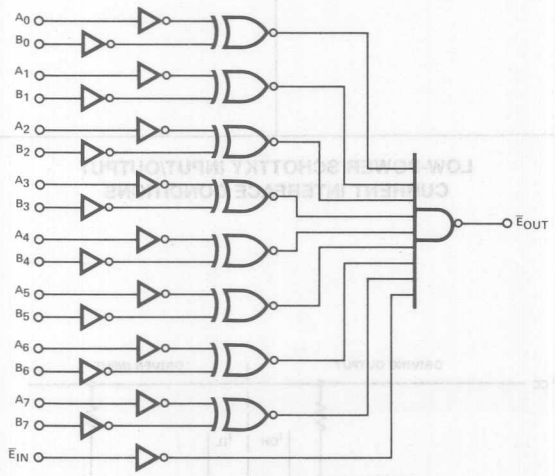
- 8-bit byte oriented equal-to comparator
- Cascadable using $\overline{E}_{IN}$
- High-speed, Low-Power Schottky technology
- $t_{pd}$ $A \odot B$ to $\overline{E}_{OUT}$ in 9ns
- Standard 20-pin package
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

The AmZ8121 is an 8-bit "equal to" comparator capable to comparing two 8-bit words for "equal to" with provision for expansion or external enabling. The matching of the two 8-bit inputs plus a logic LOW on the $\overline{E}_{IN}$ produces an active LOW on the output $\overline{E}_{OUT}$.

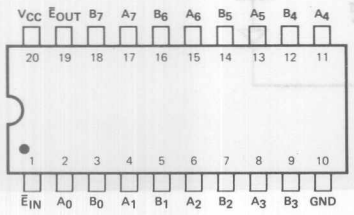
The logic expression for the device can be expressed as: $\overline{E}_{OUT} = \overline{(A_0 \odot B_0)\ (A_1 \odot B_1)\ (A_2 \odot B_2)\ (A_3 \odot B_3)\ (A_4 \odot B_4)\ (A_5 \odot B_5)\ (A_7 \odot B_7)\ E_{IN}}$. It is obvious that the expression is valid where $A_0 - A_7$ and $B_0 - B_7$ are expressed as either assertions or negations. This is also true for pair of terms i.e. $A_0$ can be compared with $B_0$ at the same time $\overline{A}_1$ is compared with $\overline{B}_1$. It is only essential that the polarity of the paired terms be maintained.

### LOGIC DIAGRAM




BLI-184

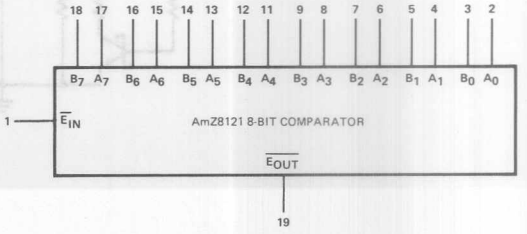
### CONNECTION DIAGRAM




Note: Pin 1 is marked for orientation

BLI-185

### LOGIC SYMBOL




$V_{CC}$ = Pin 20
GND = Pin 10

BLI-186

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

| | | | | | |
|---|---|---|---|---|---|
| COM'L | $T_A = 0°C$ to $+70°C$ | $V_{CC} = 5.0V \pm 5\%$ | MIN. = 4.75 V | MAX. = 5.25 V |
| MIL | $T_A = -55°C$ to $+125°C$ | $V_{CC} = 5.0V \pm 10\%$ | MIN. = 4.50 V | MAX. = 5.50 V |

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$, $I_{OH} = -440\mu A$ | | MIL | 2.5 | | | Volts |
| | | | | COM'L | 2.7 | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 4.0mA$ | | | | 0.4 | Volts |
| | | | $I_{OL} = 8.0mA$ | | | | 0.45 | |
| | | | $I_{OL} = 12mA$ | | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | MIL | | | 0.7 | Volts |
| | | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | $A_i$, $B_i$ | | | −0.36 | mA |
| | | | | $\overline{E}$ | | | −0.72 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | $A_i$, $B_i$ | | | 20 | μA |
| | | | | $\overline{E}$ | | | 40 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | $A_i$, $B_i$ | | | 0.1 | mA |
| | | | | $\overline{E}$ | | | 0.2 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | | 27 | 40 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. $\overline{E}$ = GND, all other inputs and outputs open.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for High Output State | −0.5V to $+V_{CC}$ max. |
| DC Input Voltage | −0.5V to +7.0V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

8

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | $A_i$ or $B_i$ to $\overline{Equal}$ | | 9 | 15 | ns | $C_L$ = 15pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 9 | 15 | | |
| $t_{PLH}$ | $\overline{E}$ to $\overline{Equal}$ | | 5 | 7 | ns | |
| $t_{PHL}$ | | | 6 | 8 | | |

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

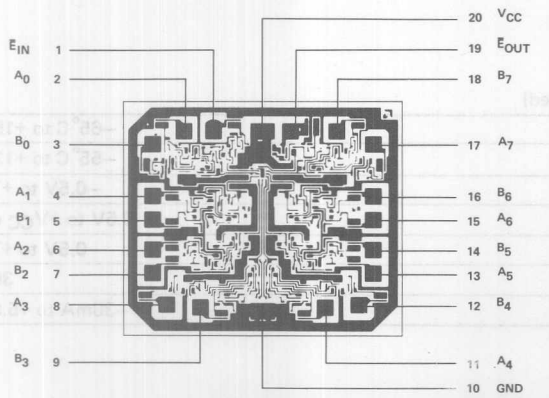
| Parameters | Description | COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | COM'L Max. | MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | $A_i$ or $B_i$ to $\overline{Equal}$ Output | | 20 | | 22 | ns | $C_L$ = 50pF, $R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 19 | | 21 | | |
| $t_{PLH}$ | $\overline{E}$ to $\overline{Equal}$ Output | | 10.5 | | 12 | ns | |
| $t_{PHL}$ | | | 12.5 | | 15 | | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

### DEFINITION OF FUNCTIONAL TERMS

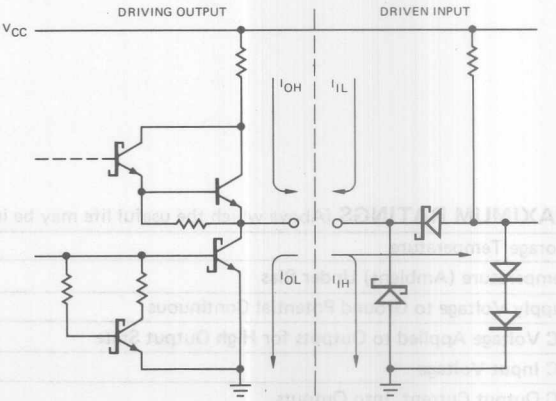
| | |
|---|---|
| $A_0$–$A_7$ | A input to comparator |
| $B_0$–$B_7$ | B input to comparator |
| $\overline{E}_{IN}$ | Enable active LOW |
| $\overline{E}_{OUT}$ | $\overline{EQUAL}$ output active LOW |

### METALLIZATION AND PAD LAYOUT




DIE SIZE 0.063" x 0.074"

### LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

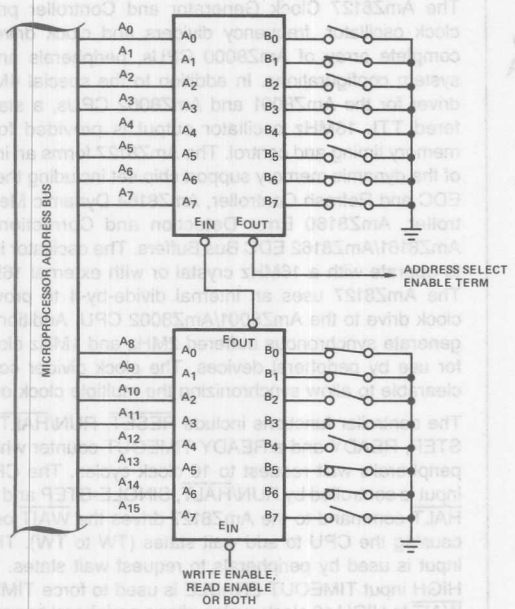



Note: Actual current flow direction shown.

BLI-187

## APPLICATIONS

### MICROPROCESSOR ENABLE CONTROLLED, SELECTABLE, ADDRESS DECODER

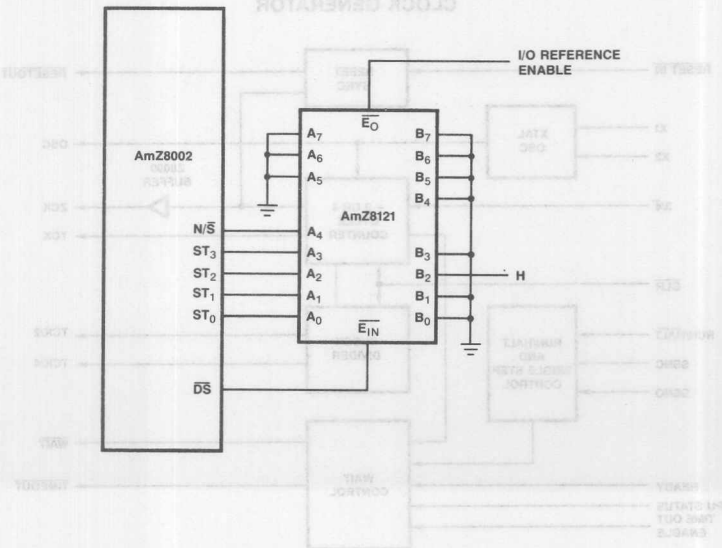



**MAX. $\overline{\text{ENABLE}}$ (HIGH-to-LOW) DELAY OVER 16-BITS**
**(Commercial Range)**

| | | |
|---|---|---|
| $t_{PHL}$ | $A_i$ or $B_i$ to $\overline{E}_{OUT}$ | 19ns |
| $t_{PHL}$ | $\overline{E}_{IN}$ to $\overline{E}_{OUT}$ | 12.5ns |
| Total | | 31.5ns |

BLI-188

### STATUS LINE DECODING




BLI-189

8

# AmZ8127

## AmZ8000 Clock Generator

**Advanced Information**

### DISTINCTIVE CHARACTERISTICS

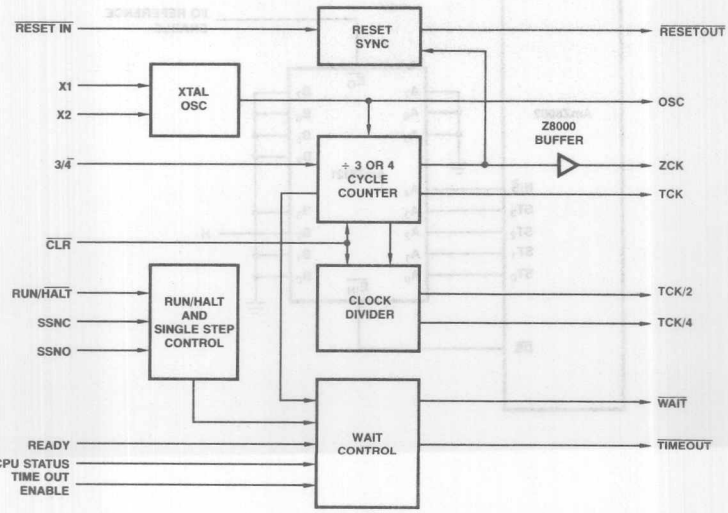
- **High-drive high-level clock output**
  Special output provides clock signal matched to requirements of AmZ8000 CPU, MMU and DMA devices.
- **Four TTL-level clocks**
  Generates synchronized TTL compatible clocks at 16MHz, 2MHz and 1MHz to drive memory circuits and LSI peripheral devices. An additional TTL clock is synchronized with the high-level clock for registers, latches and other peripherals.
- **Synchronized WAIT state and time-out controls**
  On-chip logic generates WAIT signal under control of Halt, Single-step and Ready signals. Automatic time-out of peripheral wait requests.

### FUNCTIONAL DESCRIPTION

The AmZ8127 Clock Generator and Controller provides the clock oscillator, frequency dividers and clock drivers for the complete array of AmZ8000 CPUs, peripherals and memory system configurations. In addition to the special 4MHz output driver for the AmZ8001 and AmZ8002 CPUs, a standard buffered TTL 16MHz oscillator output is provided for dynamic memory timing and control. The AmZ8127 forms an integral part of the dynamic memory support chip set including the AmZ8163 EDC and Refresh Controller, AmZ8164 Dynamic Memory Controller, AmZ8160 Error Detection and Correction Unit and AmZ8161/AmZ8162 EDC Bus Buffers. The oscillator is designed to operate with a 16MHz crystal or with external 16MHz drive. The AmZ8127 uses an internal divide-by-4 to provide 4MHz clock drive to the AmZ8001/AmZ8002 CPU. Additional dividers generate synchronous buffered 2MHz and 1MHz clock outputs for use by peripheral devices. The clock divider counters are clearable to allow synchronizing the multiple clock outputs.

The controller functions include $\overline{\text{RESET}}$, RUN/$\overline{\text{HALT}}$, SINGLE-STEP, READY and a READY TIMEOUT counter which limits a peripheral's wait request to 16 clock cycles. The CPU's $\overline{\text{WAIT}}$ input is controlled by RUN/$\overline{\text{HALT}}$, SINGLE-STEP and READY. A $\overline{\text{HALT}}$ command to the AmZ8127 drives the $\overline{\text{WAIT}}$ output LOW causing the CPU to add wait states (TW to TW). The READY input is used by peripherals to request wait states. The active HIGH input TIMEOUT ENABLE is used to force TIMEOUT and $\overline{\text{WAIT}}$ to HIGH 16 clock cycles after a peripheral has requested a wait but fails to release the request. The CPU status lines ST1, ST2 and ST3 are decoded in the AmZ8127 to disable the TIME-OUT counter during CPU "Internal Operations" and during refresh.

### BLOCK DIAGRAM
### CLOCK GENERATOR




BLI-168

# AmZ8133 • AmZ8173

## Octal Latches with Three-State Outputs

### DISTINCTIVE CHARACTERISTICS

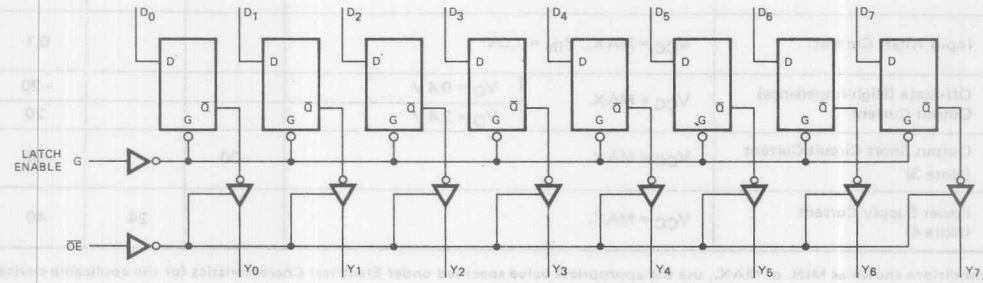
- 18ns max data in to data out
- Non-inverting AmZ8173, inverting AmZ8133
- Three-state outputs interface directly with bus organized systems
- Hysteresis on latch enable input for improved noise margin
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

The AmZ8133 and AmZ8173 are octal latches with three-state outputs for bus organized system applications. The latches appear to be transparent to the data (data changes asynchronously) when latch enable, G, is HIGH. When G is LOW, the data that meets the set-up times is latched. Data appears on the bus when the output enable, $\overline{OE}$, is LOW. When $\overline{OE}$ is HIGH the bus output is in the high-impedance state.

The AmZ8173 has non-inverted data inputs while the AmZ8133 is inverting.

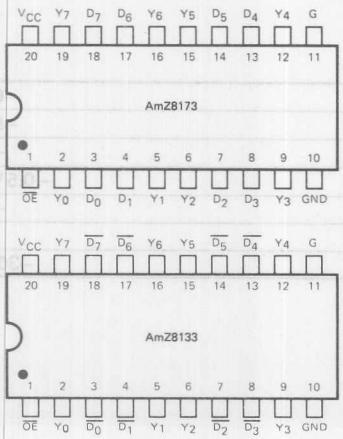
### LOGIC DIAGRAM
### AmZ8173




Inputs $D_0$ through $D_7$ are inverted on the AmZ8133.

BLI-041

### CONNECTION DIAGRAMS
### Top Views




Note: Pin 1 is marked for orientation.

BLI-042

### LOGIC SYMBOL




BLI-043

$V_{CC}$ = Pin 20
GND = Pin 10

Inputs $D_0$ through $D_7$ are inverted on the AmZ8133.

8

## AmZ8133 • AmZ8173
## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

### DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OH} = -1.0mA$ | MIL | 2.4 | 3.4 | | Volts |
| | | | $I_{OH} = -2.6mA$ | COM'L | 2.4 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 12mA$ | | | | 0.4 | Volts |
| | | | $I_{OL} = 24mA$ | | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | MIL | | | 0.7 | Volts |
| | | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | | −0.4 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | | 0.1 | mA |
| $I_{OZ}$ | Off-State (High-Impedance) Output Current | $V_{CC}$ = MAX. | $V_O = 0.4V$ | | | | −20 | μA |
| | | | $V_O = 2.4V$ | | | | 20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | | −30 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | | 24 | 40 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Inputs grounded; outputs open.

### MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5 V to +7.0 V |
| DC Voltage Applied to Outputs for High Output State | −0.5 V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5 V to +7.0 V |
| DC Output Current, Into Outputs | 30 mA |
| DC Input Current | −30 mA to +5.0 mA |

## AmZ8133
## SWITCHING CHARACTERISTICS
($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Enable to Output | | 20 | 30 | ns | $C_L$ = 45pF, $R_L$ = 667Ω |
| $t_{PHL}$ | | | 18 | 30 | | |
| $t_{PLH}$ | Data Input to Output | | 13 | 20 | ns | |
| $t_{PHL}$ | | | 15 | 23 | | |
| $t_s$(H) | HIGH Data to Enable | 3 | | | ns | |
| $t_s$(L) | LOW Data to Enable | 0 | | | | |
| $t_h$(H) | HIGH Data to Enable | 13 | | | ns | |
| $t_h$(L) | LOW Data to Enable | 7 | | | | |
| $t_{pw}$ | Enable Pulse Width | 15 | | | ns | |
| $t_{ZH}$ | $\overline{OE}$ to $Y_i$ | | | 28 | ns | |
| $t_{ZL}$ | | | | 36 | | |
| $t_{HZ}$ | $\overline{OE}$ to $Y_i$ | | | 20 | ns | $C_L$ = 5pF, $R_L$ = 667Ω |
| $t_{LZ}$ | | | | 25 | | |

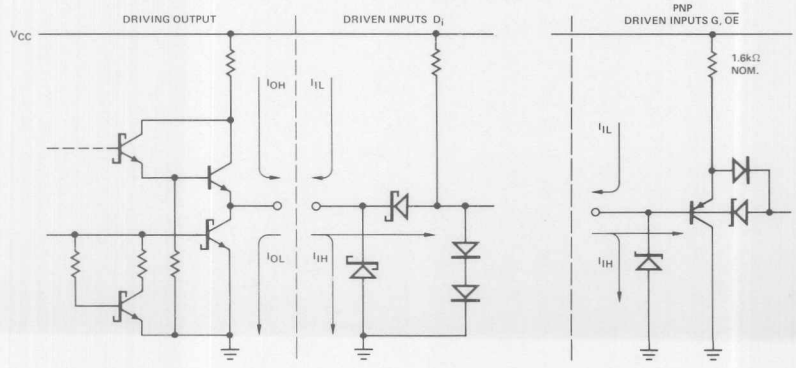
## AmZ8133
## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | COM'L Max. | MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Enable to Output | | 35 | | 40 | ns | $C_L$ = 45pF, $R_L$ = 667Ω |
| $t_{PHL}$ | | | 35 | | 40 | | |
| $t_{PLH}$ | Data Input to Output | | 20 | | 21 | ns | |
| $t_{PHL}$ | | | 25 | | 30 | | |
| $t_s$(H) | HIGH Data to Enable | 5 | | 5 | | ns | |
| $t_s$(L) | LOW Data to Enable | 0 | | 0 | | | |
| $t_h$(H) | HIGH Data to Enable | 14 | | 15 | | ns | |
| $t_h$(L) | LOW Data to Enable | 9 | | 10 | | | |
| $t_{pw}$ | Enable Pulse Width | 17 | | 20 | | ns | |
| $t_{ZH}$ | $\overline{OE}$ to $Y_i$ | | 28 | | 28 | ns | |
| $t_{ZL}$ | | | 36 | | 36 | | |
| $t_{HZ}$ | $\overline{OE}$ to $Y_i$ | | 33 | | 36 | ns | $C_L$ = 5pF, $R_L$ = 667Ω |
| $t_{LZ}$ | | | 33 | | 36 | | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

8

### LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

BLI-044

| Parameters | Description | Min | Typ | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Enable to Output | | 20 | 30 | ns | $C_L$ = 45pF<br>$R_L$ = 667Ω |
| $t_{PHL}$ | | | 18 | 30 | | |
| $t_{PLH}$ | Data Input to Output | | 10 | 18 | ns | |
| $t_{PHL}$ | | | 12 | 18 | | |
| $t_s(H)$ | HIGH Data to Enable | 0 | | | ns | |
| $t_s(L)$ | LOW Data to Enable | 0 | | | | |
| $t_h(H)$ | HIGH Data to Enable | 10 | | | ns | |
| $t_h(L)$ | LOW Data to Enable | 10 | | | | |
| $t_{pw}$ | Enable Pulse Width | 15 | | | ns | |
| $t_{ZH}$ | $\overline{OE}$ to $Y_i$ | | | 28 | ns | |
| $t_{ZL}$ | | | | 36 | | |
| $t_{HZ}$ | $\overline{OE}$ to $Y_i$ | | | 20 | ns | $C_L$ = 5pF<br>$R_L$ = 667Ω |
| $t_{LZ}$ | | | | 25 | | |

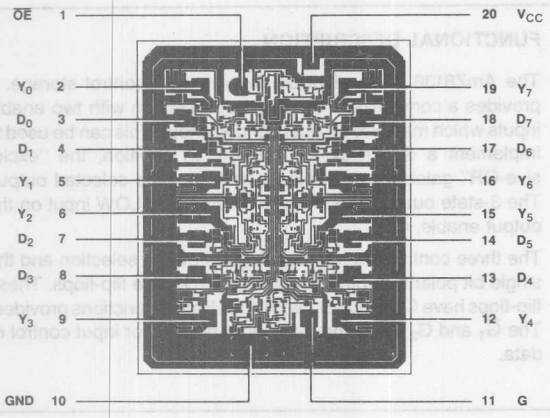
## AmZ8173 SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | COM'L<br>$T_A$ = 0°C to +70°C<br>$V_{CC}$ = 5.0V ±5% | | MIL<br>$T_A$ = –55°C to +125°C<br>$V_{CC}$ = 5.0V ±10% | | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $t_{PLH}$ | Enable to Output | | 35 | | 40 | ns | $C_L$ = 45pF<br>$R_L$ = 667Ω |
| $t_{PHL}$ | | | 35 | | 40 | | |
| $t_{PLH}$ | Data Input to Output | | 19 | | 20 | ns | |
| $t_{PHL}$ | | | 20 | | 25 | | |
| $t_s(H)$ | HIGH Data to Enable | 0 | | 0 | | ns | |
| $t_s(L)$ | LOW Data to Enable | 0 | | 0 | | | |
| $t_h(H)$ | HIGH Data to Enable | 11 | | 12 | | ns | |
| $t_h(L)$ | LOW Data to Enable | 15 | | 17 | | | |
| $t_{pw}$ | Enable Pulse Width | 17 | | 20 | | ns | |
| $t_{ZH}$ | $\overline{OE}$ to $Y_i$ | | 28 | | 28 | ns | |
| $t_{ZL}$ | | | 36 | | 36 | | |
| $t_{HZ}$ | $\overline{OE}$ to $Y_i$ | | 33 | | 36 | ns | $C_L$ = 5pF<br>$R_L$ = 667Ω |
| $t_{LZ}$ | | | 33 | | 36 | | |

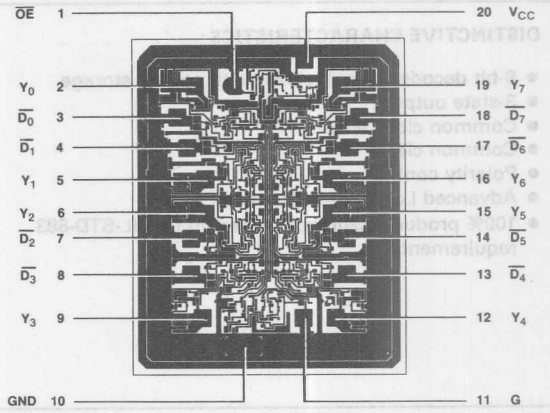
*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## Metallization and Pad Layouts

AmZ8173




AmZ8133




DIE SIZE 0.073" X 0.089"

## FUNCTION TABLES

### AmZ8173

| Inputs | | | Internal | Outputs | Function |
|---|---|---|---|---|---|
| $\overline{OE}$ | G | $D_i$ | $Q_i$ | $Y_i$ | |
| H | X | X | X | Z | Hi-Z |
| L | H | L | H | L | Transparent |
| L | H | H | L | H | |
| L | L | X | NC | NC | Latched |

### AmZ8133

| Inputs | | | Internal | Outputs | Function |
|---|---|---|---|---|---|
| $\overline{OE}$ | G | $\overline{D_i}$ | $Q_i$ | $Y_i$ | |
| H | X | X | X | Z | Hi-Z |
| L | H | L | H | H | Transparent |
| L | H | H | L | L | |
| L | L | X | NC | NC | Latched |

H = HIGH
L = LOW
X = Don't Care

NC = No Change
Z = High Impedance

## DEFINITION OF FUNCTIONAL TERMS

### AmZ8173

**$D_i$** The latch data inputs.

**G** The latch enable input. The latches are transparent when G is HIGH. Input data is latched on the HIGH-to-LOW transition.

**$Y_i$** The three-state latch outputs.

**$\overline{OE}$** The output enable control. When $\overline{OE}$ is LOW, the outputs $Y_i$ are enabled. When $\overline{OE}$ is HIGH, the outputs $Y_i$ are in the high-impedance (off) state.

### AmZ8133

**$\overline{D_i}$** The latch inverting data inputs.

**G** The latch enable input. The latches are transparent when G is HIGH. Input data is latched on the HIGH-to-LOW transition.

**$Y_i$** The three-state latch outputs.

**$\overline{OE}$** The output enable control. When $\overline{OE}$ is LOW, the inverted outputs $Y_i$ are enabled. When $\overline{OE}$ is HIGH, the outputs $Y_i$ are in the high-impedance (off) state.

8

# AmZ8136

## Eight-Bit Decoder With Control Storage

### DISTINCTIVE CHARACTERISTICS

- 8-bit decoder/demultiplexer with control storage
- 3-state outputs
- Common clock enable
- Common clear
- Polarity control
- Advanced Low Power Schottky Process
- 100% product assurance screening to MIL-STD-883 requirements

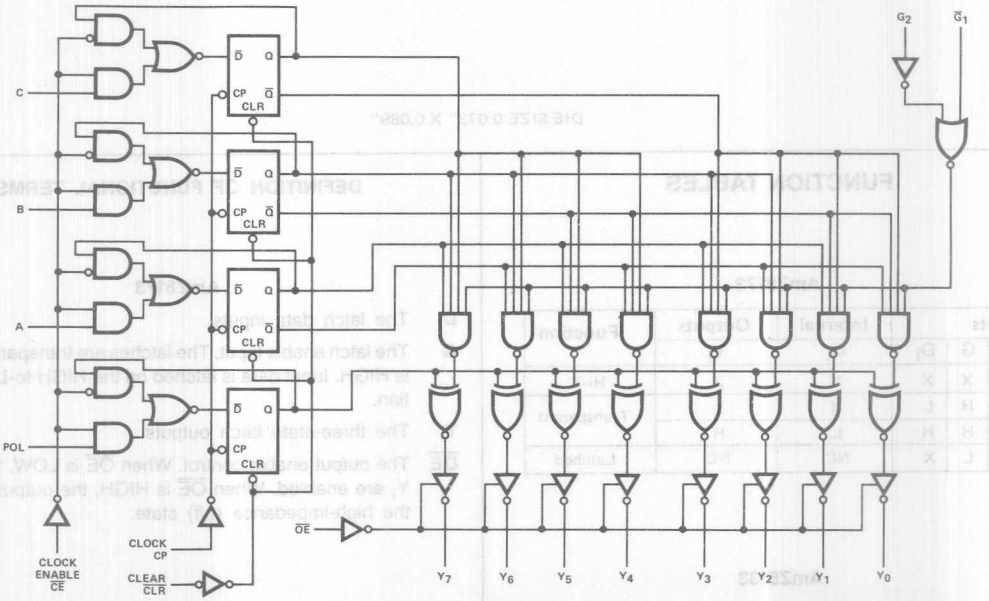
### FUNCTIONAL DESCRIPTION

The AmZ8136 is an eight-bit decoder with control storage. It provides a conventional 8-bit decoder function with two enable inputs which may also be used for data input. This can be used to implement a demultiplexer function. In addition, the "exclusive-OR" gates provide polarity control of the selected output. The 3-state outputs are enabled by an active LOW input on the output enable, $\overline{OE}$.

The three control bits representing the output selection and the single bit polarity control are stored in "D" type flip-flops. These flip-flops have Clear, Clock, and Clock Enable functions provided. The $\overline{G}_1$ and $G_2$ inputs provide either polarity for input control or data.

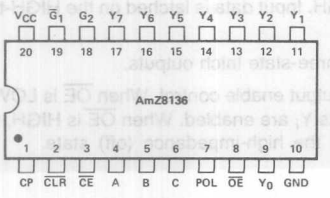
### LOGIC DIAGRAM

**8-Bit Decoder/Demultiplexer with Control Storage**




BLI-190

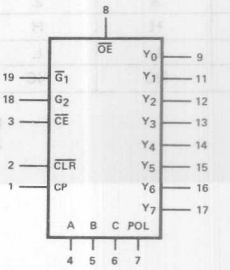
### CONNECTION DIAGRAM




Note: Pin 1 is marked for orientation.

BLI-191

### LOGIC SYMBOL




BLI-192

$V_{CC}$ = 20
GND = 10

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75 V MAX. = 5.25 V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50 V MAX. = 5.50 V

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OH} = -2.6mA$, COM'L | | 2.4 | 3.2 | | Volts |
| | | | $I_{OH} = -1.0mA$, MIL | | 2.4 | 3.4 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL} = 24mA$, COM'L | | | 0.4 | 0.5 | Volts |
| | | | $I_{OL} = 12mA$, MIL | | | 0.35 | 0.4 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | MIL | | | 0.7 | Volts |
| | | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN} = -18mA$ | | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN} = 0.4V$ | | | | | −0.4 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 2.7V$ | | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN} = 7.0V$ | | | | | 0.1 | mA |
| $I_O$ | Off-State (High-Impedance) Output Current | $V_{CC}$ = MAX. | $V_O = 0.4V$ | | | | −20 | μA |
| | | | $V_O = 2.4V$ | | | | 20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | | 37 | 56 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test Conditions: $A = B = C = \overline{G_1} = G_2 = \overline{OE} = \overline{CE} = GND$; $CLK = \overline{CLR} = POL = 4.5V$.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for High Output State | −0.5V to $+V_{CC}$ max. |
| DC Input Voltage | −0.5V to +7.0V |
| DC Output Current, Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

8

## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, $V_{CC}$ = 5.0V)

| Parameters | Description | | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | $\overline{G_1}$ to $Y_0 - Y_7$ | | | 17 | 25 | ns | $C_L$ = 45pF, $R_L$ = 667Ω |
| $t_{PLH}$ | | | | 23 | 34 | | |
| $t_{PLH}$ | $G_2$ to $Y_0 - Y_7$ | | | 20 | 30 | ns | |
| $t_{PHL}$ | | | | 26 | 39 | | |
| $t_{PLH}$ | CP to $Y_0 - Y_7$ | | | 24 | 36 | ns | |
| $t_{PHL}$ | | | | 30 | 45 | | |
| $t_{PLH}$ | $\overline{CLR}$ to $Y_0 - Y_7$ | | | 24 | 36 | ns | |
| $t_{PHL}$ | | | | 31 | 46 | | |
| $t_s$ | $\overline{CE}$ to CP | | 25 | | | ns | |
| $t_h$ | | | 0 | | | | |
| $t_s$ | A, B, C, POL to CP | | 15 | | | ns | |
| $t_h$ | | | 0 | | | | |
| $t_{HZ}$ | $\overline{OE}$ to $Y_0 - Y_7$ | | | 9 | 14 | ns | $C_L$ = 5pF, $R_L$ = 667Ω |
| $t_{LZ}$ | | | | 11 | 17 | | |
| $t_{ZH}$ | $\overline{OE}$ to $Y_0 - Y_7$ | | | 15 | 22 | ns | $C_L$ = 45pF, $R_L$ = 667Ω |
| $t_{ZL}$ | | | | 16 | 24 | | |
| $t_s$ | Set-up Time, Clear Recovery to CP | | 20 | | | ns | |
| $t_{pw}$ | Pulse Width | Clock | 15 | | | ns | |
| | | Clear | 15 | | | | |

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

| Parameters | Description | | COM'L $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ±5% Min. | COM'L Max. | MIL $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ±10% Min. | MIL Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | $\overline{G_1}$ to $Y_0 - Y_7$ | | | 29 | | 31 | ns | |
| $t_{PHL}$ | | | | 39 | | 42 | | |
| $t_{PLH}$ | $G_2$ to $Y_0 - Y_7$ | | | 34 | | 37 | ns | |
| $t_{PHL}$ | | | | 44 | | 48 | | |
| $t_{PLH}$ | CP to $Y_0 - Y_7$ | | | 40 | | 42 | ns | |
| $t_{PHL}$ | | | | 51 | | 55 | | $C_L$ = 45pF, $R_L$ = 667Ω |
| $t_{PLH}$ | $\overline{CLR}$ to $Y_0 - Y_7$ | | | 47 | | 54 | ns | |
| $t_{PHL}$ | | | | 58 | | 66 | | |
| $t_s$ | $\overline{CE}$ to CP | | 27 | | 30 | | ns | |
| $t_h$ | | | 0 | | 0 | | | |
| $t_s$ | A, B, C, POL to CP | | 17 | | 20 | | ns | |
| $t_h$ | | | 0 | | 0 | | | |
| $t_{HZ}$ | $\overline{OE}$ to $Y_0 - Y_7$ | | | 17 | | 18 | ns | $C_L$ = 5.0pF, $R_L$ = 667Ω |
| $t_{LZ}$ | | | | 27 | | 34 | | |
| $t_{ZH}$ | $\overline{OE}$ to $Y_0 - Y_7$ | | | 25 | | 27 | ns | |
| $t_{ZL}$ | | | | 28 | | 30 | | $C_L$ = 5.0pF, $R_L$ = 667Ω |
| $t_s$ | Set-up Time, Clear Recovery to CP | | 23 | | 25 | | ns | |
| $t_{pw}$ | Pulse Width | Clock | 17 | | 20 | | ns | |
| | | Clear | 15 | | 15 | | | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## FUNCTION TABLE

| Mode | Inputs | | | | | | | | | Internal Registers | | | | Three-State Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | C | B | A | POL | $\overline{CE}$ | $\overline{CLR}$ | G* | $\overline{OE}$ | CP | $Q_C$ | $Q_B$ | $Q_A$ | $Q_{POL}$ | $Y_0$ | $Y_1$ | $Y_2$ | $Y_3$ | $Y_4$ | $Y_5$ | $Y_6$ | $Y_7$ |
| Clear | X | X | X | X | X | L | L | L | X | L | L | L | L | H | H | H | H | H | H | H | H |
| | X | X | X | X | X | L | H | L | X | L | L | L | L | L | H | H | H | H | H | H | H | H |
| Hold | X | X | X | X | H | H | NC | L | ↑ | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC | NC |
| Select | L | L | L | H | L | H | H | L | ↑ | L | L | L | H | H | L | L | L | L | L | L | L |
| | L | L | H | H | L | H | H | L | ↑ | L | L | H | H | L | H | L | L | L | L | L | L |
| | L | H | L | H | L | H | H | L | ↑ | L | H | L | H | L | L | H | L | L | L | L | L |
| | L | H | H | H | L | H | H | L | ↑ | L | H | H | H | L | L | L | H | L | L | L | L |
| | H | L | L | H | L | H | H | L | ↑ | H | L | L | H | L | L | L | L | H | L | L | L |
| | H | L | H | H | L | H | H | L | ↑ | H | L | H | H | L | L | L | L | L | H | L | L |
| | H | H | L | H | L | H | H | L | ↑ | H | H | L | H | L | L | L | L | L | L | H | L |
| | H | H | H | H | L | H | H | L | ↑ | H | H | H | H | L | L | L | L | L | L | L | H |
| | L | L | L | L | L | H | H | L | ↑ | L | L | L | L | L | H | H | H | H | H | H | H |
| | L | L | H | L | L | H | H | L | ↑ | L | L | H | L | H | L | H | H | H | H | H | H |
| | L | H | L | L | L | H | H | L | ↑ | L | H | L | L | H | H | L | H | H | H | H | H |
| | L | H | H | L | L | H | H | L | ↑ | L | H | H | L | H | H | H | L | H | H | H | H |
| | H | L | L | L | L | H | H | L | ↑ | H | L | L | L | H | H | H | H | L | H | H | H |
| | H | L | H | L | L | H | H | L | ↑ | H | L | H | L | H | H | H | H | H | L | H | H |
| | H | H | L | L | L | H | H | L | ↑ | H | H | L | L | H | H | H | H | H | H | L | H |
| | H | H | H | L | L | H | H | L | ↑ | H | H | H | L | H | H | H | H | H | H | H | L |
| | X | X | X | H | L | H | L | L | ↑ | X | X | X | H | L | L | L | L | L | L | L | L |
| | X | X | X | L | L | H | L | L | ↑ | X | X | X | L | H | H | H | H | H | H | H | H |
| Output Disable | X | X | X | X | X | X | X | H | X | NC | NC | NC | NC | Z | Z | Z | Z | Z | Z | Z | Z |

* 

| $\overline{G}_1$ | $G_2$ | G |
|---|---|---|
| L | L | L |
| L | H | H |
| H | L | L |
| H | H | L |

NC = No Change  X = Don't Care  Z = High-Impedance  ↑ = Low-to-High Transition

### DEFINITION OF TERMS

**$\overline{CLR}$** CLEAR – When the CLEAR input is LOW, the control register outputs ($Q_A$, $Q_B$, $Q_C$, $Q_{POL}$) are set LOW regardless of any other inputs.

**CP** CLOCK – Enters data into the control register on the LOW-to-HIGH transition.

**$\overline{CE}$** CLOCK ENABLE – Allows data to enter the control register when $\overline{CE}$ is LOW. When $\overline{CE}$ is HIGH, the $Q_i$ outputs do not change state, regardless of data or clock input transitions.

**A,B,C** Inputs to the control register which are entered on the LOW-to-HIGH clock transition if $\overline{CE}$ is LOW.

**POL** Input to the control register bit used for determining the polarity of the selected output.

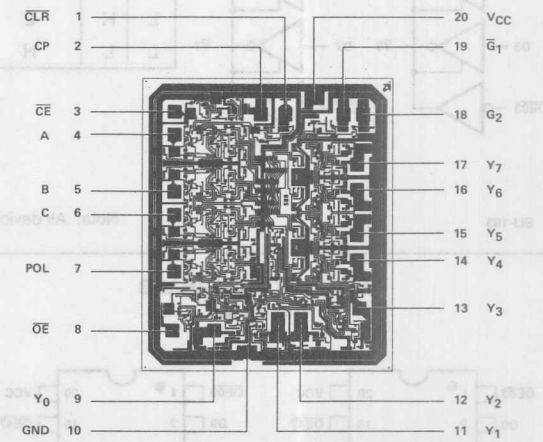
**$\overline{G}_1$** Active LOW part of the expression $G = G_1G_2$ [or $G = (\overline{G}_1)\,G_2$] where G is either data input for the selected $Y_n$ or is used as an input enable.

**$G_2$** Active HIGH part of the expression $G = G_1G_2$.

**$Y_n$** The three-state outputs. When active ($\overline{OE}$ = LOW), one of eight outputs is selected by the code stored in the control register, with the polarity of all eight determined by the bit stored in the POL flip-flop of the control register. The selected output can further be controlled by G according to the expression $Y_{SELECTED} = \overline{G \oplus Q_{POL}}$.

**$\overline{OE}$** OUTPUT ENABLE. When $\overline{OE}$ is HIGH the $Y_n$ outputs are in the high impedance state; when $\overline{OE}$ is LOW the $Y_n$'s are in their active state as determined by the other control logic. The $\overline{OE}$ input affects the $Y_n$ output buffers only and has no effect on the control register or any other logic.

### METALLIZATION AND PAD LAYOUT




DIE SIZE 0.084" X 0.099"

8

# AmZ8140 • AmZ8144

## Octal Three-State Buffers

### DISTINCTIVE CHARACTERISTICS

- Three-state outputs drive bus lines directly
- Hysteresis at inputs inproves noise margin
- PNP inputs reduce DC loading on bus lines
- Data-to-output propagation delay times – 16ns MAX
- Enable-to-output – 20ns MAX
- 48mA output current
- 20-pin hermetic and molded DIP packages
- 100% product assurance testing to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

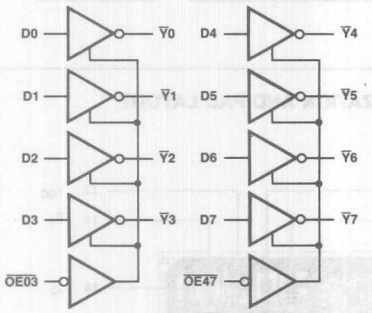
The AmZ8140 and AmZ8144 are octal buffers fabricated using advanced low-power Schottky technology. The 20-pin package provides improved printed circuit board density for use in memory address and clock driver applications.

Three-state outputs are provided to drive bus lines directly. The AmZ8140 and AmZ8144 are specified at 48mA and 24mA output sink current. Four buffers are enabled from one common line and the other four from a second enable line. The AmZ8140 and AmZ8144 enables are of similar polarity for use as a unidirectional buffer in which both halves are enabled simultaneously.

Improved noise rejection and high fan-out are provided by input hysteresis and low current PNP inputs.

### LOGIC DIAGRAMS

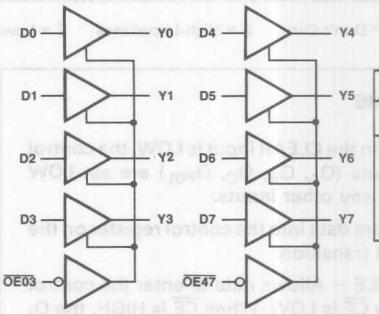
**AmZ8140**




| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | D | Y |
| H | X | Z |
| L | H | L |
| L | L | H |

BLI-193

**AmZ8144**

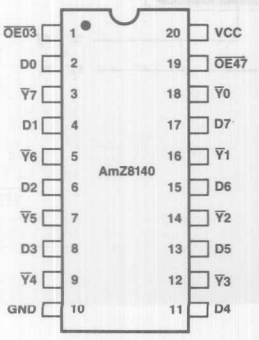



| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{OE}$ | $D_i$ | Y |
| H | X | Z |
| L | H | H |
| L | L | L |

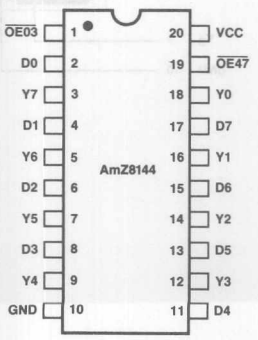
BLI-194

Note: All devices have input hysteresis.

### CONNECTION DIAGRAMS
**Top Views**



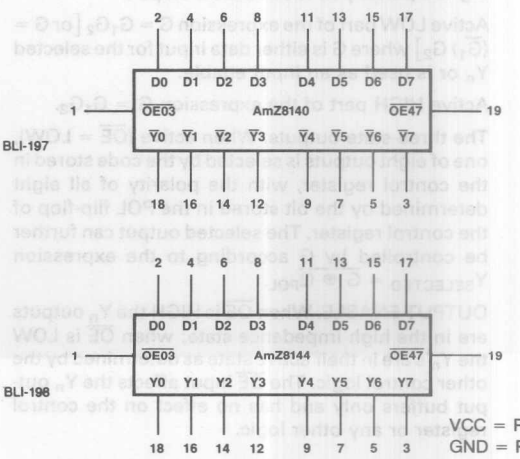

BLI-195




BLI-196

Note: Pin 1 is marked for orientation.

### LOGIC SYMBOLS




VCC = Pin 20
GND = Pin 10

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

| | | | |
|---|---|---|---|
| COM'L | $T_A$ = 0 to 70°C | VCC = 5.0V ±5% | (MIN = 4.75V MAX = 5.25V) |
| MIL | $T_A$ = −55 to +125°C | VCC = 5.0V ±10% | (MIN = 4.50V MAX = 5.50V) |

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | | Test Conditions (Note 1) | | Min | Typ (Note 2) | Max | Units |
|---|---|---|---|---|---|---|---|---|
| VOH | High-Level Output Voltage | | VCC = MIN, VIH = 2.0V, IOH = −3.0mA, VIL = VIL MAX | | 2.4 | 3.4 | | Volts |
| | | | VCC = MIN, VIL = 0.5V | MIL, IOH = −12mA | 2.0 | | | |
| | | | | COM'L, IOH = −15mA | 2.0 | | | |
| VOL | Low-Level Output Voltage | | VCC = MIN | All IOL = 12mA | | 0.25 | 0.4 | Volts |
| | | | | All IOL = 24mA | | 0.35 | 0.5 | |
| | | | | COM'L, IOL = 48mA | | | 0.55 | |
| VIH | High-Level Input Voltage | | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| VIL | Low-Level Input Voltage | COM'L | | | | | 0.8 | Volts |
| | | MIL | | | | | 0.7 | |
| VIK | Input Clamp Voltage | | VCC = MIN, II = −18mA | | | | −1.5 | Volts |
| | Hysteresis (VT+ − VT−) | | VCC = MIN | | 0.2 | 0.4 | | Volts |
| IOZH | Off-State Output Current, High-Level Voltage Applied | | VCC = MAX, VIH = 2.0V, VIL = VIL MAX | VO = 2.7V | | | 20 | µA |
| IOZL | Off-State Output Current, Low-Level Voltage Applied | | | VO = 0.4V | | | −20 | |
| II | Input Current at Maximum Input Voltage | | VCC = MAX, VI = 7.0V | | | | 0.1 | mA |
| IIH | High-Level Input Current, Any Input | | VCC = MAX, VIH = 2.7V | | | | 20 | µA |
| IIL | Low-Level Input Current | | VCC = MAX, VIL = 0.4V | | | | −200 | µA |
| ISC | Short Circuit Output Current (Note 3) | | VCC = MAX | | −50 | | −225 | mA |
| ICC | Supply Current VCC = MAX Outputs Open | AmZ8140 | All Outputs HIGH | | | 13 | 23 | mA |
| | | | All Outputs LOW | | | 26 | 44 | |
| | | | Outputs at Hi-Z | | | 29 | 50 | |
| ICC | | AmZ8144 | All Outputs HIGH | | | 13 | 23 | mA |
| | | | All Outputs LOW | | | 27 | 46 | |
| | | | Outputs at Hi-Z | | | 32 | 54 | |

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
2. All typical values are VCC = 5.0V, $T_A$ = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short-circuits should not exceed one second.

8

## MAXIMUM RATINGS above which the useful life may be impaired

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +7.0V |
| DC Output Current | 150mA |
| DC Input Current | −30mA to +5.0mA |

## AmZ8140 • AmZ8144
## SWITCHING CHARACTERISTICS
($T_A$ = +25°C, VCC = 5.0V)

| Parameters | Description | AmZ8140 Min | AmZ8140 Typ | AmZ8140 Max | AmZ8144 Min | AmZ8144 Typ | AmZ8144 Max | Units | Test Conditions (Notes 1-5) |
|---|---|---|---|---|---|---|---|---|---|
| tPLH | Propagation Delay Time, Low-to-High-Level Output | | 6 | 10 | | 9 | 13 | ns | CL = 45pF RL = 667Ω |
| tPHL | Propagation Delay Time, High-to-Low-Level Output | | 9 | 13 | | 11 | 16 | ns | |
| tPZL | Output Enable Time to Low Level | | 13 | 20 | | 13 | 20 | ns | |
| tPZH | Output Enable Time to High Level | | 8 | 14 | | 8 | 14 | ns | |
| tPLZ | Output Disable Time from Low Level | | 13 | 20 | | 13 | 20 | ns | CL = 5.0pF RL = 667Ω |
| tPHZ | Output Disable Time from High Level | | 12 | 18 | | 12 | 18 | ns | |

## AmZ8140
## SWITCHING CHARACTERISTICS
## OVER OPERATING RANGE*

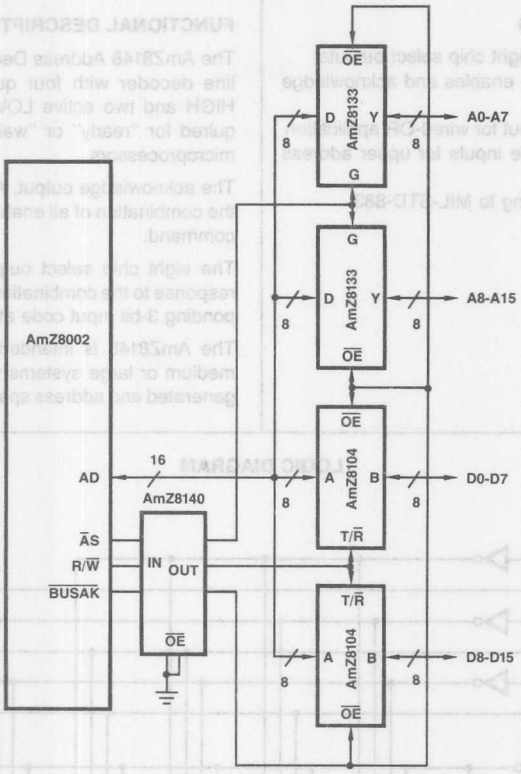
| Parameters | Description | COM'L $T_A$ = 0 to 70°C VCC = 5.0V ±5% Min | COM'L Max | MIL $T_A$ = −55 to +125°C VCC = 5.0V ±10% Min | MIL Max | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| tPLH | Propagation Delay Time, Low-to-High-Level Output | | 13 | | 15 | ns | CL = 45pF RL = 667Ω |
| tPHL | Propagation Delay Time, High-to-Low-Level Output | | 15 | | 18 | ns | |
| tPZL | Output Enable Time to Low Level | | 25 | | 30 | ns | |
| tPZH | Output Enable Time to High Level | | 18 | | 21 | ns | |
| tPLZ | Output Disable Time from Low Level | | 25 | | 30 | ns | CL = 5.0pF RL = 667Ω |
| tPHZ | Output Disable Time from High Level | | 21 | | 25 | ns | |

## AmZ8144
## SWITCHING CHARACTERISTICS
## OVER OPERATING RANGE*

| Parameters | Description | COM'L $T_A$ = 0 to 70°C VCC = 5.0V ±5% Min | COM'L Max | MIL $T_A$ = −55 to +125°C VCC = 5.0V ±10% Min | MIL Max | Units | Test Conditions |
|---|---|---|---|---|---|---|---|
| tPLH | Propagation Delay Time, Low-to-High-Level Output | | 15 | | 16 | ns | CL = 45pF RL = 667Ω |
| tPHL | Propagation Delay Time, High-to-Low-Level Output | | 18 | | 20 | ns | |
| tPZL | Output Enable Time to Low Level | | 25 | | 30 | ns | |
| tPZH | Output Enable Time to High Level | | 18 | | 21 | ns | |
| tPLZ | Output Disable Time from Low Level | | 25 | | 30 | ns | CL = 5.0pF RL = 667Ω |
| tPHZ | Output Disable Time from High Level | | 21 | | 25 | ns | |

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

## APPLICATION

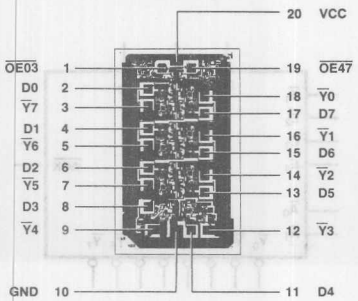



BLI-199

8

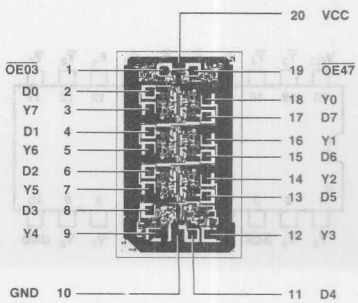
## METALLIZATION AND PAD LAYOUTS

### AmZ8140




DIE SIZE 0.060" X 0.103"

### AmZ8144




DIE SIZE 0.060" X 0.103"

# AmZ8148

## Chip Select Address Decoder With Acknowledge

### DISTINCTIVE CHARACTERISTICS

- One-of-Eight Decoder provides eight chip select outputs
- Acknowledge output responds to enables and acknowledge input command
- Open-collector Acknowledge output for wired-OR application
- Inverting and non-inverting enable inputs for upper address decoding
- 100% product assurance screening to MIL-STD-883 requirements

### FUNCTIONAL DESCRIPTION

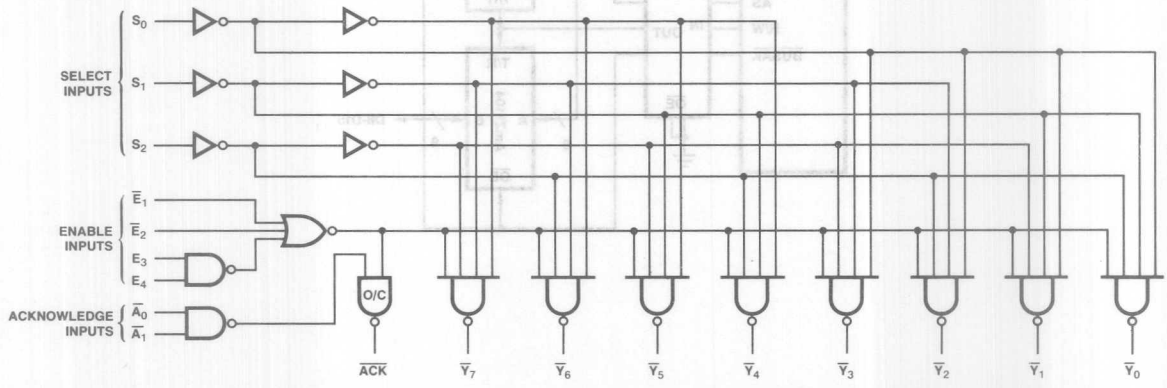
The AmZ8148 Address Decoder combines a three-line to eight-line decoder with four qualifying enable inputs (two active HIGH and two active LOW) and the acknowledge output required for "ready" or "wait state" control of all popular MOS microprocessors.

The acknowledge output, ACK, is active LOW and responds to the combination of all enables and an acknowledge active, input command.

The eight chip select outputs are individually active LOW in response to the combination of all enables active and the corresponding 3-bit input code at the S inputs.

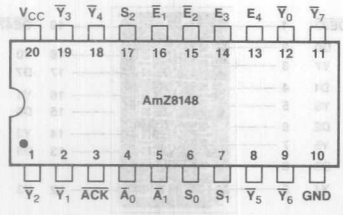
The AmZ8148 is intended for chip select decoding in small, medium or large systems where multiple chip selects must be generated and address space must be allocated conservatively.

### LOGIC DIAGRAM




BLI-045

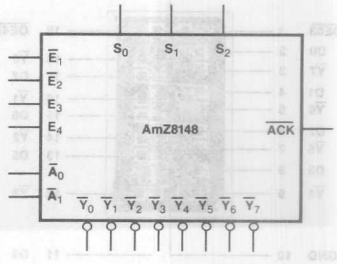
### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

BLI-046

### LOGIC SYMBOL




BLI-047

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A$ = 0°C to +70°C $V_{CC}$ = 5.0V ±5% (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A$ = −55°C to +125°C $V_{CC}$ = 5.0V ±10% (MIN. = 4.50V MAX. = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN. $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −440μA | 2.4 | 3.4 | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN. $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 4.0mA | | | 0.4 | Volts |
| | | | $I_{OL}$ = 8.0mA | | | 0.45 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | MIL | | | 0.7 | Volts |
| | | | COM'L | | | 0.8 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.4V | | | | −0.36 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 7.0V | | | | 0.1 | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −15 | | −85 | mA |
| $I_{CC}$ | Power Supply Current (Note 4) | $V_{CC}$ = MAX. | | | 15 | 20 | mA |

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. TEST CONDITIONS: $S_0 = S_1 = S_2 = \overline{E}_1 = \overline{E}_2$ = GND: $\overline{A}_0 = \overline{A}_1 = E_3 = E_4$ = 4.5V.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for High Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −0.5V to +7.0V |
| DC Output Current Into Outputs | 30mA |
| DC Input Current | −30mA to +5.0mA |

8

| | | | | | | |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | $S_i$ to $\overline{Y_i}$ (Three Level Delay) | | 14 | 20 | ns | |
| $t_{PHL}$ | | | 19 | 27 | ns | |
| $t_{PLH}$ | $S_i$ to $Y_i$ (Two Level Delay) | | 13 | 18 | ns | |
| $t_{PHL}$ | | | 15 | 21 | ns | |
| $t_{PLH}$ | $\overline{E_1}$, $\overline{E_2}$ to $\overline{Y_i}$ | | 13 | 18 | ns | |
| $t_{PHL}$ | | | 16 | 23 | ns | |
| $t_{PLH}$ | $E_3$, $E_4$ to $\overline{Y_i}$ | | 15 | 21 | ns | $C_L$ = 15pF<br>$R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 19 | 27 | ns | |
| $t_{PLH}$ | $\overline{A_i}$ to ACK | | 25 | 35 | ns | |
| $t_{PHL}$ | | | 16 | 22 | ns | |
| $t_{PLH}$ | $\overline{E_1}$, $\overline{E_2}$ to $\overline{ACK}$ | | 29 | 40 | ns | |
| $t_{PHL}$ | | | 25 | 35 | ns | |
| $t_{PLH}$ | $E_3$, $E_4$ to $\overline{ACK}$ | | 29 | 40 | ns | |
| $t_{PHL}$ | | | 25 | 35 | ns | |

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| | | COM'L | | MIL | | | |
|---|---|---|---|---|---|---|---|
| | | $T_A$ = 0°C to +70°C<br>$V_{CC}$ = 5.0V ±5% | | $T_A$ = −55°C to +125°C<br>$V_{CC}$ = 5.0V ±10% | | | |
| **Parameters** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** | **Test Conditions** |
| $t_{PLH}$ | $S_i$ to $Y_i$ (Three Level Delay) | | 27 | | 30 | ns | |
| $t_{PHL}$ | | | 34 | | 36 | ns | |
| $t_{PLH}$ | $S_i$ to $Y_i$ (Two Level Delay) | | 23 | | 25 | ns | |
| $t_{PHL}$ | | | 28 | | 31 | ns | |
| $t_{PLH}$ | $\overline{E_1}$, $\overline{E_2}$ to $\overline{Y_i}$ | | 23 | | 25 | ns | |
| $t_{PHL}$ | | | 29 | | 31 | ns | |
| $t_{PLH}$ | $E_3$, $E_4$ to $\overline{Y_i}$ | | 27 | | 28 | ns | $C_L$ = 50pF<br>$R_L$ = 2.0kΩ |
| $t_{PHL}$ | | | 34 | | 36 | ns | |
| $t_{PLH}$ | $\overline{A_i}$ to ACK | | 45 | | 45 | ns | |
| $t_{PHL}$ | | | 31 | | 35 | ns | |
| $t_{PLH}$ | $\overline{E_1}$, $\overline{E_2}$ to $\overline{ACK}$ | | 45 | | 45 | ns | |
| $t_{PHL}$ | | | 39 | | 40 | ns | |
| $t_{PLH}$ | $E_3$, $E_4$ to $\overline{ACK}$ | | 45 | | 45 | ns | |
| $t_{PHL}$ | | | 39 | | 40 | ns | |

## DEFINITION OF FUNCTIONAL TERMS

**$S_0$, $S_1$, $S_2$** Three-line to eight-line chip select decoder inputs.

**$\overline{E}_1$, $\overline{E}_2$** The active LOW enable inputs. A HIGH on either the $\overline{E}_1$ or $\overline{E}_2$ input forces all decoded functions to be disabled, and forces $\overline{ACK}$ HIGH.

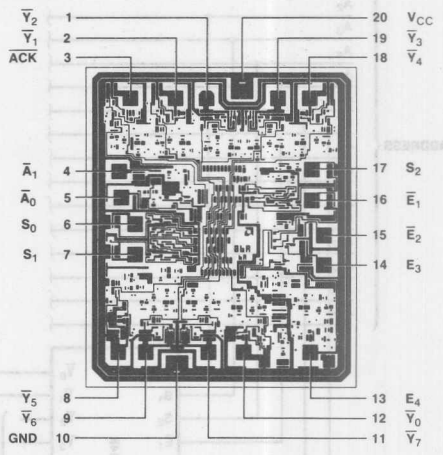
**$E_3$, $E_4$** The active HIGH enable inputs. A LOW on either $E_3$ or $E_4$ inputs forces all the decoded functions to be inhibited, and forces $\overline{ACK}$ HIGH.

**$A_0$, $A_1$** The acknowledge inputs, $A_0$ and $A_1$, are active LOW inputs used as conditions for an active LOW output at the acknowledge, $\overline{ACK}$, output.

**$\overline{ACK}$** The acknowledge output, $\overline{ACK}$, is an active LOW output used to signal the microprocessor that specific devices have been selected. $\overline{ACK}$ goes LOW only when $\overline{E}_1$ and $\overline{E}_2$ are LOW, $E_3$ and $E_4$ are HIGH and $\overline{A}_0$ or $\overline{A}_1$ is LOW.

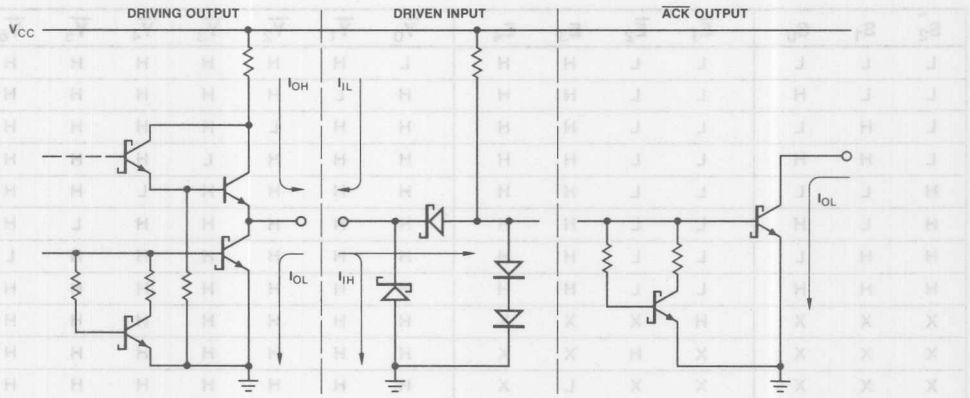
**$\overline{Y}_i$** The eight active LOW chip select outputs.

## METALLIZATION AND PAD LAYOUT




DIE SIZE: 0.081" X 0.096"

## LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

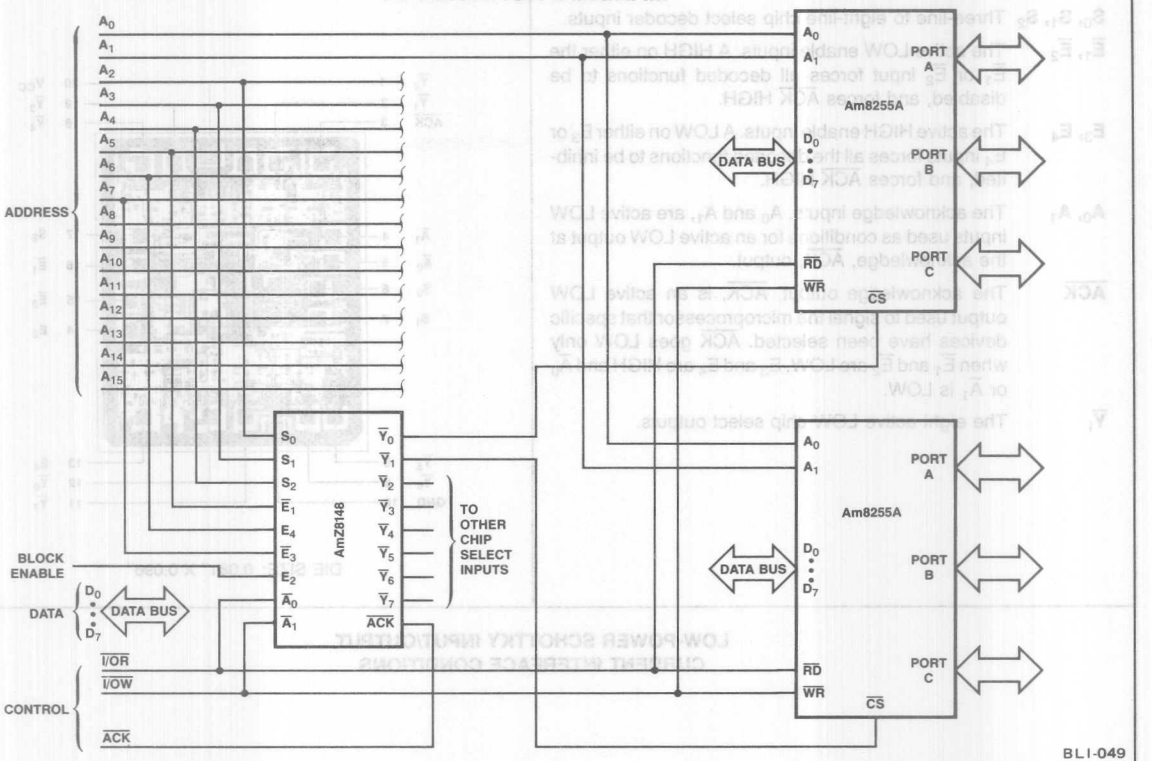



Note: Actual current flow direction shown.

BLI-048

8

## APPLICATION DIAGRAM




## FUNCTION TABLES

### CHIP SELECT OUTPUTS $Y_i$

| $S_2$ | $S_1$ | $S_0$ | $\overline{E}_1$ | $\overline{E}_2$ | $E_3$ | $E_4$ | $\overline{Y}_0$ | $\overline{Y}_1$ | $\overline{Y}_2$ | $\overline{Y}_3$ | $\overline{Y}_4$ | $\overline{Y}_5$ | $\overline{Y}_6$ | $\overline{Y}_7$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| L | L | L | L | L | H | H | L | H | H | H | H | H | H | H |
| L | L | H | L | L | H | H | H | L | H | H | H | H | H | H |
| L | H | L | L | L | H | H | H | H | L | H | H | H | H | H |
| L | H | H | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | L | L | L | H | H | H | H | H | H | L | H | H | H |
| H | L | H | L | L | H | H | H | H | H | H | H | L | H | H |
| H | H | L | L | L | H | H | H | H | H | H | H | H | L | H |
| H | H | H | L | L | H | H | H | H | H | H | H | H | H | L |
| X | X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| X | X | X | X | H | X | X | H | H | H | H | H | H | H | H |
| X | X | X | X | X | L | X | H | H | H | H | H | H | H | H |
| X | X | X | X | X | X | L | H | H | H | H | H | H | H | H |

### ACKNOWLEDGE OUTPUT $\overline{ACK}$

| $\overline{E}_1$ | $\overline{E}_2$ | $E_3$ | $E_4$ | $\overline{A}_0$ | $\overline{A}_1$ | $\overline{ACK}$ |
|---|---|---|---|---|---|---|
| H | X | X | X | X | X | H |
| X | H | X | X | X | X | H |
| X | X | L | X | X | X | H |
| X | X | X | L | X | X | H |
| L | L | H | H | L | X | L |
| L | L | H | H | X | L | L |

# AmZ8160

## Cascadable 16-Bit Error Detection and Correction Unit

## ADVANCED DATA

### DISTINCTIVE CHARACTERISTICS

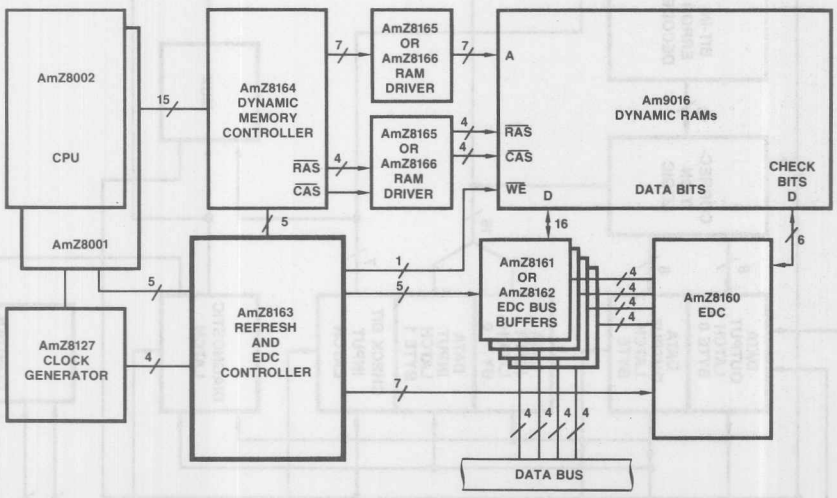
- Modified Hamming Code
  Detects multiple errors and corrects single bit errors in a parallel data word. Ideal for use in dynamic memory systems.
- Syndromes provided
  The AmZ8160 makes available the syndrome bits when an error occurs so the location of memory faults can be logged.
- Microprocessor compatible
  The AmZ8160 is designed to work with AmZ8000 microprocessor systems.
- Advanced circuit and process technologies
  Newest bipolar LSI techniques provide very high performance.
  Data-in to error detection typically 30ns
  Data-in to corrected data out typically 50ns
- Built-in Diagnostics
  Extra logic on the chip provides diagnostic functions to be used during device test and for system diagnostics.

### GENERAL DESCRIPTION

The AmZ8160 Error Detection and Correction Unit (EDC) contains the logic necessary to generate 6 check bits on a 16-bit data field according to a modified Hamming Code, and to correct the data word when check bits are supplied. Operating on data read from memory, the AmZ8160 will correct any single bit error and will detect all double on some triple bit errors. The AmZ8160 is expandable to operate on 32-bit words (7 check bits) and 64-bit words (8 check bits). In all configurations, the device makes the error syndrome available on separate outputs for data logging.

The AmZ8160 also features two diagnostic modes, in which diagnostic data can be forced into portions of the chip to simplify device testing and to execute system diagnostic functions. The product is supplied in a 48 lead hermetic DIP package.

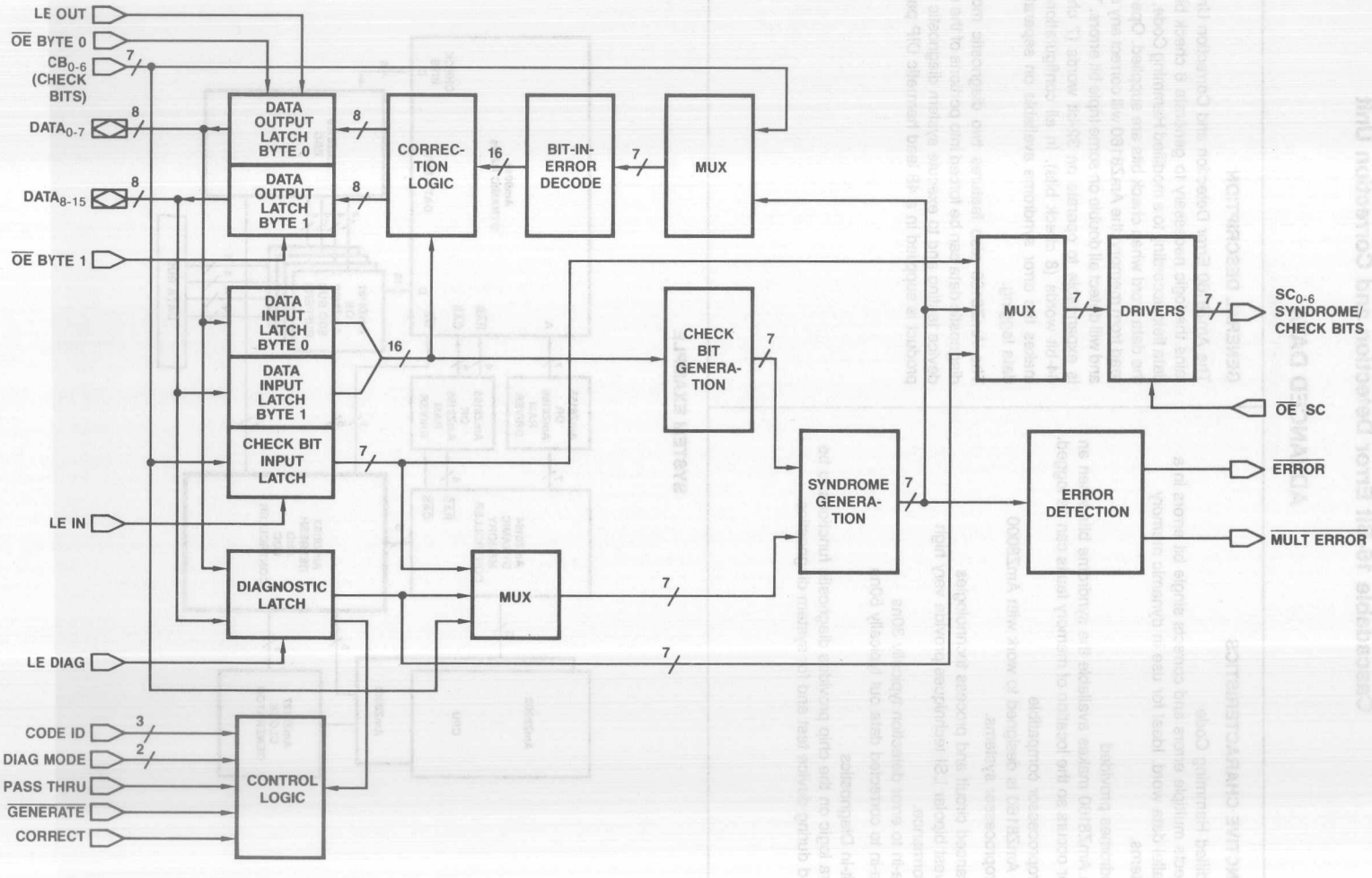
### SYSTEM EXAMPLE




BLI-200



8




BLOCK DIAGRAM

### EDC Architecture

The EDC Unit is a powerful 16-bit cascadable slice used for check bit generation, error detection, error correction and diagnostics.

As shown in the block diagram, the device consists of the following:

- Data Input Latch
- Check Bit Input Latch
- Check Bit Generation Logic
- Syndrome Generation Logic
- Error Detection Logic
- Error Correction Logic
- Data Output Latch
- Diagnostic Latch
- Control Logic

### Data Input Latch

16 bits of data are loaded from the bidirectional DATA lines under control of the Latch Enable input, LE IN. Depending on the control mode the input data is either used for check bit generation or error detection/correction.

### Check Bit Input Latch

Seven check bits are loaded under control of LE IN. Check bits are used in the Error Detection and Error Correction modes.

### Check Bit Generation Logic

This block generates the appropriate check bits for the 16 bits of data in the Data Input Latch. The check bits are generated according to a modified Hamming code.

### Syndrome Generation Logic

In both Error Detection and Error Correction modes, this logic block compares the check bits read from memory against a newly generated set of check bits produced for the data read in from memory. If both sets of check bits match, then there are no errors. If there is a mismatch, then one or more of the data or check bits is in error.

The syndrome bits are produced by an exclusive-OR of the two sets of check bits. If the two sets of check bits are identical (meaning there are no errors) the syndrome bits will be all zeroes. If there are errors, the syndrome bits can be decoded to determine the number of errors and the bit-in-error.

### Error Detection Logic

This section decodes the syndrome bits generated by the Syndrome Generation Logic. If there are no errors in either the input data or check bits, the $\overline{\text{ERROR}}$ and $\overline{\text{MULTI ERROR}}$ outputs remain HIGH. If one or more errors are detected, $\overline{\text{ERROR}}$ goes LOW. If two or more errors are detected, both $\overline{\text{ERROR}}$ and $\overline{\text{MULTI ERROR}}$ go LOW.

### Error Correction Logic

For single errors, the Error Correction Logic complements (corrects) the single data bit in error. This corrected data is loadable into the Data Output Latch, which can then be read onto the bidirectional data lines. If the single error is one of the check bits, the correction logic does not place corrected check bits on the syndrome/check bit outputs. If the corrected check bits are needed the EDC must be switched to Generate Mode.

### Data Output Latch

The Data Output Latch is used for storing the result of an error correction operation. The latch is loaded from the correction logic under control of the Data Output Latch Enable, LE OUT. The Data Output Latch may also be loaded directly from the Data Input Latch under control of the PASS THRU control input.

The Data Output Latch is split into two 8-bit (byte) latches which may be enabled independently for reading onto the bidirectional data lines.

### Diagnostic Latch

This is a 16-bit latch loadable from the bidirectional data lines under control of the Diagnostic Latch Enable, LE DIAG. The Diagnostic Latch contains check bit information in one byte and control information in the other byte. The Diagnostic Latch is used for driving the device when in Internal Control Mode, or for supplying check bits when in one of the Diagnostic Modes.

### Control Logic

The control logic determines the specific mode the device operates in. Normally the control logic is driven by external control inputs. However, in Internal Control Mode, the control signals are instead read from the Diagnostic Latch.

## PIN DEFINITIONS

**$DATA_{0-15}$** 16 bidirectional data lines. They provide input to the Data Input Latch and Diagnostic Latch, and receive output from the Data Output Latch. $DATA_0$ is the least significant bit; $DATA_{15}$ the most significant.

**$CB_{0-6}$** Seven Check Bit input lines. The check bit lines are used to input check bits for error detection. Also used to input syndrome bits for error correction in 32 and 64-bit configurations.

**LE IN** Latch Enable – Data Input Latch. Controls latching of the input data. When HIGH the Data Input Latch and Check Bit Input Latch follow the input data and input check bits. When LOW, the Data Input Latch and Check Bit Input Latch are latched to their previous state.

**$\overline{\text{GENERATE}}$** Generate Check Bits input. When this input is LOW the EDC is in the Check Bit Generate Mode. When HIGH the EDC is in the Detect Mode or Correct Mode.

In the Generate Mode the circuit generates the check bits or partial check bits specific to the data in the Data Input Latch. The generated check bits are placed on the SC outputs.

In the Detect or Correct Modes the EDC detects single and multiple errors, and generates syndrome bits based upon the contents of the Data Input Latch and Check Bit Input Latch. In Correct Mode, single-bit errors are also automatically corrected – corrected data is placed at the inputs of the Data Output Latch. The syndrome result is placed on the SC outputs and indicates in a coded form the number of errors and the bit-in-error.

**$SC_{0-6}$** Syndrome/Check Bit outputs. These seven lines hold the check/partial-check bits when the EDC is in Generate Mode, and will hold the syndrome/partial syndrome bits when the device is in Detect or Correct Modes. These are 3-state outputs.

**$\overline{\text{OE SC}}$** Output Enable – Syndrome/Check Bits. When LOW, the 3-state output lines $SC_{0-6}$ are enabled. When HIGH, the SC outputs are in the high impedance state.

**$\overline{\text{ERROR}}$** Error Detected output. When the EDC is in Detect or Correct Mode, this output will go LOW if one or more syndrome bits are asserted, meaning there are one or more bit errors in the data or check bits. If no syndrome bits are asserted, there are no errors detected and the output will be HIGH. In Generate Mode, $\overline{\text{ERROR}}$ is forced HIGH. (In a 64-bit configuration, $\overline{\text{ERROR}}$ must be externally implemented.)

**$\overline{\text{MULTI ERROR}}$** Multiple Errors Detected output. When the EDC is in Detect or Correct Mode, this output if LOW indicates that there are two or more bit errors that have been detected. If HIGH this indicates that either one or no errors have been detected. In Generate Mode, $\overline{\text{MULTI ERROR}}$ is forced HIGH. (In a 64-bit configuration, $\overline{\text{MULTI ERROR}}$ must be externally implemented.)

**CORRECT** Correct input. When HIGH this signal allows the correction network to correct any single-bit error in the Data Input Latch (by complementing the bit-in-error) before putting it onto the Data Output Latch. When LOW the EDC will drive data directly from the Data Input Latch to the Data Output Latch without correction.

**LE OUT** Latch Enable – Data Output Latch. Controls the latching of the Data Output Latch. When LOW the Data Output Latch is latched to its previous state. When HIGH the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network. In Correct Mode, single-bit errors are corrected by the network before loading into the Data Output Latch. In Detect Mode, the contents of the Data Input Latch are passed through the correction network unchanged into the Data Output Latch. The inputs to the Data Output Latch are unspecified if the EDC is in Generate Mode.

**$\overline{\text{OE}}$ BYTE 0, $\overline{\text{OE}}$ BYTE 1** Output Enable – Bytes 0 and 1, Data Output Latch. These lines control the 3-state outputs for each of the two bytes of the Data Output Latch. When LOW these lines enable the Data Output Latch and when HIGH these lines force the Data Output Latch into the high impedance state. The two enable lines can be separately activated to enable only one byte of the Data Output Latch at a time.

**PASS THRU** Pass Thru input. This line when HIGH forces the contents of the Check Bit Input Latch onto the Syndrome/Check Bit outputs ($SC_{0-6}$) and the unmodified contents of the Data Input Latch onto the inputs of the Data Output Latch.

**DIAG $MODE_{0-1}$** Diagnostic Mode Select. These two lines control the initialization and diagnostic operation of the EDC.

**CODE $ID_{0-2}$** Code Identification inputs. These three bits identify the size of the total data word to be processed and which 16-bit slice of larger data words a particular EDC is processing. The three allowable data word sizes are 16, 32 and 64 bits and their respective modified Hamming codes are designated 16/22, 32/39 and 64/72. Special CODE ID input 001 ($ID_2$, $ID_1$, $ID_0$) is also used to instruct the EDC that the signals CODE $ID_{0-2}$, DIAG $MODE_{0-1}$, CORRECT and PASS THRU are to be taken from the Diagnostic Latch, rather than from the input control lines.

**LE DIAG** Latch Enable – Diagnostic Latch. When HIGH the Diagnostic Latch follows the 16-bit data on the input lines. When LOW the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits, and internal control signals for CODE $ID_{0-2}$, DIAG $MODE_{0-1}$, CORRECT and PASS THRU.

## FUNCTIONAL DESCRIPTION

The EDC contains the logic necessary to generate check bits on a 16-bit data field according to a modified Hamming code. Operating on data read from memory, the EDC will correct any single-bit error, and will detect all double and some triple-bit errors. It may be configured to operate on 16-bit data words (with 6 check bits), 32-bit data words (with 7 check bits) and 64-bit data words (with 8 check bits). In all configurations, the device makes the error syndrome bits available on separate outputs for error data logging.

### Code and Byte Specification

The EDC may be configured in several different ways and operates differently in each configuration. It is necessary to indicate to the device what size data word is involved and which bytes of the data word it is processing. This is done with input lines CODE $ID_{0-2}$, as shown in Table I. The three modified Hamming codes referred to in Table I are:

- 16/22 code – 16 data bits
  – 6 check bits
  – 22 bits in total.
- 32/39 code – 32 data bits
  – 7 check bits
  – 39 bits in total.
- 64/72 code – 64 data bits
  – 8 check bits
  – 72 bits in total.

CODE ID input 001 ($ID_2$, $ID_1$, $ID_0$) is a special code used to operate the device in Internal Control Mode (described later in this section).

**TABLE I. HAMMING CODE AND SLICE IDENTIFICATION.**

| CODE $ID_2$ | CODE $ID_1$ | CODE $ID_0$ | Hamming Code and Slice Selected |
|---|---|---|---|
| 0 | 0 | 0 | Code 16/22 |
| 0 | 0 | 1 | Internal Control Mode |
| 0 | 1 | 0 | Code 32/39, Bytes 0 and 1 |
| 0 | 1 | 1 | Code 32/39, Bytes 2 and 3 |
| 1 | 0 | 0 | Code 64/72, Bytes 0 and 1 |
| 1 | 0 | 1 | Code 64/72, Bytes 2 and 3 |
| 1 | 1 | 0 | Code 64/72, Bytes 4 and 5 |
| 1 | 1 | 1 | Code 64/72, Bytes 6 and 7 |

### Control Mode Selection

The device control lines are $\overline{\text{GENERATE}}$, CORRECT, PASS THRU, DIAG $MODE_{0-1}$ and CODE $ID_{0-2}$. Table II indicates the control modes selected by various combinations of the control line inputs.

### Diagnostics

Table III shows specifically how DIAG $MODE_{0-1}$ select between normal operation, initialization and one of two diagnostic modes.

The Diagnostic Modes allow the user to operate the EDC under software control in order to verify proper functioning of the device.

### Check and Syndrome Bit Labeling

The check bits generated in the EDC are designated as follows:

- 16-bit configuration – CX C0, C1, C2, C4, C8;
- 32-bit configuration – CX, C0, C1, C2, C4, C8, C16;
- 64-bit configuration – CX, C0, C1, C2, C4, C8, C16, C32.

Syndrome bits are similarly labeled SX through S32. There are only 6 syndrome bits in the 16-bit configuration, 7 for 32 bits and 8 syndrome bits in the 64-bit configuration.

## FUNCTIONAL DESCRIPTION – 16-BIT DATA WORD CONFIGURATION

The 16-bit format consists of 16 data bits, 6 check bits and is referred to as 16/22 code (see Figure 1).

The 16-bit configuration is shown in Figure 2.

### Generate Mode

In this mode check bits will be generated that correspond to the contents of the Data Input Latch. The check bits generated are placed on the outputs $SC_{0-5}$ ($SC_6$ is unspecified for 16-bit operation).

Check bits are generated according to a modified Hamming code. Details of the code for check bit generation are contained in Table IV. Each check bit is generated as either an XOR or XNOR of eight of the 16 data bits as indicated in the table. The XOR function results in an even parity check bit, the XNOR is an odd parity check bit.

### Detect Mode

In this mode the device examines the contents of the Data Input Latch against the Check Bit Input Latch, and will detect all single-bit errors, all double-bit errors and some triple-bit errors. If one or more errors are detected, $\overline{\text{ERROR}}$ goes LOW. If two or more errors are detected, $\overline{\text{MULTI ERROR}}$ goes LOW. Both error indicators are HIGH if there are no errors.

Also available on device outputs $SC_{0-5}$ are the syndrome bits generated by the error detection step. The syndrome bits may be decoded to determine if a bit error was detected and, for single-bit errors, which of the data or check bits is in error. Table V gives the chart for decoding the syndrome bits generated by the 16-bit configuration (as an example, if the syndrome bits SX/S0/S1/S2/S4/S8 were 101001 this would be decoded to indicate that there is a single-bit error at data bit 9). If no error is detected the syndrome bits will all be zeroes.

In Detect Mode, the contents of the Data Input Latch are driven directly to the inputs of the Data Output Latch without correction.

### Correct Mode

In this mode, the EDC functions the same as in Detect Mode except that the correction network is allowed to correct (complement) any single-bit error of the Data Input Latch before putting it onto the inputs of the Data Output Latch. If multiple errors are detected, the output of the correction network is unspecified. If the single-bit error is a check bit there is no automatic correction. If check bit correction is desired, this can be done by placing the device in Generate Mode to produce a correct check bit sequence for the data in the Data Input Latch.

### Pass Thru Mode

In this mode, the unmodified contents of the Data Input Latch are placed on the inputs of the Data Output Latch and the contents of the Check Bit Input Latch are placed on outputs $SC_{0-5}$.

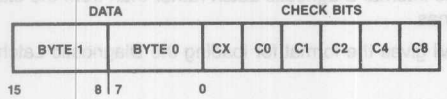
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**TABLE II. EDC CONTROL MODE SELECTION.**

| $\overline{\text{GENERATE}}$ | CORRECT | PASS THRU | DIAG MODE$_{0\text{-}1}$ ($DM_1$, $DM_0$) | CODE ID$_{0\text{-}2}$ ($ID_2$, $ID_1$, $ID_0$) | Control Mode Selected |
|---|---|---|---|---|---|
| LOW | LOW | LOW | 00 | Not 001 | Generate |
| LOW | LOW | LOW | 01 | Not 001 | Generate Using Diagnostic Latch |
| LOW | LOW | LOW | 10 | Not 001 | Generate |
| LOW | LOW | LOW | 11 | Not 001 | Initialize |
| LOW | LOW | HIGH | 00 | Not 001 | Pass Thru |
| LOW | LOW | HIGH | 01 | Not 001 | Pass Thru |
| LOW | LOW | HIGH | 10 | Not 001 | Pass Thru |
| LOW | LOW | HIGH | 11 | Not 001 | Undefined |
| LOW | HIGH | LOW | 00 | Not 001 | Generate |
| LOW | HIGH | LOW | 01 | Not 001 | Generate Using Diagnostic Latch |
| LOW | HIGH | LOW | 10 | Not 001 | Generate |
| LOW | HIGH | LOW | 11 | Not 001 | Initialize |
| LOW | HIGH | HIGH | 00 | Not 001 | Pass Thru |
| LOW | HIGH | HIGH | 01 | Not 001 | Pass Thru |
| LOW | HIGH | HIGH | 10 | Not 001 | Pass Thru |
| LOW | HIGH | HIGH | 11 | Not 001 | Undefined |
| HIGH | LOW | LOW | 00 | Not 001 | Detect |
| HIGH | LOW | LOW | 01 | Not 001 | Detect |
| HIGH | LOW | LOW | 10 | Not 001 | Detect Using Diagnostic Latch |
| HIGH | LOW | LOW | 11 | Not 001 | Initialize |
| HIGH | LOW | HIGH | 00 | Not 001 | Pass Thru |
| HIGH | LOW | HIGH | 01 | Not 001 | Pass Thru |
| HIGH | LOW | HIGH | 10 | Not 001 | Pass Thru |
| HIGH | LOW | HIGH | 11 | Not 001 | Undefined |
| HIGH | HIGH | LOW | 00 | Not 001 | Correct |
| HIGH | HIGH | LOW | 01 | Not 001 | Correct |
| HIGH | HIGH | LOW | 10 | Not 001 | Correct Using Diagnostic Latch |
| HIGH | HIGH | LOW | 11 | Not 001 | Initialize |
| HIGH | HIGH | HIGH | 00 | Not 001 | Pass Thru |
| HIGH | HIGH | HIGH | 01 | Not 001 | Pass Thru |
| HIGH | HIGH | HIGH | 10 | Not 001 | Pass Thru |
| HIGH | HIGH | HIGH | 11 | Not 001 | Undefined |
| Any | Any | Any | Any | 001 | Internal Control Using Diagnostic Latch |

**TABLE III. DIAGNOSTIC MODE CONTROL.**

| DIAG MODE$_1$ | DIAG MODE$_0$ | Diagnostic Mode Selected |
|---|---|---|
| 0 | 0 | **Non-diagnostic mode.** The EDC functions normally in all modes. |
| 0 | 1 | **Diagnostic Mode A.** The contents of the Diagnostic Latch are substituted for the normally generated check bits when in the Generate Mode. The EDC functions normally in the Detect or Correct modes. |
| 1 | 0 | **Diagnostic Mode B.** In the Detect or Correct Mode, the contents of the Diagnostic Latch are substituted for the check bits normally read from the Check Bit Input Latch. The EDC functions normally in the Generate Mode. |
| 1 | 1 | **Initialize.** The inputs of the Data Output Latch are forced to zeroes and the check bits generated correspond to the all-zero data. |




Uses Modified Hamming Code 16/22
- 16 data bits
- 6 check bits
- 22 bits in total

BLI-202

**Figure 1. 16 Bit Data Format.**

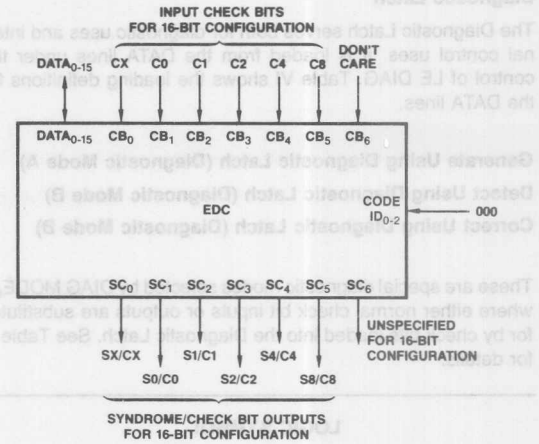



**Figure 2. 16 Bit Configuration.**

BLI-203

**TABLE IV. 16-BIT MODIFIED HAMMING CODE – CHECK BIT ENCODE CHART.**

| Generated Check Bits | Parity | Participating Data Bits | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| CX | Even (XOR) | | X | X | X | | X | | | X | X | | X | | | X | |
| C0 | Even (XOR) | X | X | X | | X | | X | | X | | X | | X | | | |
| C1 | Odd (XNOR) | X | | | X | X | | | X | | X | X | | | X | | X |
| C2 | Odd (XNOR) | X | X | | | | X | X | X | | | | X | X | X | | |
| C4 | Even (XOR) | | | X | X | X | X | X | X | | | | | | | X | X |
| C8 | Even (XOR) | | | | | | | | | X | X | X | X | X | X | X | X |

The check bit is generated as either an XOR or XNOR of the eight data bits noted by an "X" in the table.

**TABLE V. SYNDROME DECODE TO BIT-IN-ERROR.**

| Syndrome Bits | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | S8 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| | | | S4 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| | | | S2 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| SX | S0 | S1 | | | | | | | | | |
| 0 | 0 | 0 | | * | C8 | C4 | T | C2 | T | T | M |
| 0 | 0 | 1 | | C1 | T | T | 15 | T | 13 | 7 | T |
| 0 | 1 | 0 | | C0 | T | T | M | T | 12 | 6 | T |
| 0 | 1 | 1 | | T | 10 | 4 | T | 0 | T | T | M |
| 1 | 0 | 0 | | CX | T | T | 14 | T | 11 | 5 | T |
| 1 | 0 | 1 | | T | 9 | 3 | T | M | T | T | M |
| 1 | 1 | 0 | | T | 8 | 2 | T | 1 | T | T | M |
| 1 | 1 | 1 | | M | T | T | M | T | M | M | T |

* – no errors detected
Number – the location of the single bit-in-error
T – two errors detected
M – three or more errors detected

**TABLE VI. DIAGNOSTIC LATCH LOADING – 16-BIT FORMAT.**

| Data Bit | Internal Function |
|---|---|
| 0 | Diagnostic Check Bit X |
| 1 | Diagnostic Check Bit 0 |
| 2 | Diagnostic Check Bit 1 |
| 3 | Diagnostic Check Bit 2 |
| 4 | Diagnostic Check Bit 4 |
| 5 | Diagnostic Check Bit 8 |
| 6, 7 | Don't Care |
| 8 | CODE ID 0 |
| 9 | CODE ID 1 |
| 10 | CODE ID 2 |
| 11 | DIAG MODE 0 |
| 12 | DIAG MODE 1 |
| 13 | CORRECT |
| 14 | PASS THRU |
| 15 | Don't Care |

8

### Diagnostic Latch

The Diagnostic Latch serves both for diagnostic uses and internal control uses. It is loaded from the DATA lines under the control of LE DIAG. Table VI shows the loading definitions for the DATA lines.

**Generate Using Diagnostic Latch (Diagnostic Mode A)**

**Detect Using Diagnostic Latch (Diagnostic Mode B)**

**Correct Using Diagnostic Latch (Diagnostic Mode B)**

These are special diagnostic modes selected by DIAG $MODE_{0-1}$ where either normal check bit inputs or outputs are substituted for by check bits loaded into the Diagnostic Latch. See Table III for details.

### Internal Control Mode

This mode is selected by CODE $ID_{0-2}$ input 001 ($ID_2$, $ID_1$, $ID_0$).

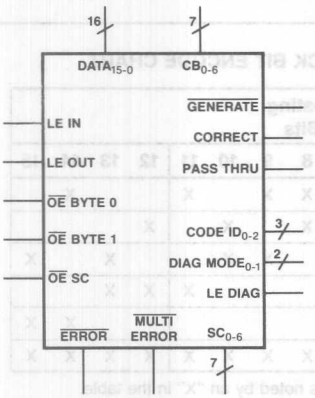
When in Internal Control Mode, the EDC takes the CODE $ID_{0-2}$, DIAG $MODE_{0-1}$, CORRECT and PASS THRU control signals from the internal Diagnostic Latch rather than from the external input lines.

Table VI gives the format for loading the Diagnostic Latch.

### 32 and 64-Bit Operation

The EDC can easily be cascaded to operate on 32 and 64-bit data words. Since this is unlikely to occur in a Z8000 system, it is not discussed in this data sheet. Interested users should refer to the Am2960 data sheet for more information.

### LOGIC SYMBOL




BLI-204

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

BLI-205

# AmZ8161 • AmZ8162

## 4-Bit Error Correction Multiple Bus Buffers

**IN DEVELOPMENT**

### DISTINCTIVE CHARACTERISTICS

- Quad high-speed LSI bus-transceiver
- Provides complete data path interface between the AmZ8160 Error Detection and Correction Unit, the system data bus and dynamic RAM memory
- 3-state 24mA output to data bus
- 3-state data output to memory
- Inverting data bus for AmZ8161 and non-inverting for AmZ8162
- Data bus latches allow operation with multiplexed buses
- Advanced Low-Power Schottky processing
- 100% product assurance screening to MIL-STD-883 requirements

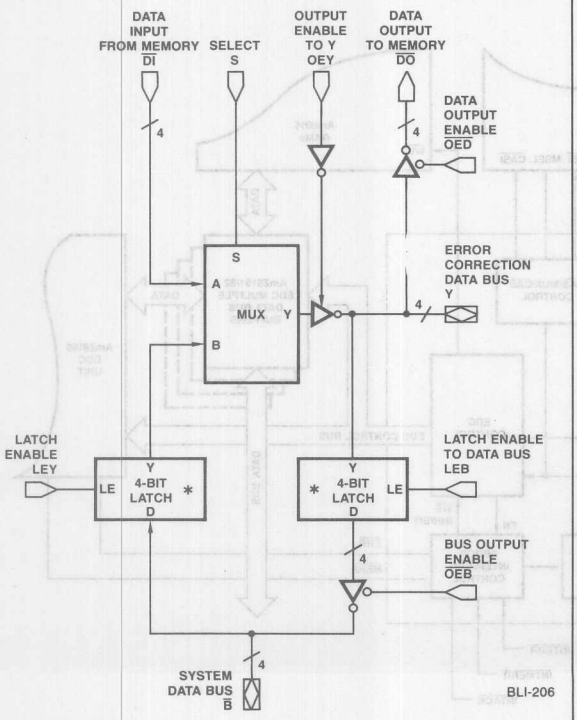
### FUNCTIONAL DESCRIPTION

The AmZ8161 and AmZ8162 are high-performance, low-power Schottky multiple bus buffers that provide the complete data path interface between the AmZ8160 Error Detection and Correction Unit, dynamic RAM memory and the AmZ8000 system data bus. The AmZ8161 provides an inverting data path between the data bus ($\overline{B_i}$) and the AmZ8160 error correction data input ($Y_i$) and the AmZ8162 provides a non-inverting configuration ($B_i$ to $Y_i$). Both devices provide inverting data paths between the AmZ8160 and memory data bus thereby optimizing internal data path speeds.

The AmZ8161 and AmZ8162 are 4-bit devices. Four devices are used to interface each 16-bit AmZ8160 Error Detection and Correction Unit with dynamic memory. The system can easily be expanded to 32 or more bits for wider memory applications. The 4-bit configuration allows enabling the appropriate devices two-at-a-time for intermixed word or byte, read and write in 16-bit systems with error correction.

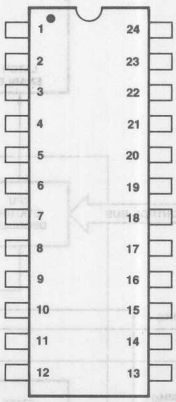
Data latches between the error correction data bus and the system data bus facilitate the addition of error corrected memory in synchronous data bus systems. They also provide a data holding capability during single-step system operation.

### AmZ8161 LOGIC DIAGRAM




*AmZ8162 is the same function but non-inverting between the Y bus to the system data bus, B. This is done by making both latches inverting.

### CONNECTION DIAGRAM
**Top View**




24 pin slim (0.3")

BLI-207

Note: Pin 1 is marked for orientation.

8

# AmZ8163

## Dynamic Memory Timing, Refresh and EDC Controller

### DISTINCTIVE CHARACTERISTICS

- Complete AmZ8000 CPU to dynamic RAM contol interface
- RAS/CAS Sequencer to eliminate delay lines
- Memory request/refresh arbitration
- Controls for Word/Byte read or write
- Complete EDC data path and mode controls
- Refresh interval timer independent of CPU
- Refresh control during Single Step or Halt modes
- EDC error flag latches for error logging under software control
- Also, complete control for 8-Bit MOS $\mu$P

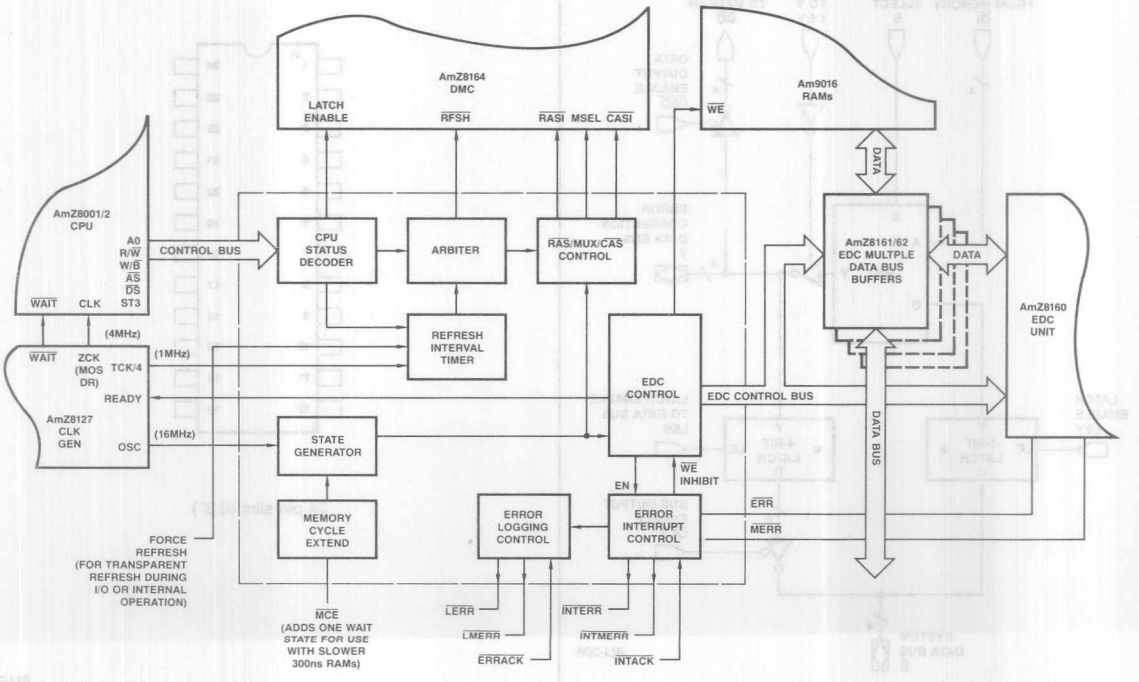
### FUNCTIONAL DESCRIPTION

The AmZ8163 is a high speed bus interface controller forming an integral part of the AmZ8000 memory support chip set using dynamic MOS RAMs with Error Detection and Correction (EDC). The complete chip set includes the AmZ8127 Clock Generator and Controller, the AmZ8164 Dynamic Memory Controller, the AmZ8161/2 EDC Bus Buffers, the AmZ8160 EDC Unit and optional AmZ8165/6 RAM Drivers.

The AmZ8163 provides all of the control interface functions including RAS/Address MUX/CAS timing (without delay lines), refresh timing, memory request/refresh arbitration and all EDC enables and controls. The enable controls are configured for both word and byte operations including the data controls for byte write with error correction. The AmZ8163 generates bus and operating mode controls for the AmZ8160 EDC Unit.

The AmZ8163 uses the AmZ8127 16MHz (4 x CLK) output to generate RAS/Address MUX/CAS timing. An internal refresh interval timer generates the memory refresh request independent of the CPU to guarantee the proper refresh timing under all combinations of CPU and DMA memory requests.

### FUNCTION DIAGRAM
### REFRESH AND EDC CONTROLLER




BLI-167

# AmZ8164

## Dynamic Memory Controller

### ADVANCED INFORMATION

#### DISTINCTIVE CHARACTERISTICS

- Dynamic Memory Controller for 16K and 64K MOS dynamic RAMs
- 8-Bit Refresh Counter for refresh address generation, has clear input and terminal count output
- Refresh Counter Terminal count selectable at 256 or 128
- Latch Input RAS Decoder provides 4 RAS outputs, all active during refresh
- Dual 8-Bit Address Latches plus separate $\overline{RAS}$ Decoder Latches
- Grouping functions on a common chip minimizes speed differential/skew between address, $\overline{RAS}$ and $\overline{CAS}$ outputs
- 3-Port 8-Bit Address Multiplexer with Schottky speed
- Burst mode, distributed refresh or transparent refresh mode determined by user
- Non-inverting address, $\overline{RAS}$ and $\overline{CAS}$ paths
- 100% product assurance screening to MIL-STD-883 requirements

#### FUNCTIONAL DESCRIPTION

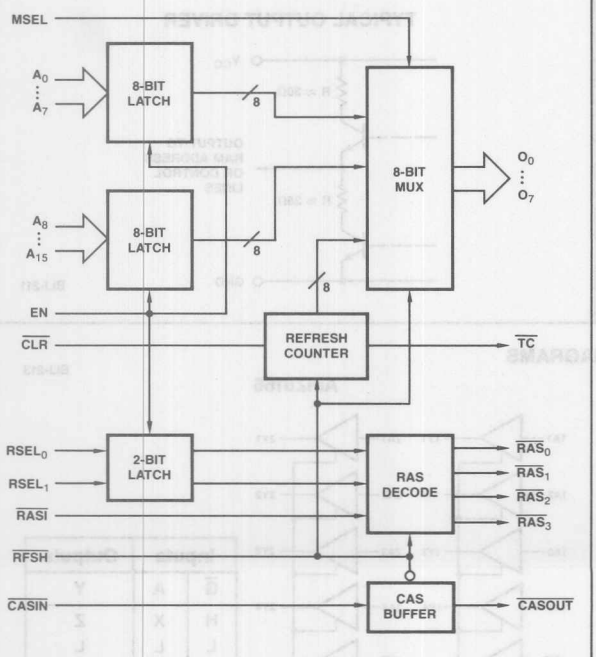
The AmZ8164 Dynamic Memory Controller replaces several MSI devices by grouping several unique functions. Two 8-bit latches capture and hold the memory address from the AmZ8000 multiplexed data and address bus. These latches and a clearable, 8-bit refresh counter feed into an 8-bit, 3-input, Schottky speed MUX, for output to the dynamic RAM address lines. The device is also compatible with Am8085 or any CPU interfacing with dynamic RAMs.

The same silicon chip also includes a special RAS decoder and CAS buffer. Placing these functions on the same chip minimizes the time skew between output functions which would otherwise be separate MSI chips, and therefore, allows a faster memory cycle time by the amount of skew eliminated.

Pulsing the active LOW refresh line, $\overline{RFSH}$, switches the MUX to the counter output, inhibits $\overline{CAS}$, and forces all four $\overline{RAS}$ decoder outputs active simultaneously. The counter is advanced at the end of the refresh cycle – the LOW-to-HIGH transition of $\overline{RFSH}$. Various refresh modes can be accommodated – for 16K or 64K RAMs and for a wide variety of processor configurations.

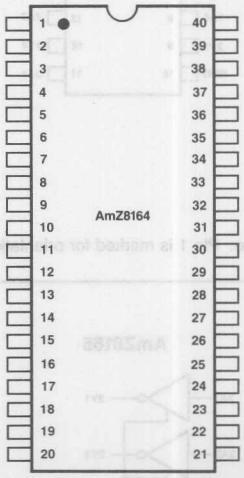
$A_{15}$ is a dual function input which controls the refresh counter's range. For 64K RAMs it is an address input. For 16K RAMs it can be pulled to +12V through 1KΩ to terminate the refresh count at 128 instead of 256 if this is needed.

#### LOGIC DIAGRAM




BLI-208

#### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

BLI-209

8

## DISTINCTIVE CHARACTERISTICS

- **Controlled rise and fall characteristics**
  Internal resistors provide symmetrical drive to HIGH and LOW states, eliminating need for external series resistor.
- **Output swings designed to drive 16K and 64K RAMs**
  $V_{OH}$ guaranteed at $V_{CC} - 1.15V$. Undershoot going LOW guaranteed at less than 0.5V.
- **Large capacitive drive capability**
  35mA min source or sink current at 2.0V. Propagation delays specified for 50pF and 500pF loads.
- **Pin-compatible with 'S240 and 'S244**
  Non-inverting AmZ8166 replaces 74S244; inverting AmZ8165 replaces 74S240. Faster than 'S240/244 under equivalent load.
- **No-glitch outputs**
  Outputs forced into OFF state during power up and down.

## CONNECTION DIAGRAM
### Top View




Note: Pin 1 is marked for orientation.

BLI-210

## FUNCTIONAL DESCRIPTION

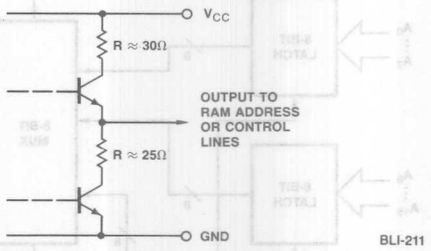
The AmZ8165 and AmZ8166 are designed and specified to drive the capacitive input characteristics of the address and control lines of MOS dynamic RAMs. The unique design of the lower output driver includes a collector resistor to control undershoot on the HIGH-to-LOW transition. The upper output driver pulls up to $V_{CC} - 1.15V$ to be compatible with MOS memory and is designed to have a rise time symmetrical with the lower output's controlled fall time. This allows optimization of Dynamic RAM performance.

The AmZ8165 and AmZ8166 are pin-compatible with the popular 'S240 and 'S244 with identical 3-state output enable controls. The AmZ8165 has inverting drivers and the AmZ8166 has non-inverting drivers.

The inclusion of an internal resistor in the lower output driver eliminates the requirement for an external series resistor, therefore reducing package count and the board area required. The internal resistor controls the output fall and undershoot without slowing the output rise.

These devices are designed for use with the AmZ8164 Dynamic Memory Controller where large dynamic memories with highly capacitive input lines require additional buffering. Driving eight address lines or four $\overline{RAS}$ and four $\overline{CAS}$ lines with drivers on the same silicon chip also provides a significant performance advantage by minimizing skew between drivers. Each device has specified skew between drivers to improve the memory access worst case timing over the min and max $t_{PD}$ difference of unspecified devices.

## TYPICAL OUTPUT DRIVER

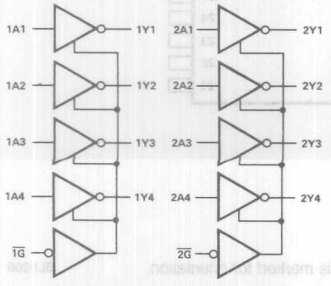



BLI-211

## LOGIC DIAGRAMS

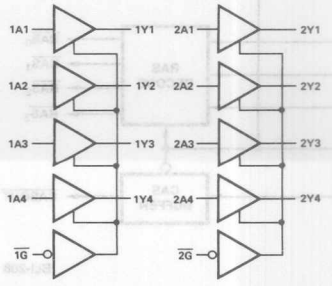
BLI-212

### AmZ8165




| Inputs | | Outputs |
|---|---|---|
| $\overline{G}$ | A | Y |
| H | X | Z |
| L | H | L |
| L | L | H |

### AmZ8166




| Inputs | | Outputs |
|---|---|---|
| $\overline{G}$ | A | Y |
| H | X | Z |
| L | L | L |
| L | H | H |

BLI-213

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65 to +150°C |
| Temperature (Ambient) Under Bias | −55 to +125°C |
| Supply Voltage to Ground Potential Continuous | −0.5 to +7.0V |
| DC Voltage Applied to Outputs for High Output State | −0.5V to +$V_{CC}$ max |
| DC Input Voltage | −0.5 to +7.0V |
| DC Output Current, into Outputs | 30mA |
| DC Input Current | −30 to +5.0mA |

## ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A$ = 0 to 70°C $V_{CC}$ = 5.0V ±10% (MIN = 4.50V MAX = 5.50V)
MIL $T_A$ = −55 to +125°C $V_{CC}$ = 5.0V ±10% (MIN = 4.50V MAX = 5.50V)

## DC CHARACTERISTICS OVER OPERATING RANGE

| Parameters | Description | | Test Conditions (Note 1) | | Min | Typ (Note 2) | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage | | $V_{CC}$ = MIN, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −1mA | $V_{CC}$−1.15 | $V_{CC}$−0.7V | | Volts |
| $V_{OL}$ | Output LOW Voltage | | $V_{CC}$ = MIN, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 1mA | | | 0.5 | Volts |
| | | | | $I_{OL}$ = 12mA | | | 0.8 | |
| $V_{IH}$ | Input HIGH Level | | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | | Guaranteed input logical LOW voltage for all inputs | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{IL}$ | Input LOW Current | | $V_{CC}$ = MAX, $V_{IN}$ = 0.4V | | | | −200 | μA |
| $I_{IH}$ | Input HIGH Current | | $V_{CC}$ = MAX, $V_{IN}$ = 2.7V | | | | 20 | μA |
| $I_I$ | Input HIGH Current | | $V_{CC}$ = MAX, $V_{IN}$ = 7.0V | | | | 0.1 | mA |
| $I_{OZH}$ | Off-State Current | | $V_O$ = 2.7V | | | | 100 | μA |
| $I_{OZL}$ | Off-State Current | | $V_O$ = 0.4V | | | | −200 | μA |
| $I_{OL}$ | Output Sink Current | | $V_{OL}$ = 2.0V | | 35 | | | mA |
| $I_{OH}$ | Output Source Current | | $V_{OH}$ = 2.0V | | −35 | | | mA |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | | $V_{CC}$ = MAX | | −60 (see $I_{OH}$) | | −200 | mA |
| $I_{CC}$ | Supply Current | AmZ8165 | All Outputs HIGH | $V_{CC}$ = MAX Outputs Open | | 24 | 50 | mA |
| | | | All Outputs LOW | | | 86 | 125 | |
| | | | All Outputs Hi-Z | | | 86 | 125 | |
| | | AmZ8166 | All Outputs HIGH | $V_{CC}$ = MAX Outputs Open | | 53 | 75 | |
| | | | All Outputs LOW | | | 92 | 130 | |
| | | | All Outputs Hi-Z | | | 116 | 150 | |

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

8

## AmZ8165 • AmZ8166
## SWITCHING CHARACTERISTICS

($T_A$ = +25°C, VCC = 5.0V)

| Parameters | Description | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time from LOW-to-HIGH Output | Figure 1 Test Circuit Figure 3 Voltage Levels and Waveforms | $C_L$ = 0pF | | 6 | (Note 4) | ns |
| | | | $C_L$ = 50pF | 6 | 9 | 15 | |
| | | | $C_L$ = 500pF | 15 | 22 | 35 | |
| $t_{PHL}$ | Propagation Delay Time from HIGH-to-LOW Output | | $C_L$ = 0pF | | 4 | (Note 4) | ns |
| | | | $C_L$ = 50pF | 6 | 12 | 20 | |
| | | | $C_L$ = 500pF | 20 | 30 | 45 | |
| $t_{PLZ}$ | Output Disable Time from LOW, HIGH | Figures 2 and 4, S = 1 | | | 13 | 20 | ns |
| $t_{PHZ}$ | | Figures 2 and 4, S = 2 | | | 8 | 12 | |
| $t_{PZL}$ | Output Enable Time from LOW, HIGH | Figures 2 and 4, S = 1 | | | 13 | 20 | ns |
| $t_{PZH}$ | | Figures 2 and 4, S = 2 | | | 13 | 20 | |
| $t_{SKEW}$ | Output-to-Output Skew | Figures 1 and 3, $C_L$ = 50pF | | | ±0.5 | ±3.0 (Note 5) | ns |
| $V_{ONP}$ | Output Voltage Undershoot | Figures 1 and 3, $C_L$ = 50pF | | | 0 | −0.5 | Volts |

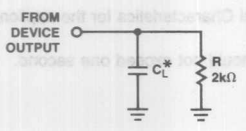
## SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Note 6)

| Parameters | Description | Test Conditions | | COM'L $T_A$ = 0 to 70°C $V_{CC}$ = 5.0V ±10% Min | COM'L Max | MIL $T_A$ = −55 to +125°C $V_{CC}$ = 5.0V ±10% Min | MIL Max | Units |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay Time LOW-to-HIGH Output | Figures 1 and 3 | $C_L$ = 50pF | 4 | 20 | 4 | 20 | ns |
| | | | $C_L$ = 500pF | 13 | 40 | 13 | 40 | |
| $t_{PHL}$ | Propagation Delay Time HIGH-to-LOW Output | Figures 1 and 3 | $C_L$ = 50pF | 4 | 24 | 4 | 24 | ns |
| | | | $C_L$ = 500pF | 17 | 50 | 17 | 50 | |
| $t_{PLZ}$ | Output Disable Time from LOW, HIGH | Figures 2 and 4 | S = 1 | | 24 | | 24 | ns |
| $t_{PHZ}$ | | | S = 2 | | 16 | | 16 | |
| $t_{PZL}$ | Output Enable Time from LOW, HIGH | Figures 2 and 4 | S = 1 | | 28 | | 28 | ns |
| $t_{PZH}$ | | | S = 2 | | 28 | | 28 | |
| $V_{ONP}$ | Output Voltage Undershoot | Figures 1 and 3, $C_L$ = 50pF | | | −0.5 | | −0.5 | Volts |

Notes: 4. Typical time shown for reference only – not tested.
5. Time Skew specification is guaranteed by design but not tested.
6. AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

### SWITCHING TEST CIRCUITS

BLI-214




*$t_{pd}$ specified at C = 50 and 500pF.

**Figure 1. Capacitive Load Switching.**

BLI-215

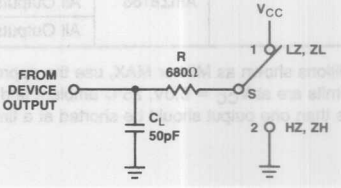



**Figure 2. Three-State Enable/Disable.**

## TYPICAL SWITCHING CHARACTERISTICS

### VOLTAGE WAVEFORMS

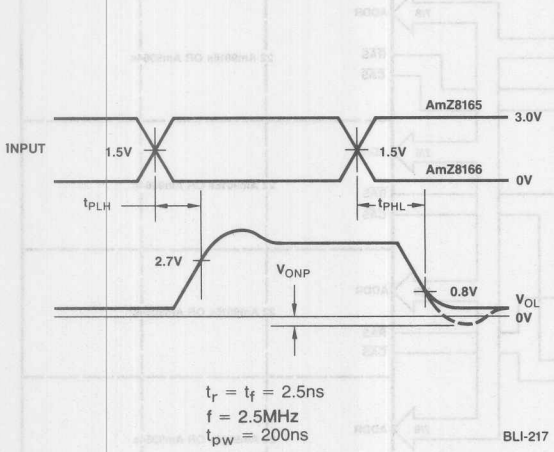



Figure 3. Output Drive Levels.

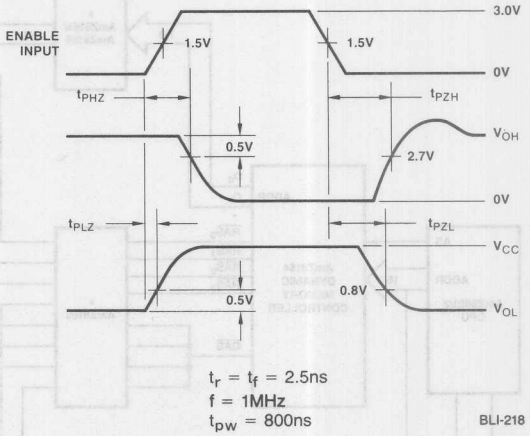



Figure 4. Three-State Control Levels.

The RAM Driver symmetrical output design offers significant improvement over a standard Schottky output by providing a balanced drive output impedance (≈33Ω both HIGH and LOW), and by pulling up to MOS $V_{OH}$ levels ($V_{CC}$ – 1.15V). External resistors, not required with the RAM Driver, protect standard Schottky drivers from error causing undershoot but also slow the output rise by adding to the internal R.

The RAM Driver is optimized to drive LOW at maximum speed based on safe undershoot control and to drive HIGH with a symmetrical speed characteristic. This is an optimum approach because the dominant RAM loading characteristic is input capacitance.

The curves shown below provide performance characteristics typical of both the inverting (AmZ8165) and non-inverting (AmZ8166) RAM Drivers.

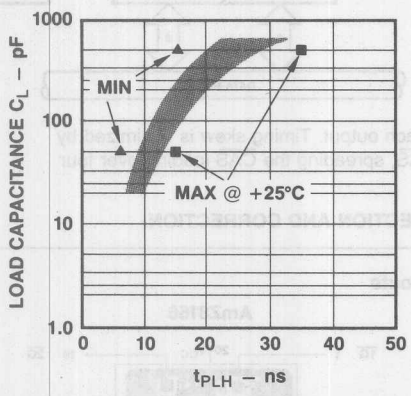



Figure 5. $t_{PLH}$ vs. $C_L$.

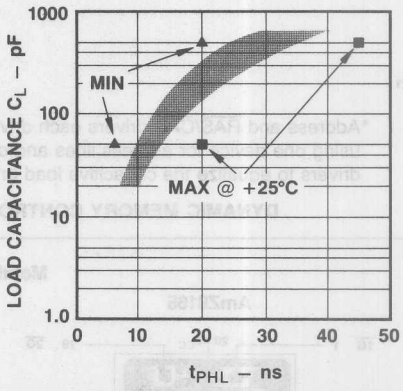
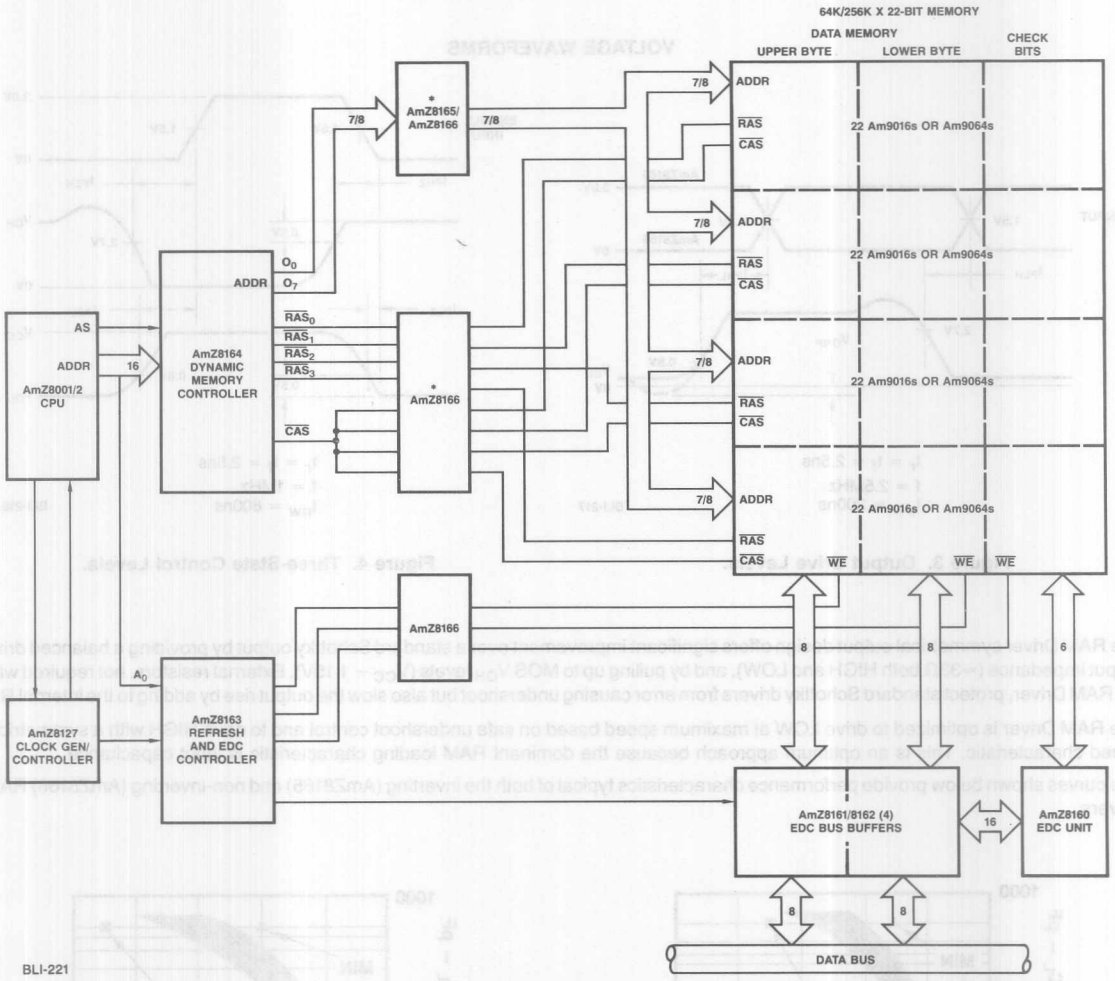



Figure 6. $t_{PHL}$ vs. $C_L$.

The curves above depict the typical $t_{PLH}$ and $t_{PHL}$ for the RAM Driver outputs as a function of load capacitance. The minimums and maximums are shown for worst case design. The typical band is provided as a guide for intermediate capacitive loads.

8

## APPLICATION

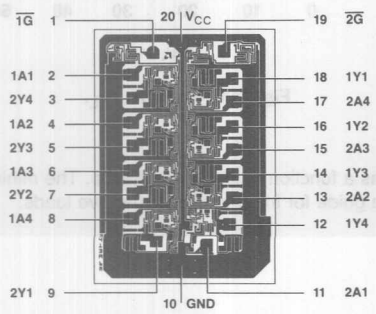



*Address and $\overline{RAS}/\overline{CAS}$ drivers each drive 22 RAM inputs at each output. Timing skew is minimized by using one device for address lines and one device for $\overline{RAS}/\overline{CAS}$, spreading the $\overline{CAS}$ loading over four drivers to equalize the capacitive load on each driver.

**DYNAMIC MEMORY CONTROL WITH ERROR DETECTION AND CORRECTION**

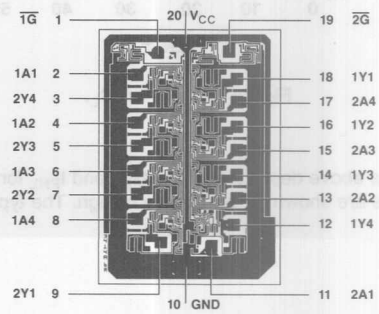
### Metallization and Pad Layouts

**AmZ8165**




DIE SIZE 0.094" X 0.060"

**AmZ8166**




DIE SIZE 0.094" X 0.060"

## ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

| AmZ8165 Order Number | AmZ8166 Order Number | Package Type | Temperature Range | Screening Level |
|---|---|---|---|---|
| AMZ8165PC | AMZ8166PC | P-20 | C | C-1 |
| AMZ8165DC | AmZ8166DC | D-20 | C | C-1 |
| AMZ8165DM | AMZ8166DM | D-20 | M | C-3 |
| AMZ8165XC | AMZ8166XC | Dice | C | Visual Inspection to MIL-STD-883 Method 2010B. |
| AMZ8165XM | AMZ8166XM | Dice | M | |

Notes: 1. P = Molded DIP, D = Hermetic DIP. Number following letter is number of leads.
2. C = 0 to 70°C, $V_{CC}$ = 4.50 to 5.50V, M = −55 to +125°C, $V_{CC}$ = 4.50 to 5.50V.
3. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

8

# Am3212·Am8212

## Eight-Bit Input/Output Port

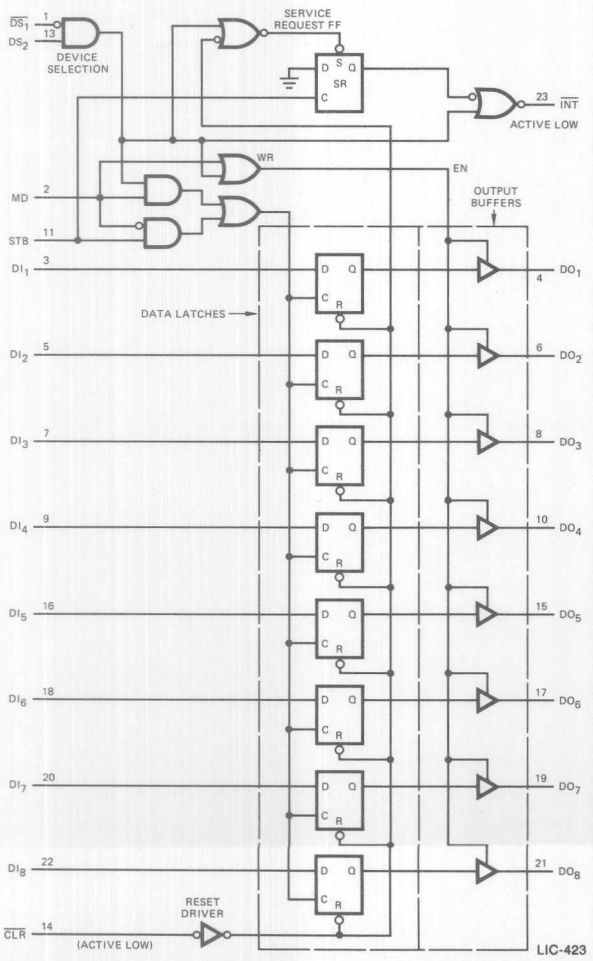
### Distinctive Characteristics

- Fully parallel, 8-bit data register and buffer replacing latches, multiplexers and buffers needed in microprocessor systems.
- 4.0V output high voltage for direct interface to MOS microprocessors, such as the Am9080A family.
- Input load current 250μA max.
- Reduces system package count
- Available for operation over both commercial and military temperature ranges.
- Advanced Schottky processing with 100% reliability assurance testing in compliance with MIL-STD-883.
- Service request flip-flop for interrupt generation
- Three-state outputs sink 15mA
- Asynchronous register clear with clock over-ride

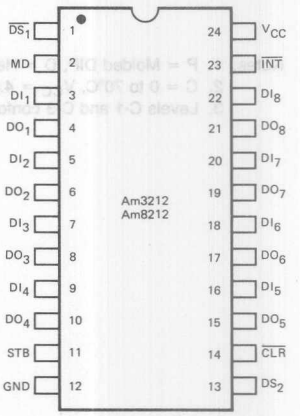
### FUNCTIONAL DESCRIPTION

All of the principal peripheral and input/output functions of a Microcomputer System can be implemented with the Am3212 • Am8212. The Am3212 • Am8212 input/output port consists of an 8-latch with 3-state output buffers along with control and device selection logic, which can be used to implement latches, gated buffers or multiplexers.

### LOGIC DIAGRAM




### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

LIC-424

### PIN DEFINITION

| | |
|---|---|
| $DI_1 - DI_8$ | DATA IN |
| $DO_1 - DO_8$ | DATA OUT |
| $\overline{DS_1} - DS_2$ | DEVICE SELECT |
| MD | MODE |
| STB | STROBE |
| $\overline{INT}$ | INTERRUPT (ACTIVE LOW) |
| $\overline{CLR}$ | CLEAR (ACTIVE LOW) |

### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Hermetic DIP | –55°C to +125°C | AM8212DM |
| Hermetic DIP | 0°C to +70°C | D8212 |
| Molded DIP | 0°C to +70°C | P8212 |
| Dice | 0°C to +70°C | AM8212XC |
| Hermetic DIP | 0°C to +70°C | D3212 |
| Hermetic DIP | –55°C to +125°C | MD3212 |
| Molded DIP | 0°C to +70°C | P3212 |

## FUNCTIONAL DESCRIPTION (Cont'd)

### Data Latch

The 8 flip-flops that make up the data latch are of a "D" type design. The output (Q) of the flip-flop will follow the data input (D) while the clock input (C) is high. Latching will occur when the clock (C) returns low.

The data latch is cleared by an asynchronous reset input ($\overline{CLR}$). (Note: Clock (C) Overrides Reset ($\overline{CLR}$)).

### Output Buffer

The outputs of the data latch (Q) are connected to 3-state, non-inverting output buffers. These buffers have a common control line (EN); this control line either enables the buffer to transmit the data from the outputs of the data latch (Q) or disables the buffer, forcing the output into a high impedance state. (3-state). This high-impedance state allows the Am3212 • Am8212 to be connected directly onto the microprocessor bi-directional data bus.

### Control Logic

The Am3212 • Am8212 has control inputs $\overline{DS_1}$, $DS_2$, MD And STB. These inputs are used to control device selection, data latching, output buffer state and service request flip-flop.

### $\overline{DS_1}$, $DS_2$ (Device Select)

These 2 inputs are used for device selection. When $\overline{DS_1}$ is low and $DS_2$ is high ($\overline{DS_1} \cdot DS_2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

### MD (Mode)

This input is used to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is high (output mode) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS_1} \cdot DS_2$).

When MD is low (input mode) the output buffer state is determined by the device selection logic ($\overline{DS_1} \cdot DS_2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

### STB (Strobe)

This input is used as the clock (C) to the data latch for the input mode MD = 0) and to synchronously reset the service request flip-flop (SR).

Note that the SR flip-flop is negative edge triggered.

### Service Request Flip-Flop

The SR flip-flop is used to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output of the (SR) flip-flop (Q) is connected to an inverting input of a "NOR" gate. The other input to the "NOR" gate is non-inverting and is connected to the device selection logic ($\overline{DS_1} \cdot DS_2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.

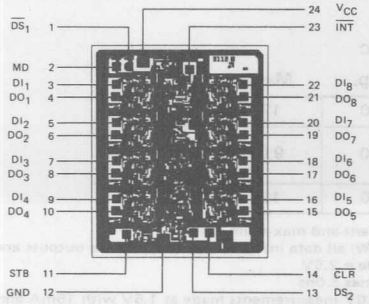
## TRUTH TABLE

| STB | MD | $\overline{DS_1} - DS_2$ | Data Out Equals |
|---|---|---|---|
| 0 | 0 | 0 | Three-State |
| 1 | 0 | 0 | Three-State |
| 0 | 1 | 0 | Data Latch |
| 1 | 1 | 0 | Data Latch |
| 0 | 0 | 1 | Data Latch |
| 1 | 0 | 1 | Data In |
| 0 | 1 | 1 | Data In |
| 1 | 1 | 1 | Data In |

| CLR | $\overline{DS_1} - DS_2$ | STB | SR* | $\overline{INT}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | ↓ | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | ↓ | 1 | 0 |
| | | | | |
| | | | | |

$\overline{CLR}$ — Resets Data Latch
— Sets SR Flip-Flop (no effect on Output Buffer)
* Internal SR Flip-Flop

### Metallization and Pad Layout




DIE SIZE
0.091" X 0.112"

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage | −0.5V to +7.0V |
| Output Voltage | −0.5V to +7.0V |
| Input Voltages | −1.0V to +5.5V |
| Output Current (Each Output) | 125mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

P8212, D8212, P3212, D3212 (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$
Am8212DM, MD3212 (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$

### DC CHARACTERISTICS

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $I_F$ | Input Load Current ACK, $DS_2$, CR, $DI_1 - DI_8$ Inputs | $V_F = 0.45V$ | | | | −0.25 | mA |
| $I_F$ | Input Load Current MD Input | $V_F = 0.45V$ | | | | −0.75 | mA |
| $I_F$ | Input Load Current $DS_1$ Input | $V_F = 0.45V$ | | | | −1.0 | mA |
| $I_R$ | Input Leakage Current ACK, DS, CR, $DI_1 - DI_8$ Inputs | $V_R = 5.25V$ | | | | 10 | μA |
| $I_R$ | Input Leakage Current MO Input | $V_R = 5.25V$ | | | | 30 | μA |
| $I_R$ | Input Leakage Current $DS_1$ Input | $V_R = 5.25V$ | | | | 40 | μA |
| $V_C$ | Input Forward Voltage Clamp | $I_C = -5.0mA$ | COM'L | | | −1.0 | Volts |
| | | | MIL | | | −1.2 | |
| $V_{IL}$ | Input LOW Voltage | | COM'L | | | 0.85 | Volts |
| | | | MIL | | | 0.80 | |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $I_{OL} = 15mA$ | | | | 0.45 | Volts |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -1.0mA$ | COM'L | 3.65 | 4.0 | | Volts |
| | | | MIL | 3.3 | 4.0 | | |
| | | $I_{OH} = -0.5mA$ | MIL | 3.4 | 4.0 | | |
| $I_{SC}$ | Short Circuit Output Current | $V_O = 0V$ | | −15 | | −75 | mA |
| $\|I_O\|$ | Output Leakage Current High Impedance | $V_O = 0.45V/5.25V$ | | | | 20 | μA |
| $I_{CC}$ | Power Supply Current | Note 2 | | | 90 | 130 | mA |

### AC CHARACTERISTICS (Note 3)

| Parameters | Description | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|
| $t_{pw}$ | Pulse Width | 30 | 8 | | ns |
| $t_{pd}$ | Data to Output Delay | | 12 | 30 | ns |
| $t_{we}$ | Write Enable to Output Delay | | 18 | 40 | ns |
| $t_{set}$ | Data Set-up Time | 15 | | | ns |
| $t_h$ | Data Hold Time | 20 | | | ns |
| $t_r$ | Reset to Output Delay | | 18 | 40 | ns |
| $t_s$ | Set to Output Delay | | 15 | 30 | ns |
| $t_e$ | Output Enable/Disable Time | | 14 | 45 | ns |
| $t_c$ | Clear to Output Delay | | 25 | 55 | ns |

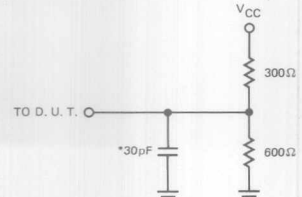
### CAPACITANCE (Note 4)

F = 1.0MHz, $V_{BIAS} = 2.5V$, $V_{CC} = +5.0V$, $T_A = 25°C$

| Parameters | Description | Typ. | Max. | Units |
|---|---|---|---|---|
| $C_{IN}$ | $DS_1$ MD Input Capacitance | 9.0 | 12 | pF |
| $C_{IN}$ | $DS_2$, CK, ACK, $DI_1 - DI_8$ Input Capacitance | 5.0 | 9.0 | pF |
| $C_{OUT}$ | $DO_1 - DO_8$ Output Capacitance | 8.0 | 12 | pF |

Notes: 1. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
2. CLR = STB = HIGH; $DS_1 = DS_2$ = MD = LOW; all data inputs are gound, all data outputs are open.
3. Conditions of Test: a) Input pulse amplitude = 2.5V
b) Input rise and fall times 5.0ns
c) Between 1.0V and 2.0V measurements made at 1.5V with 15mA and 30pF Test Load.
4. This parameter is sampled and not 100% tested.

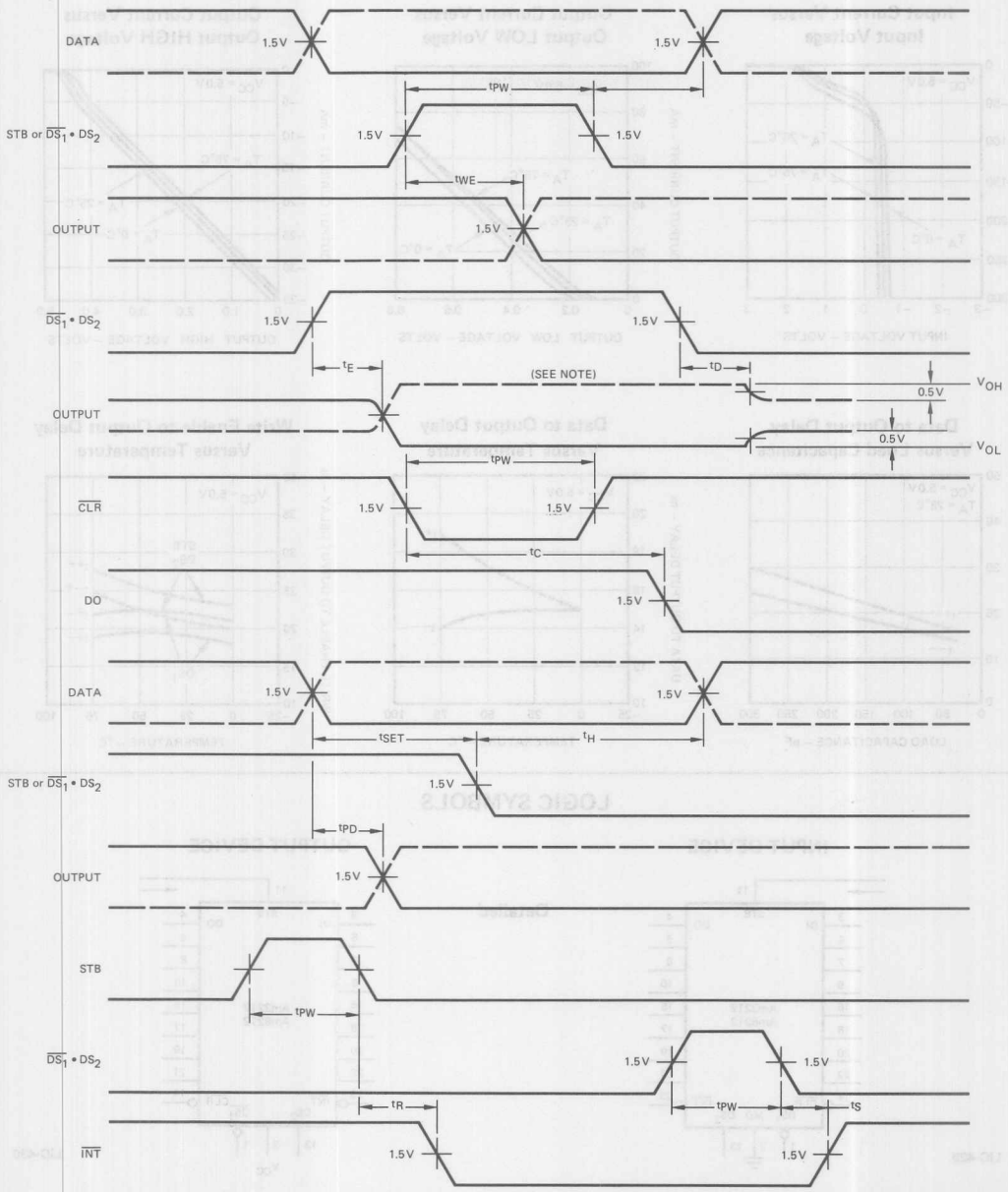
**TEST LOAD** (15mA and 30pF)




*Including Jig and Probe Capacitance.

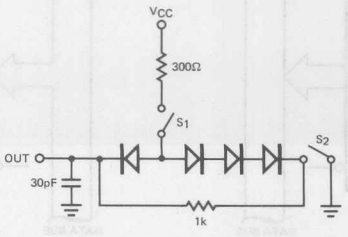
LIC-425

## TIMING DIAGRAM




LIC-426

Note: Alternative Test Load.

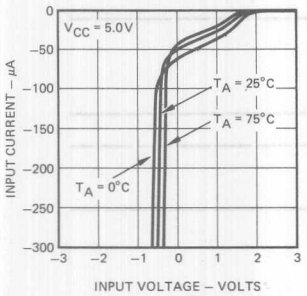



LIC-427

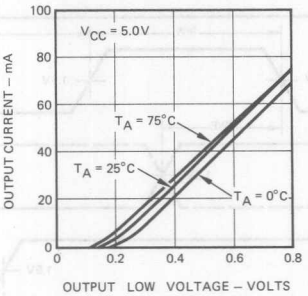
8

## TYPICAL CHARACTERISTICS

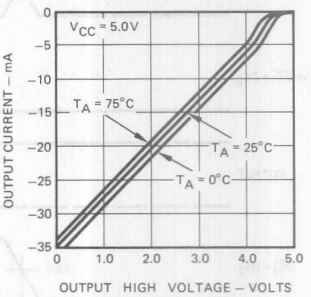
### Input Current Versus Input Voltage



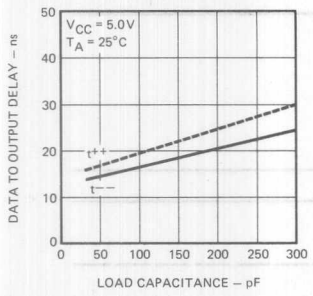

### Output Current Versus Output LOW Voltage



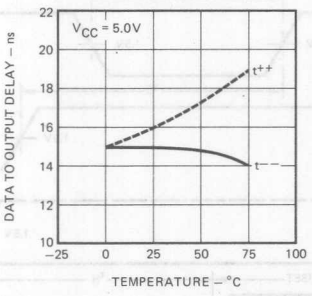

### Output Current Versus Output HIGH Voltage



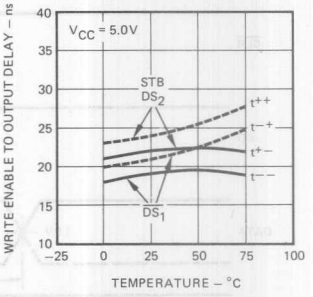

### Data to Output Delay Versus Load Capacitance




### Data to Output Delay Versus Temperature



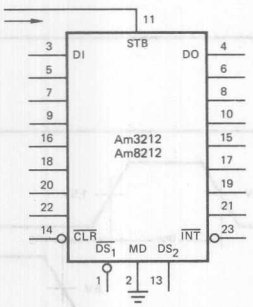

### Write Enable to Output Delay Versus Temperature




LIC-428

## LOGIC SYMBOLS

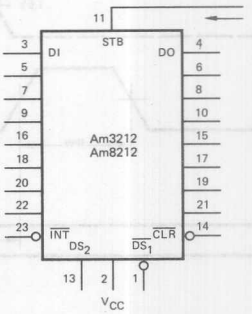
### INPUT DEVICE




LIC-429

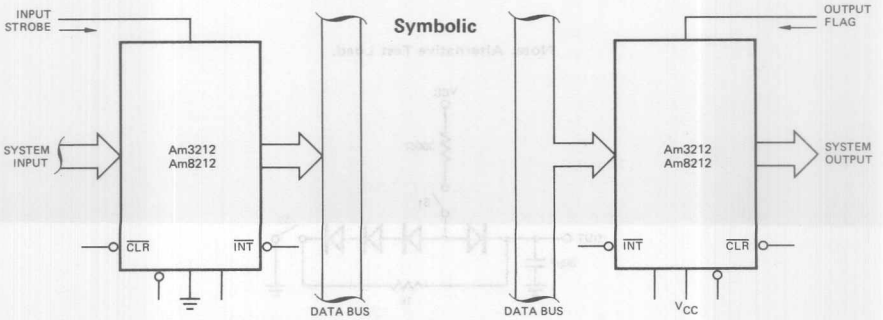
### Detailed

### OUTPUT DEVICE




LIC-430

### Symbolic




LIC-431

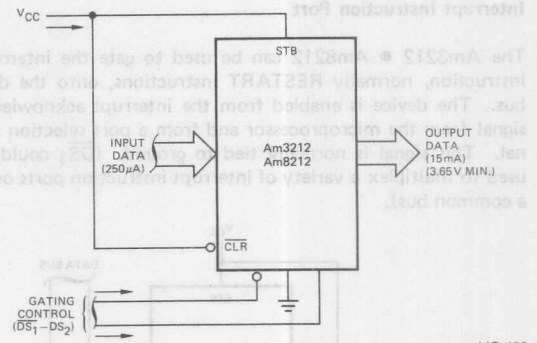
LIC-432

## TYPICAL APPLICATIONS OF THE Am8212

### GATED BUFFER (3-STATE)

By tying the mode signal low and the strobe input high, the data latch is acting as a straight through gate. The output buffers are then enabled from the device selection logic $\overline{DS_1}$ and $DS_2$.

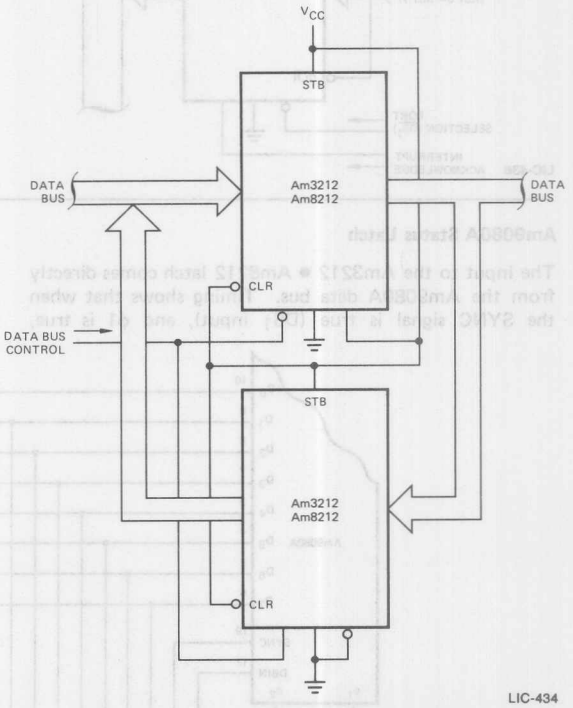
When the device selection logic is false, the outputs are 3-state. When the device selection logic is true, the input data from the system is directly transferred to the output.




LIC-433

### Bi-Directional Bus Driver

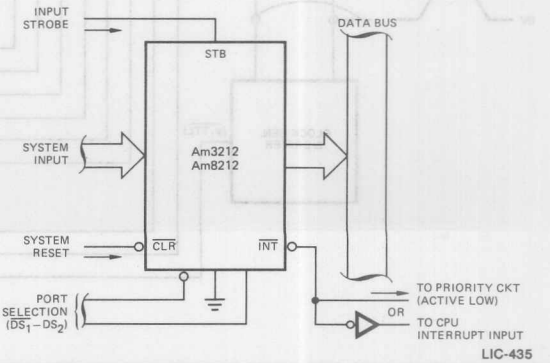
Two Am3212 • Am8212's wired back-to back can be used as a symmetrical drive, bi-directional bus driver. The devices are controlled by the data bus input control which is connected to $\overline{DS_1}$ on the first Am3212 • Am8212 and to $DS_2$ on the second. While one device is active, and acting as a straight through buffer the other is in its 3-state mode.




LIC-434

### Interrupting Input Port

The Am3212 • Am8212 accepts a strobe from the system input source, which in turn clears the service request flip-flop and interrupts the processor. The processor then goes through a service routine, identifies the port, and causes the device selection logic to go true – enabling the system input data onto the data bus.



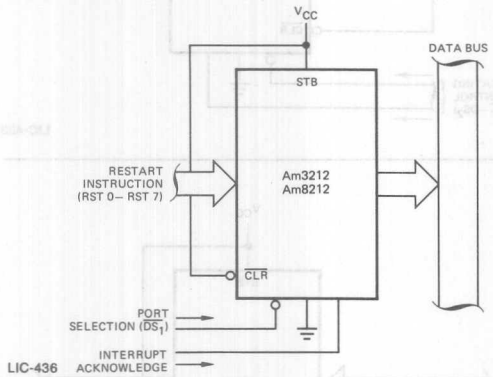

LIC-435

8

## TYPICAL APPLICATIONS OF THE Am8212 (Cont'd)

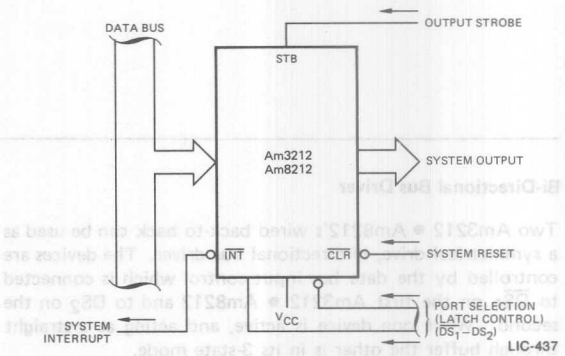
### Interrupt Instruction Port

The Am3212 • Am8212 can be used to gate the interrupt instruction, normally RESTART instructions, onto the data bus. The device is enabled from the interrupt acknowledge signal from the microprocessor and from a port selection signal. This signal is normally tied to ground. ($\overline{DS_1}$ could be used to multiplex a variety of interrupt instruction ports onto a common bus).



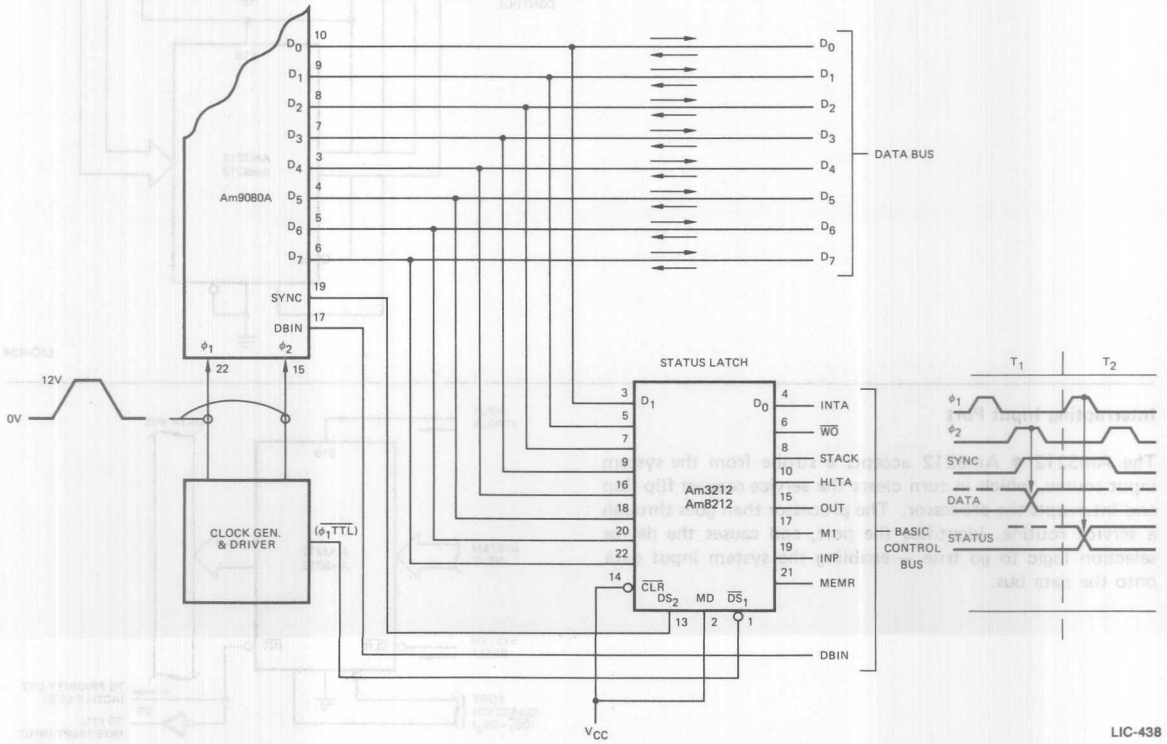

### Output Port (With Hand-Shaking)

The Am3212 • Am8212 is used to transmit data from the data bus to a system output. The output strobe could be a hand-shaking signal such as "reception of data" from the device that the system is outputting to. It in turn, can interrupt the system signifying the reception of date. The selection of the port comes from the device selection logic. ($\overline{DS_1} \cdot DS_2$).




### Am9080A Status Latch

The input to the Am3212 • Am8212 latch comes directly from the Am9080A data bus. Timing shows that when the SYNC signal is true ($\overline{DS_1}$ input), and $\phi 1$ is true, ($\overline{DS_1}$ input) then the status data will be latched into the Am3212 • Am8212. The mode signal is tied high so that the output on the latch is active and evabled all the time.



# Am3216 • Am3226 • Am8216 • Am8226

## Four-Bit Parallel Bidirectional Bus Driver

### Distinctive Characteristics

- Data bus buffer driver for 8080 type CPU's
- Low input load current — 0.25mA maximum
- High output drive capability for driving system data bus — 50mA at 0.5V
- 100% reliability assurance testing in compliance with MIL-STD-883
- Am3216 and Am8216 have non-inverting outputs
- Output high voltage compatible with direct interface to MOS
- Three-state outputs
- Advanced Schottky processing
- Available in military and commercial temperature range
- Am3226 and Am8226 have inverting outputs

### FUNCTIONAL DESCRIPTION

The Am3216, Am3226, Am8216 and Am8226 are four-bit, bi-directional bus drivers for use in bus oriented applications. The non-inverting Am3216 and Am8216, and inverting Am3226 and Am8226 drivers are provided for flexibility in system design.

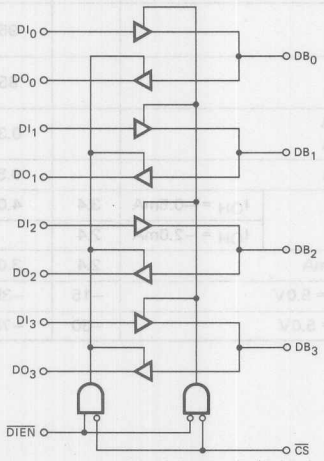
Each buffered line of the four bit driver consists of two separate buffers that are three-state to achieve direct bus interface and bi-directional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB), this side is used to interface to the system side components such as memories, I/O, etc., because its interface is TTL compatible and it has high drive (50mA). On the other side of the driver the inputs and outputs are separated to provide maximum flexibility. Of course, they can be tied together so that the driver can be used to buffer a true bi-directional bus. The DO outputs on this side of the driver have a special high voltage output drive capability so that direct interface to the 8080 type CPUs is achieved with an adequate amount of noise immunity.

The $\overline{CS}$ input is a device enable. When it is "high" the output drivers are all forced to their high-impedance state. When it is a "LOW" the device is enabled and the direction of the data flow is determined by the $\overline{DIEN}$ input.

The $\overline{DIEN}$ input controls the direction of data flow which is accomplished by forcing one of the pair of buffers into its high impedance state and allowing the other to transmit its data. A simple two gate circuit is used for this function.

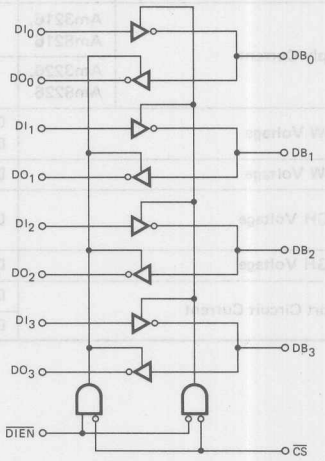
### LOGIC DIAGRAMS

**Am3216 • Am8216**




LIC-439

**Am3226 • Am8226**



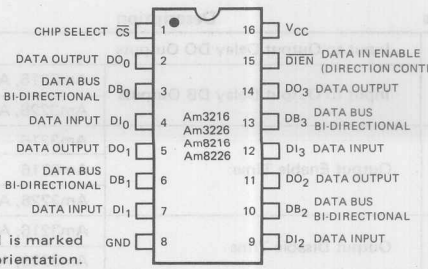

LIC-440

### ORDERING INFORMATION

| Package Type | Temperature Range | Am3216 Am8216 Order Number | Am3226 Am8226 Order Number |
|---|---|---|---|
| Hermetic DIP | –55°C to +125°C | MD3216 | MD3226 |
| Hermetic DIP | 0°C to +70°C | D3216 | D3226 |
| Molded DIP | 0°C to +70°C | P3216 | P3226 |
| Hermetic DIP | –55°C to +125°C | MD8216 | MD8226 |
| Hermetic DIP | 0°C to +70°C | D8216 | D8226 |
| Molded DIP | 0°C to +70°C | P8216 | P8226 |
| Dice | 0°C to +70°C | AM8216XC | AM8226XC |

### CONNECTION DIAGRAM

**Top View**




Note: Pin 1 is marked for orientation.

LIC-441

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Storage Temperature | −65°C to +150°C |
| All Output and Supply Voltages | −0.5 V to +7.0 V |
| All Input Voltages | −1.0 V to +5.5 V |
| Output Currents | 125 mA |

## Am3216, Am3226, Am8216 AND Am8226 MILITARY ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (−55°C to +125°C)

The following conditions apply unless otherwise specified:

MD3216, MD8216, MD3226, MD8226 (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$

### DC CHARACTERISTICS

| Parameters | Description | | Test Conditions | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $I_{F1}$ | Input Load Current $\overline{DIEN}$, $\overline{CS}$ | | $V_F = 0.45$ | | | −0.15 | −0.5 | mA |
| $I_{F2}$ | Input Load Current All Other Inputs | | $V_F = 0.45$ | | | −0.08 | −0.25 | mA |
| $I_{R1}$ | Input Leakage Current $\overline{DIEN}$, $\overline{CS}$ | | $V_R = 5.5V$ | | | | 80 | μA |
| $I_{R2}$ | Input Leakage Current DI Inputs | | $V_R = 5.5V$ | | | | 40 | μA |
| $V_C$ | Input Forward Voltage Clamp | | $I_C = -5.0mA$ | | | | −1.2 | Volts |
| $V_{IL}$ | Input LOW Voltage | Am3216, Am8216 | | | | | 0.95 | Volts |
| | | Am3226, Am8226 | | | | | 0.9 | |
| $V_{IH}$ | Input HIGH Voltage | | | | 2.0 | | | Volts |
| $I_O$ | Output Leakage Current (Three-State) | DO | $V_O = 0.45V/5.5V$ | | | | 20 | μA |
| | | DB | | | | | 100 | |
| $I_{CC}$ | Power Supply Current | Am3216, Am8216 | | | | 95 | 130 | mA |
| | | Am3226, Am8226 | | | | 85 | 120 | |
| $V_{OL1}$ | Output LOW Voltage | | DO Outputs $I_{OL} = 15mA$<br>DB Outputs $I_{OL} = 25mA$ | | | 0.3 | 0.45 | Volts |
| $V_{OL2}$ | Output LOW Voltage | | DB Outputs $I_{OL} = 45mA$ | | | 0.5 | 0.6 | Volts |
| $V_{OH1}$ | Output HIGH Voltage | | DO Outputs | $I_{OH} = -0.5mA$ | 3.4 | 4.0 | | Volts |
| | | | | $I_{OH} = -2.0mA$ | 2.4 | | | |
| $V_{OH2}$ | Output HIGH Voltage | | DB Outputs $I_{OH} = -5.0mA$ | | 2.4 | 3.0 | | Volts |
| $I_{OS}$ | Output Short Circuit Current | | DO Outputs ≅ 0V, $V_{CC} = 5.0V$ | | −15 | −35 | −65 | mA |
| | | | DB Outputs = 0V, $V_{CC} = 5.0V$ | | −30 | −75 | −120 | |

### AC CHARACTERISTICS

| Parameters | Description | | Test Conditions | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $t_{PD1}$ | Input to Output Delay DO Outputs | | $C_L = 30pF$, $R_1 = 300\Omega$, $R_2 = 600\Omega$ | | 15 | 25 | ns |
| $t_{PD2}$ | Input to Output Delay DB Outputs | Am3216, Am8216 | $C_L = 300pF$, $R_1 = 90\Omega$, $R_2 = 180\Omega$ | | 20 | 33 | ns |
| | | Am3226, Am8226 | | | 16 | 25 | |
| $t_E$ | Output Enable Time | Am3216 | Note 3 | | 45 | 75 | ns |
| | | Am8216 | Note 2 | | 45 | 75 | |
| | | Am3226, Am8226 | Note 3 | | 35 | 62 | |
| $t_D$ | Output Disable Time | Am3216, Am8216 | Note 4 | | 20 | 40 | ns |
| | | Am3226, Am8226 | | | 16 | 38 | |

## Am3216, Am3226, Am8216 AND Am8226 COMMERCIAL ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (0°C to +70°C)

The following conditions apply unless otherwise specified:

D3216, D8216, D3226, D8226, P3216, P8216, P3226, P8226 (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$

### DC CHARACTERISTICS

| Parameters | Description | | Test Conditions | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $I_{F1}$ | Input Load Current $\overline{DIEN}$, $\overline{CS}$ | | $V_F = 0.45$ | | −0.15 | −0.5 | mA |
| $I_{F2}$ | Input Load Current All Other Inputs | | $V_F = 0.45$ | | −0.08 | −0.25 | mA |
| $I_{R1}$ | Input Leakage Current $\overline{DIEN}$, $\overline{CS}$ | | $V_R = 5.25V$ | | | 20 | μA |
| $I_{R2}$ | Input Leakage Current DI Inputs | | $V_R = 5.25V$ | | | 10 | μA |
| $V_C$ | Input Forward Voltage Clamp | | $I_C = -5.0mA$ | | | −1.0 | Volts |
| $V_{IL}$ | Input LOW Voltage | | | | | 0.95 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | | | Volts |
| $\|I_{OL}\|$ | Output Leakge Current (Three-State) | DO | $V_O = 0.45V/5.5V$ | | | 20 | μA |
| | | DB | | | | 100 | |
| $I_{CC}$ | Power Supply Current | Am3216, Am8216 | | | 95 | 130 | mA |
| | | Am3226, Am8226 | | | 85 | 120 | |
| $V_{OL1}$ | Output LOW Voltage | | DB Outputs $I_{OL} = 15mA$<br>DB Outputs $I_{OL} = 25mA$ | | 0.3 | 0.45 | Volts |
| $V_{OL2}$ | Output LOW Voltage | Am3216, Am8216 | DB Outputs $I_{OL} = 55mA$ | | 0.5 | 0.6 | Volts |
| | | Am3226, Am8226 | DB Outputs $I_{OL} = 50mA$ | | 0.5 | 0.6 | |
| $V_{OH1}$ | Output HIGH Voltage | | DO Outputs $I_{OH} = -1.0mA$ COM'L | 3.65 | 4.0 | | Volts |
| $V_{OH2}$ | Output HIGH Voltage | | DB Outputs $I_{OH} = -10mA$ | 2.4 | 3.0 | | Volts |
| $I_{OS}$ | Output Short Circuit Current | | DO Outputs ≅ 0V | −15 | −35 | −65 | mA |
| | | | DB Outputs $V_{CC} = 5.0V$ | −30 | −75 | −120 | |

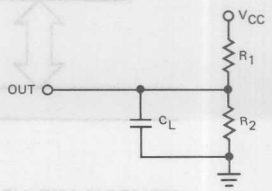
### AC CHARACTERISTICS

| Parameters | Description | | Test Conditions | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $t_{PD1}$ | Input to Output Delay DO Outputs | | $C_L = 30pF$, $R_1 = 300\Omega$, $R_2 = 600\Omega$ | | 15 | 25 | ns |
| $t_{PD2}$ | Input to Output Delay DB Outputs | Am3216, Am8216 | $C_L = 300pF$, $R_1 = 90\Omega$, $R_2 = 180\Omega$ | | 20 | 30 | ns |
| | | Am3226, Am8226 | | | 16 | 25 | |
| $t_E$ | Output Enable Time | Am3216 | Note 3 | | 45 | 65 | ns |
| | | Am8216 | Note 2 | | 45 | 65 | |
| | | Am3226, Am8226 | Note 3 | | 35 | 54 | |
| $t_D$ | Output Disable Time | | Note 4 | | 20 | 35 | ns |

**TEST CONDITIONS**

Input pulse amplitude of 2.5V.
Input rise and fall times of 5.0ns between 1.0 and 2.0 volts.
Output loading is 5.0mA and 10pF.
Speed measurements are made at 1.5V levels.

**TEST LOAD CIRCUIT**



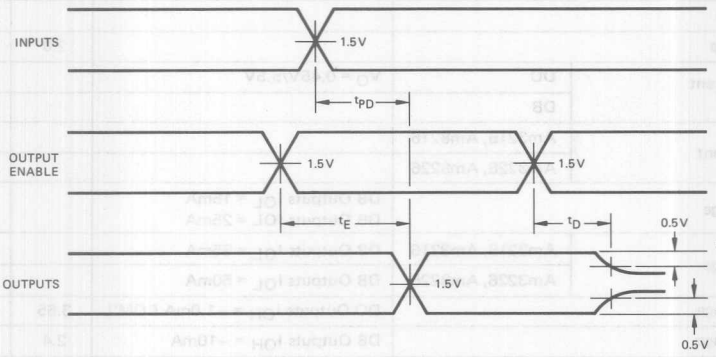

LIC-442

8

| | | | | | | |
|---|---|---|---|---|---|---|
| $C_{OUT1}$ | Output Capacitance | $T_A = 25°C$, f = 1.0MHz | | 13 | 18 | pF |
| $C_{OUT2}$ | Output Capacitance | | | 13 | 18 | pF |

Notes: 1. Typical values are for $T_A = 25°C$, $V_{CC} = 5.0V$.
2. DO outputs, $C_L = 30pF$, $R_1 = 300/10k\Omega$, $R_2 = 180/1.0k\Omega$; DB outputs, $C_L = 300pF$, $R_1 = 90/10k\Omega$, $R_2 = 180/1.0k\Omega$.
3. DO outputs, $C_L = 30pF$, $R_1 = 300/10k\Omega$, $R_2 = 600/1.0k\Omega$; DB outputs, $C_L = 300pF$, $R_1 = 90/10k\Omega$, $R_2 = 180/1.0k\Omega$.
4. DO outputs, $C_L = 5.0pF$, $R_1 = 300/10k\Omega$, $R_2 = 600/1.0k\Omega$; DB outputs, $C_L = 5.0pF$, $R_1 = 90/10k\Omega$, $R_2 = 180/1.0k\Omega$.
5. This parameter is periodically sampled and not 100% tested.

## SWITCHING WAVEFORMS




LIC-443

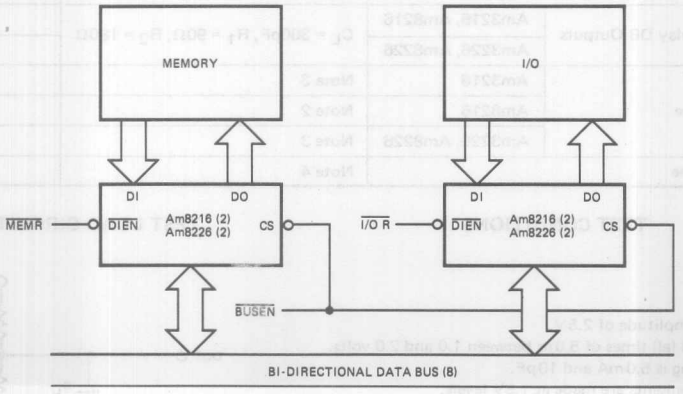
## FUNCTION TABLE

| $\overline{DIEN}$ | $\overline{CS}$ | | 8216 | | 8226 | |
|---|---|---|---|---|---|---|
| | | | DB | DO | DB | DO |
| L | L | DI ⇒ DB | DI | Z | $\overline{DI}$ | Z |
| H | L | DB ⇒ DO | Z | DB | Z | $\overline{DB}$ |
| L | H | | Z | Z | Z | Z |
| H | H | | Z | Z | Z | Z |

H = HIGH
L = LOW

LIC-444

## TYPICAL APPLICATION

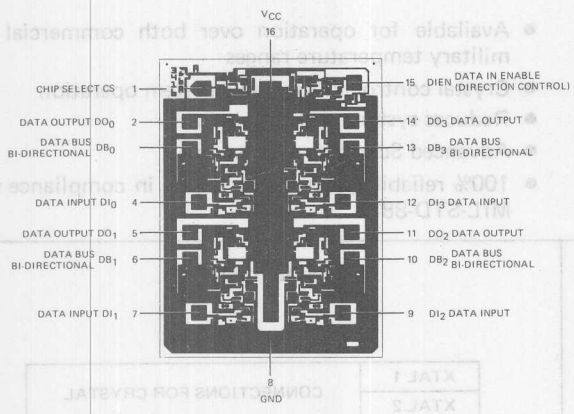



MEMORY AND I/O INTERFACE TO A BI-DIRECTIONAL BUS

LIC-445

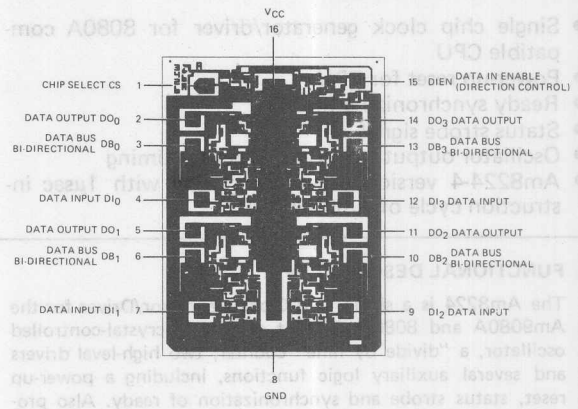
## Metallization and Pad Layout

**Am3216**
**Am8216**




DIE SIZE 0.066" X 0.090"

**Am3226**
**Am8226**




DIE SIZE 0.066" X 0.090"

8

# Am8224

## Clock Generator and Driver for 8080A Compatible Microprocessors

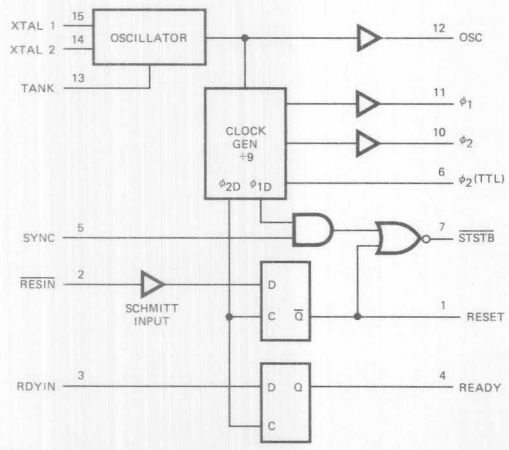
### Distinctive Characteristics

- Single chip clock generator/driver for 8080A compatible CPU
- Power-up reset for CPU
- Ready synchronizing flip-flop
- Status strobe signal
- Oscillator output for external system timing
- Am8224-4 version available for use with 1$\mu$sec instruction cycle of Am9080A-4
- Available for operation over both commercial and military temperature ranges
- Crystal controlled for stable system operation
- Reduces system package count
- Advanced Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

### FUNCTIONAL DESCRIPTION

The Am8224 is a single chip Clock Generator/Driver for the Am9080A and 8080A CPU. It contains a crystal-controlled oscillator, a "divide by nine" counter, two high-level drivers and several auxiliary logic functions, including a power-up reset, status strobe and synchronization of ready. Also provided are TTL compatible oscillator and $\phi_2$ outputs for external system timing. The Am8224 provides the designer with a significant reduction of packages used to generate clocks and timing for the Am9080A or 8080A for both commercial and military temperature range applications. A high speed version, the Am8224-4, is available for use with the high speed Am9080A-4.

### LOGIC DIAGRAM

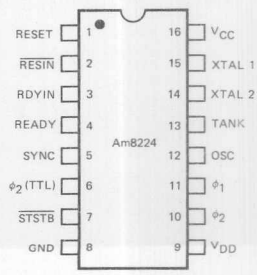



LIC-619

### PIN DEFINITION

| | |
|---|---|
| XTAL 1 | CONNECTIONS FOR CRYSTAL |
| XTAL 2 | |
| TANK | USED WITH OVERTONE XTAL |
| OSC | OSCILLATOR OUTPUT |
| $\phi_2$(TTL) | $\phi_2$ CLK (TTL LEVEL) |
| $V_{CC}$ | +5.0V |
| $V_{DD}$ | +12V |
| GND | 0V |
| $\overline{\text{RESIN}}$ | RESET INPUT |
| RESET | RESET OUTPUT |
| RDYIN | READY INPUT |
| READY | READY OUTPUT |
| SYNC | SYNC INPUT |
| $\overline{\text{STSTB}}$ | STATUS STB (ACTIVE LOW) |
| $\phi_1$ | Am9080A/8080A CLOCKS |
| $\phi_2$ | |

### CONNECTION DIAGRAM
**Top View**




Note: Pin 1 is marked for orientation.

LIC-620

### ORDERING INFORMATION

| Package Type | Temperature Range | Order Number |
|---|---|---|
| Hermetic DIP | –55°C to +125°C | AM8224DM |
| Hermetic DIP | 0°C to +70°C | D8224 |
| Molded DIP | 0°C to +70°C | AM8224PC |
| Dice | 0°C to +70°C | AM8224XC |
| Hermetic DIP | 0°C to +70°C | AM8224-4DC* |

* For use with Am9080A-4 with clock period between 250ns and 320ns.

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Voltage to Ground Potential | |
| $V_{CC}$ | 7.5V |
| $V_{DD}$ | 15V |
| Maximum Output Current $\phi_1$ and $\phi_2$ (Note 1) | 100mA |

## ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

The Following Conditions Apply Unless Otherwise Noted:

Am8224XC, Am8224-4XC (COM'L) $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ $V_{DD} = 12V \pm 5\%$
Am8224XC (MIL) $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ $V_{DD} = 12V \pm 10\%$

| Parameters | Description | Test Conditions | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| $I_F$ | Input Current Loading | $V_F = 0.45V$ | | | | −0.25 | mA |
| $I_R$ | Input Leakage Current | $V_R = 5.25V$ | | | | 10 | μA |
| $V_C$ | Input Forward Clamp Voltage | $I_C = -5.0mA$ | COM'L | | | −1.0 | Volts |
| | | | MIL | | | −1.2 | |
| $V_{IL}$ | Input LOW Voltage | $V_{CC} = 5.0V$ | | | | 0.8 | Volts |
| $V_{IH}$ | Input HIGH Voltage | Reset input | COM'L | 2.6 | 2.2 | | Volts |
| | | | MIL | 2.8 | 2.2 | | |
| | | All other inputs | | 2.0 | | | |
| $V_{IH}$-$V_{IL}$ | $\overline{RESIN}$ Input Hysteresis | $V_{CC} = 5.0V$ | | 0.25 | 0.5 | | Volts |
| $V_{OL}$ | Output LOW Voltage | ($\phi_1$, $\phi_2$), Ready, Reset, $\overline{STSTB}$ $I_{OL} = 2.5mA$ | | | | 0.45 | Volts |
| | | All other inputs $I_{OL} = 15mA$ | | | | 0.45 | |
| $V_{OH}$ | Output HIGH Voltage | $\phi_1$, $\phi_2$; $I_{OH} = -100\mu A$ | COM'L | 9.4 | 11 | | Volts |
| | | | MIL | $V_{DD} - 1.6V$ | $V_{DD} - 1.0V$ | | |
| | | READY, RESET; $I_{OH} = -100\mu A$ | COM'L | 3.6 | 4.0 | | |
| | | | MIL | 3.35 | 4.0 | | |
| | | All other outputs; $I_{OH} = -1.0mA$ | | 2.4 | 3.0 | | |
| $I_{SC}$ | Output Short Circuit Current (All Low Voltage Outputs Only) | $V_O = 0V$ $V_{CC} = 5.0V$ | | −10 | | −60 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. (Note 3) | | | 70 | 115 | mA |
| $I_{DD}$ | Power Supply Current | $V_{DD}$ = MAX. | | | 5.0 | 12 | mA |

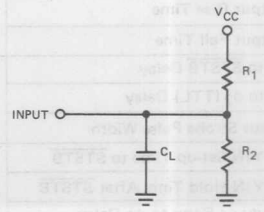
Notes: 1. Caution: $\phi_1$ and $\phi_2$ outputs do not have short circuit protection.
2. Typical limits are at $V_{CC} = 5.0V$, $V_{DD} = 12V$, 25°C ambient and maximum loading.
3. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.

### CRYSTAL REQUIREMENTS

Tolerance: .005% at 0°C – 70°C
Resonance: Series (Fundamental)*
Load Capacitance: 20-35pF
Equivalent Resistance: 75-20 ohms
Power Dissipation (Min): 4mW

*With frequency in excess of 18MHz use 3rd overtone XTALs and tank circuit.

### TEST CIRCUIT




LIC-621

## AC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

| Parameters | Description | Test Conditions | Am8224XM Min. | Am8224XM Typ. | Am8224XM Max. | Am8224XC Min. | Am8224XC Typ. | Am8224XC Max. | Am8224-4XC (Note 2) Min. | Am8224-4XC (Note 2) Typ. | Am8224-4XC (Note 2) Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{\phi 1}$ | $\phi_1$ Pulse Width | $C_L$ = 20pF to 50pF | $\frac{2t_{CY}}{9}$ − 23ns | | | $\frac{2t_{CY}}{9}$ − 20ns | | | 45 | | | ns |
| $t_{\phi 2}$ | $\phi_2$ Pulse Width | | $\frac{5t_{CY}}{9}$ − 35ns | | | $\frac{5t_{CY}}{9}$ − 35ns | | | 110 | | | |
| $t_{D1}$ | $\phi_1$ to $\phi_2$ Delay | | 0 | | | 0 | | | 0 | | | |
| $t_{D2}$ | $\phi_2$ to $\phi_1$ Delay | | $\frac{2t_{CY}}{9}$ − 17ns | | | $\frac{2t_{CY}}{9}$ − 14ns | | | 35 | | | |
| $t_{D3}$ | $\phi_1$ to $\phi_2$ Delay | | $\frac{2t_{CY}}{9}$ | | $\frac{2t_{CY}}{9}$ + 22ns | $\frac{2t_{CY}}{9}$ | | $\frac{2t_{CY}}{9}$ + 20ns | 55 | | 76 | |
| $t_r$ | $\phi_1$ and $\phi_2$ Rise Time | | | | 20 | | | 20 | | | 20 | |
| $t_f$ | $\phi_1$ and $\phi_2$ Fall Time | | | | 20 | | | 20 | | | 20 | |
| $t_{D\phi 2}$ | $\phi_2$ to $\phi_2$(TTL) Delay | $\phi_2$(TTL), $C_L$ = 30pF, $R_1$ = 300Ω, $R_2$ = 600Ω | −5.0 | | 15 | −5.0 | | 15 | −5.0 | | 15 | ns |
| $t_{DSS}$ | $\phi_2$ to $\overline{STSTB}$ Delay | $\overline{STSTB}$, $C_L$ = 15pF, $R_1$ = 2.0kΩ, $R_2$ = 4.0kΩ | $\frac{6t_{CY}}{9}$ − 33ns | | $\frac{6t_{CY}}{9}$ | $\frac{6t_{CY}}{9}$ − 30ns | | $\frac{6t_{CY}}{9}$ | 137 | | 167 | ns |
| $t_{PW}$ | $\overline{STSTB}$ Pulse Width | | $\frac{t_{CY}}{9}$ − 18ns | | | $\frac{t_{CY}}{9}$ − 15ns | | | 18 | | | |
| $t_{DRS}$ | RDYIN Set-up Time to Status Strobe | | 50ns − $\frac{4t_{CY}}{9}$ | | | 50ns − $\frac{4t_{CY}}{9}$ | | | −61 | | | |
| $t_{DRH}$ | RDYIN Hold Time After STSTB | | $\frac{4t_{CY}}{9}$ | | | $\frac{4t_{CY}}{9}$ | | | 111 | | | |
| $t_{DR}$ | RDYIN or RESIN to $\phi_2$ Delay | Ready and Reset $C_L$ = 10pF, $R_1$ = 2.0kΩ, $R_2$ = 4.0kΩ | $\frac{4t_{CY}}{9}$ − 25ns | | | $\frac{4t_{CY}}{9}$ − 25ns | | | 86 | | | ns |
| $t_{CLK}$ | CLK Period | | | $\frac{t_{CY}}{9}$ | | | $\frac{t_{CY}}{9}$ | | | 28 | | |
| $f_{Max.}$ | Maximum Oscillating Frequency | | 27 | | | 28.12 | | | 36 | | | MHz |
| $C_{in}$ | Input Capacitance | $V_{CC}$ = 5.0V, $V_{DD}$ = 12V, $V_{BIAS}$ = 2.5V, f = 1.0MHz | | | 8.0 | | | 8.0 | | | 8.0 | pF |

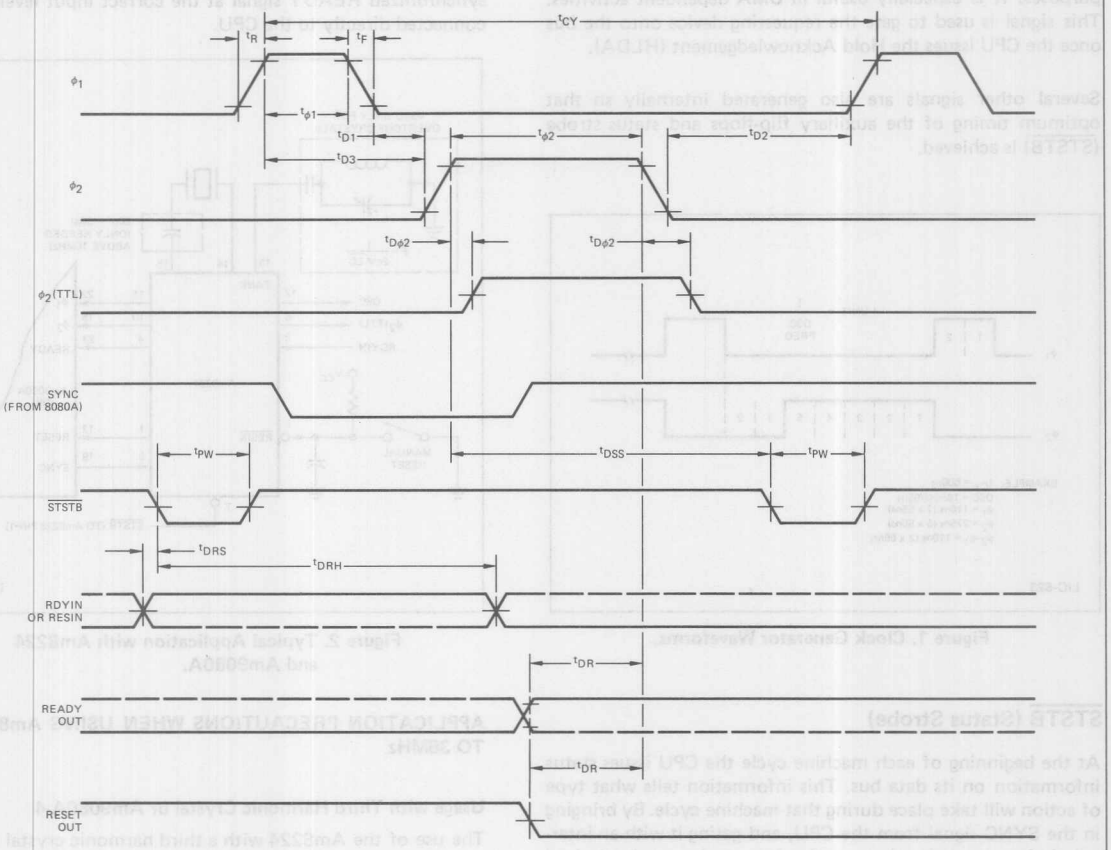
## AC CHARACTERISTICS (For $t_{CY}$ = 488.28ns)

$T_A$ = 0°C to +70°C  $V_{CC}$ = +5.0V ±5%  $V_{DD}$ = +12V ±5%

| Parameters | Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $t_{\phi 1}$ | $\phi_1$ Pulse Width | $\phi_1$ and $\phi_2$ Loaded, $C_L$ = 20 to 50pF | 89 | | | ns |
| $t_{\phi 2}$ | $\phi_2$ Pulse Width | | 236 | | | ns |
| $t_{D1}$ | Delay $\phi_1$ to $\phi_2$ | | 0 | | | ns |
| $t_{D2}$ | Delay $\phi_2$ to $\phi_1$ | | 95 | | | ns |
| $t_{D3}$ | Delay $\phi_1$ to $\phi_2$ Leading Edges | | 109 | | 129 | ns |
| $t_r$ | Output Rise Time | | | | 20 | ns |
| $t_f$ | Output Fall Time | | | | 20 | ns |
| $t_{DSS}$ | $\phi_2$ to $\overline{STSTB}$ Delay | | 296 | | 326 | ns |
| $t_{D\phi 2}$ | $\phi_2$ to $\phi_2$(TTL) Delay | | −5.0 | | 15 | ns |
| $t_{PW}$ | Status Strobe Pulse Width | | 40 | | | ns |
| $t_{DRS}$ | RDYIN Set-up Time to $\overline{STSTB}$ | Ready and Reset Loaded, $C_L$ = 20 to 50pF, $R_1$ = 2.0kΩ, $R_2$ = 4.0kΩ | −167 | | | ns |
| $t_{DRH}$ | RDYIN Hold Time After $\overline{STSTB}$ | | 217 | | | ns |
| $t_{DR}$ | Ready or Reset to $\phi_2$ Delay | | 192 | | | ns |
| FREQ | Oscillator Frequency | | | | 18.432 | MHz |

Notes: 1. All measurements referenced to 1.5V unless specified otherwise.
2. Am8224-4 parameter limits are given for $t_{CY}$ = 250ns or an oscillating frequency of 36MHz. Between 28.12MHz and 36MHz min. and max. limits should be ratioed between the calculated Am8224XC limits at 28.12MHz and the given 36MHz parameter limits.

## SWITCHING WAVEFORMS




Voltage measurement points: $\phi_1$, $\phi_2$ Logic "0" = 1.0V, Logic "1" = 8.0V.
All other signals measured at 1.5V.

LIC-622

8

### Oscillator

The oscillator circuit derives its basic operating frequency from an external, series resonant, fundamental mode crystal. Two inputs are provided for the crystal connections (XTAL1, XTAL2).

The selection of the external crystal frequency depends mainly on the speed at which the CPU is to be run. Basically, the oscillator operates at 9 times the desired processor speed.

The formula to determine the crystal frequency is:

$$f(XTAL) = \frac{1}{t_{CY}} \text{ times } 9$$

When using crystals above 10MHz a small amount of frequency "trimming" is necessary to produce the desired frequency. The addition of a selected capacitance (20pF – 30pF) in series with the crystal will accomplish this function.

Another input to the oscillator is TANK. This input allows the use overtone mode crystals. This type of crystal generally has a much lower output at its rated frequency and has a tendency to oscillate at its fundamental.

To avoid the unwanted oscillation and increase the desired frequency output it is necessary to provide a parallel tuned resonant circuit of low impedance. The external LC network is connected to the TANK input and is AC coupled. See typical application with Am8228 and Am9080A in Figure 2.

The formula for the LC network is:

$$F = \frac{1}{2\pi\sqrt{LC}}$$

The output of the oscillator is buffered and brought out on OSC (pin 12) so that other system timing signals can be derived from this stable, crystal-controlled source.

### Clock Generator

The Clock Generator consists of a synchronous "divide by nine" counter and the associated decode gating to create the waveforms of the two clocks and auxiliary timing signals.

The waveforms generated by the decode gating follow a simple 2-5-2 digital pattern. See Figure 2. The clocks generated; $\phi_1$ and $\phi_2$, can best be thought of as consisting of "units" based on the oscillator frequency. Assume that one "unit" equals the period of the oscillator frequency. By multiplying the number of "units" that are contained in a pulse width or delay, times the period of the oscillator frequency, the approximate time in nanoseconds can be derived.

The outputs of the clock generator are connected to two high level drivers for direct interface to the CPU. A TTL level phase 2 is also brought out $\phi_2$ (TTL) for external timing purposes. It is especially useful in DMA dependent activities. This signal is used to gate the requesting device onto the bus once the CPU issues the Hold Acknowledgement (HLDA).

Several other signals are also generated internally so that optimum timing of the auxiliary flip-flops and status strobe ($\overline{STSTB}$) is achieved.

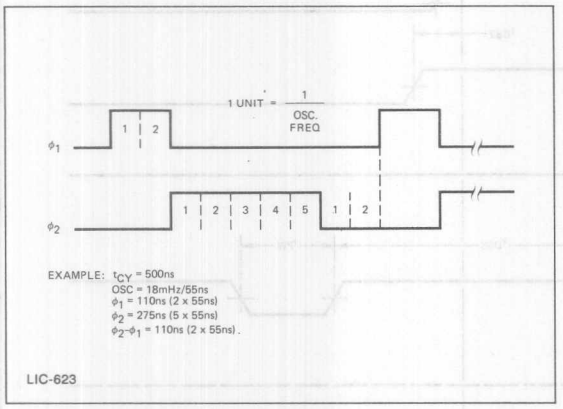



**Figure 1. Clock Generator Waveforms.**

flop is required. The Am8224 has this feature built-in. The RDYIN input presents the asynchronous "wait request" to the "D" type flip-flop. By clocking the flip-flop with $\phi_{2D}$, a synchronized READY signal at the correct input level, can be connected directly to the CPU.

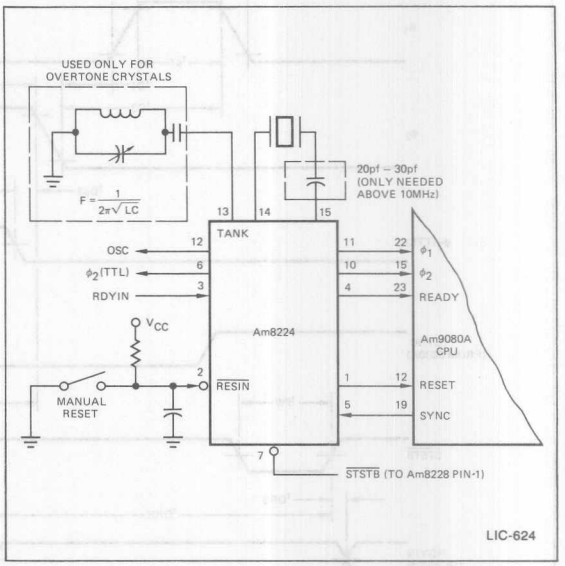



**Figure 2. Typical Application with Am8224 and Am9080A.**

## $\overline{STSTB}$ (Status Strobe)

At the beginning of each machine cycle the CPU issues status information on its data bus. This information tells what type of action will take place during that machine cycle. By bringing in the SYNC signal from the CPU, and gating it with an internal timing signal ($\phi_{1A}$), an active low strobe can be derived that occurs at the start of each machine cycle at the earliest possible moment that status data is stable on the bus. The $\overline{STSTB}$ signal connects directly to the Am8228 System Controller.

The power-on Reset also generates $\overline{STSTB}$, but of course, for a longer period of time. This feature allows the Am8228 to be automatically reset without additional pins devoted for this function.

## Power-On Reset and Ready Flip-Flops

A common function in microcomputer systems is the generation of an automatic system reset and start-up upon initial power-on. The Am8224 has a built-in feature to accomplish this feature.

An external RC network is connected to the $\overline{RESIN}$ input. The slow transition of the power supply rise is sensed by an internal Schmitt Trigger. This circuit converts the slow transition into a clean, fast edge when its input level reaches a predetermined value. The output of the Schmitt Trigger is connected to a "D" type flip-flop that is clocked with $\phi_{2D}$ (an internal timing signal). The flip-flop is synchronously reset and an active high level that complies with the microprocessor input spec is generated. For manual switch type system Reset circuits, an active low switch closing can be connected to the RESIN input in addition to the power-on RC network.

The READY input to the CPU has certain timing specifications such as "set-up and hold" thus, an external synchronizing flip-

## APPLICATION PRECAUTIONS WHEN USING Am8224 UP TO 36MHz

### Usage with Third Harmonic Crystal or Am9080A-4

The use of the Am8224 with a third harmonic crystal requires a minor modification to the external circuitry associated with the Am8224. The changes are as follows:

- Series capacitor in conjunction with the xtal
- Adding a tuned circuit in the "tank" lead
- Tuning of circuit to proper frequency

It is necessary to maintain the crystal activity to a proper level if an xtal controlled circuit is to operate properly. A 20-30pfd capacitor placed in series will help achieve this level in third overtone crystal, while helping to suppress the fundamental mode. The Am8224 has an auxiliary port provided to allow for a tuned circuit. This tuned circuit eliminates the tendency of the circuit to oscillate at the crystal's fundamental. The tank or tuned circuit must have the following properties:

1. It must be parallel resonant at the crystal frequency (third order).
2. The off resonance impedance must be low enough to spoil the AC gain of the Am8224.
3. The circuit must be DC decoupled (or returned to $V_{CC}$) at a low impedance (substantially below 100Ω).

All frequency determining components must be in close proximity to the Am8224. Insert crystal and tune tank for best waveform at Pin 12 (OSC). If counter is available, adjust for match of crystal marking. The circuit in Figure 3 will accomplish the above result for the 36MHz range.

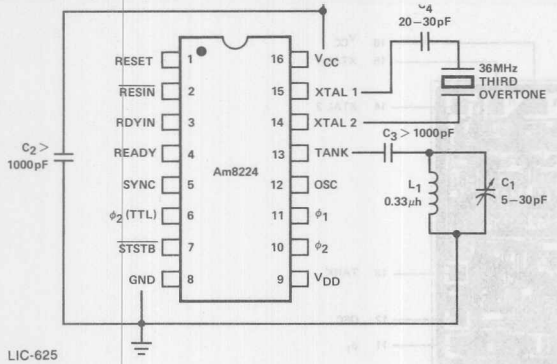



**Figure 3.**

$C_1$ = E.F. Johnson
275-0430-005
5-30pF Trimmer or Equiv.

$L_1$ = J.W. Miller Inductor
9230-08

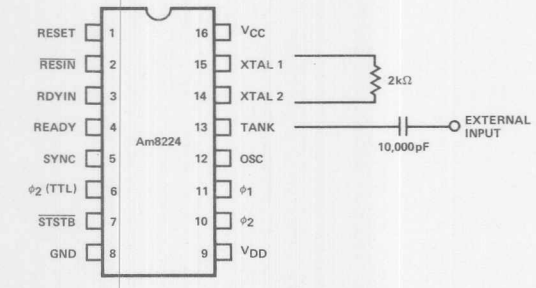
Due to the nature of our device (fast switching, higher voltage) it is necessary to provide a bypass capacitor from $V_{CC}$ to ground in the immediate proximity of the Am8224. This insures proper operation of the device while reducing noise spiking on adjacent circuits.

### Resin Bypass

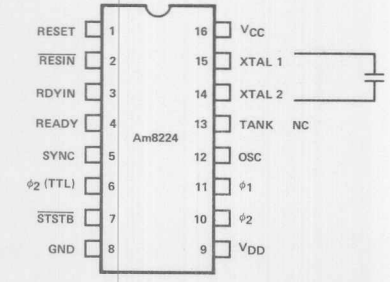
The use of a high impedance capacitor for timing R-C, and/or timing components remotely located from the Am8224 device may cause a disturbance to occur during the linear transition region. The capacitor for this function should be of the ceramic type and a value of 1000pF or greater.

This can be cured by placing a >1000pfd ceramic capacitor from Resin (Pin 2) to Ground (Pin 8) in the immediate proximity of the device. This will allow the timing R-C to be placed at will.

## APPLICATIONS



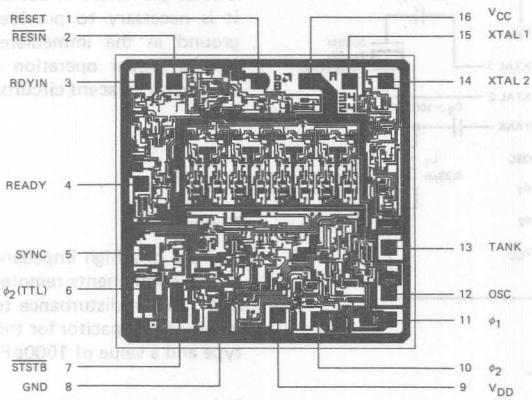

The Am8224 can be driven from an external source of frequency by connecting as shown and driven with approximately 500mV over a wide frequency range.




The Am8224 can oscillate without a xtal by placing a small value capacitor (10→200pF) in place of a crystal.

8

## Metallization and Pad Layout




DIE SIZE 0.085" X 0.084"

# Am8228 • Am8238

## System Controller and Bus Driver for 8080A Compatible Microprocessors

### Distinctive Characteristics

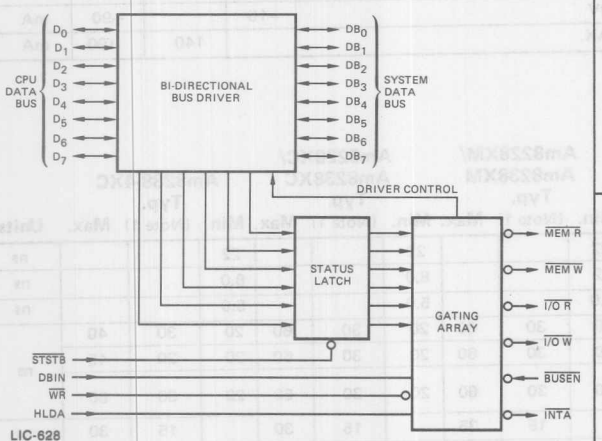
- Multi-byte instruction interrupt acknowledge
- Selectable single level vectored interrupt (RST-7)
- 28-pin molded or hermetic DIP package
- Single chip system controller and data bus driver for Am9080/8080A systems
- Am8238-4 high speed version available for use with 1μsec instruction cycle of Am9080A-4
- Bi-directional three-state bus driver for CPU independent operation
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- Available in military and commercial temperature range
- Am8238 has extended $\overline{IOW}/\overline{MEMW}$ pulse width

### FUNCTIONAL DESCRIPTION

The Am8228 and Am8238 are single chip System Controller Data Bus drivers for the Am9080A Microcomputer System. They generate all control signals required to directly interface Am9080A/8080A compatible system circuits (memory and I/O) to the CPU.

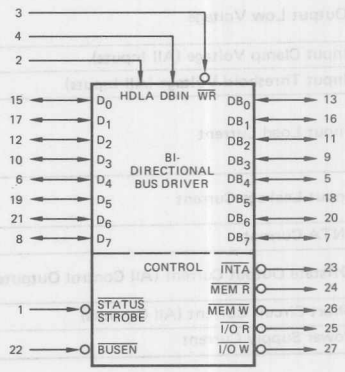
Bi-directional bus drivers with three-state outputs are provided for the system data bus, facilitating CPU independent bus operations such as direct memory access. Interrupt processing is accommodated by means of a single vectored interrupt or by means of the standard 8080A multiple byte interrupt vector operation.

### LOGIC DIAGRAM




LIC-628

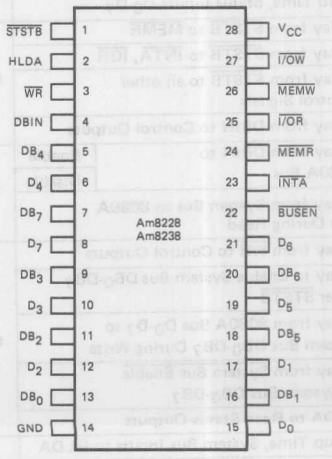
### LOGIC SYMBOL




$V_{CC}$ = Pin 28
GND = Pin 14

LIC-629

### CONNECTION DIAGRAM
Top View




Note: Pin 1 is marked for orientation.

LIC-630

### ORDERING INFORMATION

| Package Type | Temperature Range | Am8228 Order Number | Am8238 Order Number |
|---|---|---|---|
| Molded DIP | 0°C to +70°C | AM8228PC | AM8238PC |
| Hermetic DIP | 0°C to +70°C | D8228 | D8238 |
| Hermetic DIP | −55°C to +125°C | AM8228DM | AM8238DM |
| Dice | 0°C to +70°C | AM8228XC | AM8238XC |
| Hermetic DIP | 0°C to +70°C | | AM8238-4DC* |
| Molded DIP | 0°C to +70°C | | AM8238-4PC* |

*For use with Am9080A-4 with minimum clock period of 250ns.

8

## MAXIMUM RATINGS (Above which the useful life may be impaired)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Temperature (Ambient) Under Bias | −55°C to +125°C |
| Supply Volatge to Ground Potential (Pin 28 to Pin 14) Continuous | −0.5V to +7.0V |
| DC Voltage Applied to Outputs for HIGH Output State | −0.5V to +$V_{CC}$ max. |
| DC Input Voltage | −1.5V to +7.0V |
| DC Output Current, Into Outputs | 50mA |
| DC Input Current | −30mA to +5.0mA |

## ELECTRICAL CHARACTERISTICS The Following Conditions Apply Unless Otherwise Noted:

| | | | |
|---|---|---|---|
| Am8228XM, Am8238XM | $T_A$ = −55°C to +125°C | $V_{CC}$MIN. = 4.50V | $V_{CC}$MAX. = 5.50V |
| Am8228XC, Am8238XC, Am8238-4XC | $T_A$ = 0°C to +70°C | $V_{CC}$MIN. = 4.75V | $V_{CC}$MAX. = 5.25V |

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

| Parameters | Description | Test Conditions (Note 2) | | | | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN. | $I_{OH}$ = −10μA | $D_0$–$D_7$ | MIL | 3.35 | 3.8 | | Volts |
| | | | | | COM'L | 3.6 | 3.8 | | |
| | | | $I_{OH}$ = −1.0mA | All other outputs | | 2.4 | | | |
| $V_{OL}$ | Output Low Voltage | $V_{CC}$ = MIN. | $I_{OL}$ = 2.0mA | $D_0$–$D_7$ | | | | 0.45 | Volts |
| | | | $I_{OL}$ = 10mA | All other outputs | | | | 0.45 | |
| $V_C$ | Input Clamp Voltage (All Inputs) | $V_{CC}$ = MIN., $I_C$ = −5.0mA | | | | | −0.75 | −1.0 | Volts |
| $V_{TH}$ | Input Threshold Voltage (All Inputs) | $V_{CC}$ = 5.0V | | | | 0.8 | | 2.0 | Volts |
| $I_F$ | Input Load Current | $V_{CC}$ = MAX., $V_F$ = 0.45V | | $\overline{STSTB}$ | | | | −500 | μA |
| | | | | $D_2$ and $D_6$ | | | | −750 | |
| | | | | All other inputs | | | | −250 | |
| $I_R$ | Input Leakage Current | $V_{CC}$ = MAX., $V_R$ = 5.25V | | $DB_0$–$DB_7$ | | | | 20 | μA |
| | | | | All other inputs | | | | 100 | |
| $I_{INT}$ | INTA Current | See INTA test circuit | | | | | | 5.0 | mA |
| $I_{O(OFF)}$ | Offstate Output Current (All Control Outputs) | $V_{CC}$ = MAX., $V_O$ = 5.25V | | | | | | 100 | μA |
| | | $V_O$ = 0.45V | | | | | | −100 | |
| $I_{OS}$ | Short Circuit Current (All Outputs) | $V_{CC}$ = 5.0V | | | | −15 | | −90 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX. | | | | | 140 | 190 | mA |

## AC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

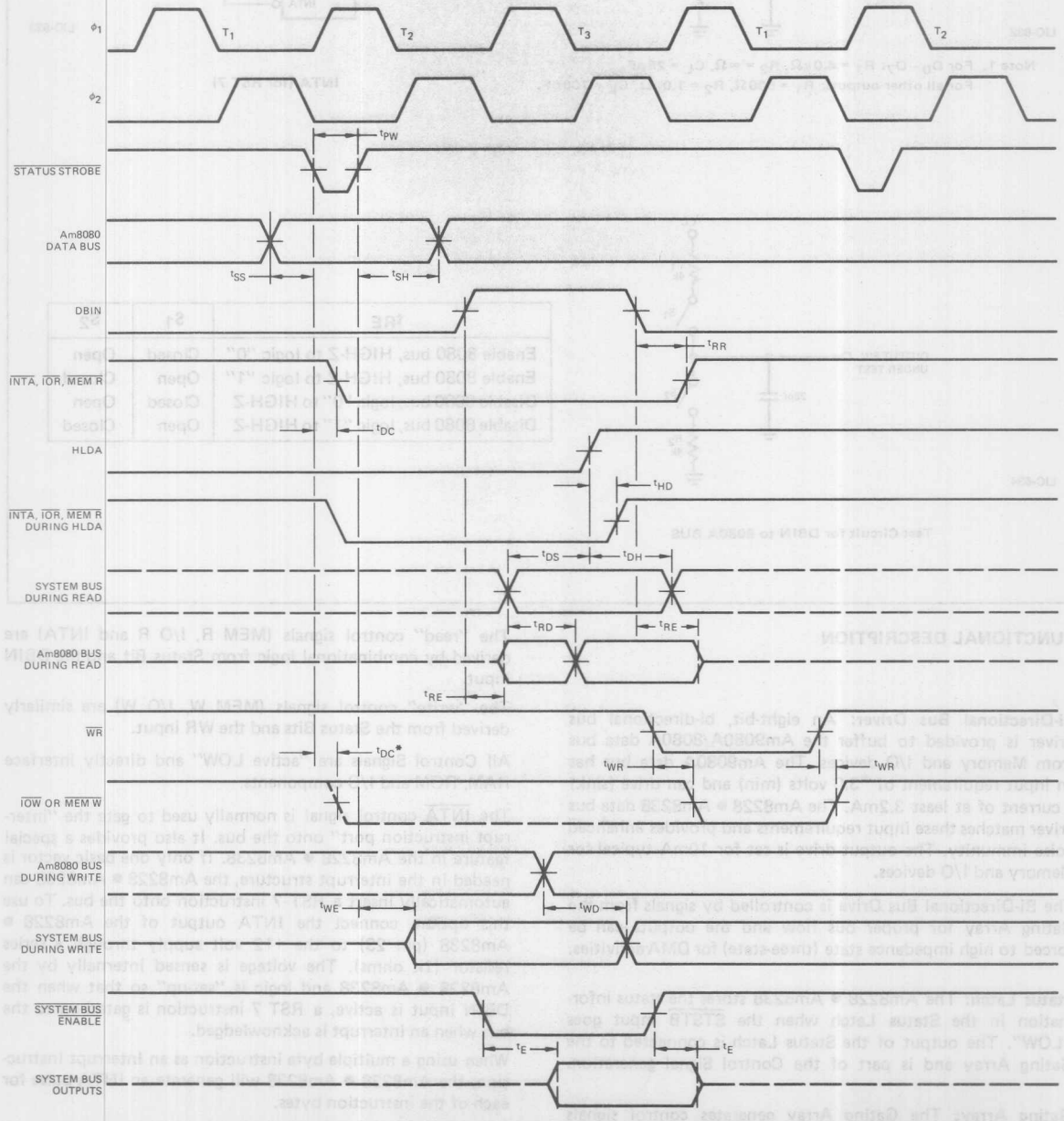
| Parameters | Description | | Test Conditions | Am8228XM/ Am8238XM Min. | Typ. (Note 1) | Max. | Am8228XC/ Am8238XC Min. | Typ. (Note 1) | Max. | Am8238-4XC Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PW}$ | Width of Status Strobe | | | 22 | | | 22 | | | 22 | | | ns |
| $t_{SS}$ | Set-up Time, Status Inputs $D_0$-$D_7$ | | | 12 | | | 8.0 | | | 8.0 | | | ns |
| $t_{SH}$ | Hold Time, Status Inputs $D_0$-$D_7$ | | | 5.0 | | | 5.0 | | | 5.0 | | | ns |
| $t_{DC}$ | Delay from $\overline{STSTB}$ to $\overline{MEMR}$ | | $C_L$ = 100pF | 20 | 30 | 60 | 20 | 30 | 60 | 20 | 30 | 40 | ns |
| | Delay from $\overline{STSTB}$ to $\overline{INTA}$, $\overline{IOR}$ | | | 20 | 30 | 60 | 20 | 30 | 60 | 20 | 30 | 45 | |
| | Delay from $\overline{STSTB}$ to all other Control Signals | | | 20 | 30 | 60 | 20 | 30 | 60 | 20 | 30 | 60 | |
| $t_{RR}$ | Delay from DBIN to Control Outputs | | | | 15 | 35 | | 15 | 30 | | 15 | 30 | ns |
| $t_{RE}$ | Delay from DBIN to 8080A Bus | Enable | $C_L$ = 25pF | | 25 | 45 | | 25 | 45 | | 12 | 20 | ns |
| | | Disable | | | 25 | 45 | | 25 | 45 | | 25 | 35 | |
| $t_{RD}$ | Delay from System Bus to 8080A Bus During Read | | | | 15 | 30 | | 15 | 30 | | 15 | 20 | ns |
| $t_{WR}$ | Delay from $\overline{WR}$ to Control Outputs | | $C_L$ = 100pF | 5.0 | 20 | 45 | 5.0 | 20 | 45 | 5.0 | 20 | 45 | ns |
| $t_{WE}$ | Delay to Enable System Bus $DB_0$-$DB_7$ After $\overline{STSTB}$ | | | | 25 | 36 | | 25 | 30 | | 25 | 30 | ns |
| $t_{WD}$ | Delay from 8080A Bus $D_0$-$D_7$ to System Bus $DB_0$-$DB_7$ During Write | | | 5.0 | 20 | 40 | 5.0 | 20 | 40 | 5.0 | 20 | 40 | ns |
| $t_E$ | Delay from System Bus Enable to System Bus $DB_0$-$DB_7$ | | | | 25 | 35 | | 25 | 30 | | 20 | 30 | ns |
| $t_{HD}$ | HLDA to Read Status Outputs | | | | 15 | 28 | | 15 | 25 | | 15 | 25 | ns |
| $t_{DS}$ | Set-up Time, System Bus Inputs to HLDA | | | 10 | | | 10 | | | 10 | | | ns |
| $t_{DH}$ | Hold Time, System Bus Inputs to HLDA | | | 20 | | | 20 | | | 20 | | | ns |

Notes: 1. Typical values are for $T_A$ = 25°C and nominal supply voltages.
2. For conditions shown as MIN. or MAX., use the appropriate value specified under electrical characteristics for the applicable device type.

**CAPACITANCE** (This parameter is periodically sampled and not 100% tested.)

| Parameters | Description | Test Conditions | Min. | Typ. (Note 1) | Max. | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{BIAS}$ = 2.5V, $V_{CC}$ = 5.0V, $T_A$ = 25°C, f = 1.0MHz | | 8.0 | 12 | pF |
| $C_{OUT}$ | Output Capacitance Control Signals | | | 7.0 | 15 | pF |
| I/O | I/O Capacitance (D or DB) | | | 8.0 | 15 | pF |

## SWITCHING WAVEFORMS

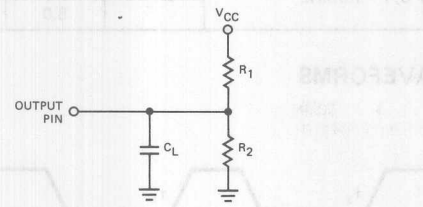



Voltage measurements points: $D_0-D_7$ (when outputs) Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

*Extended IOW/MEMW for Am8238 only.

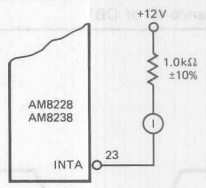
LIC-631

## TEST CIRCUITS



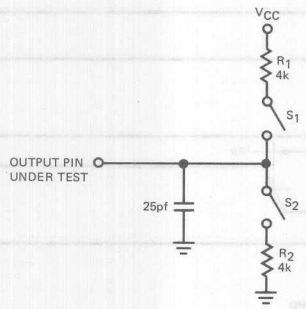

LIC-632

Note 1. For $D_0-D_7$: $R_1 = 4.0k\Omega$, $R_2 = \infty\Omega$, $C_L = 25pF$.
For all other outputs: $R_1 = 500\Omega$, $R_2 = 1.0k\Omega$, $C_L = 100pF$.




LIC-633

INTA (for RST 7)




LIC-634

Test Circuit for DBIN to 8080A BUS

| tRE | S1 | S2 |
|---|---|---|
| Enable 8080 bus, HIGH-Z to logic "0" | Closed | Open |
| Enable 8080 bus, HIGH-Z to logic "1" | Open | Closed |
| Disable 8080 bus, logic "0" to HIGH-Z | Closed | Open |
| Disable 8080 bus, logic "1" to HIGH-Z | Open | Closed |

## FUNCTIONAL DESCRIPTION

**Bi-Directional Bus Driver:** An eight-bit, bi-directional bus driver is provided to buffer the Am9080A/8080A data bus from Memory and I/O devices. The Am9080A data bus has an input requirement of *3.0 volts (min) and can drive (sink) a current of at least 3.2mA. The Am8228 • Am8238 data bus driver matches these input requirements and provides enhanced noise immunity. The output drive is set for 10mA typical for Memory and I/O devices.

The Bi-Directional Bus Drive is controlled by signals from the Gating Array for proper bus flow and the outputs can be forced to high impedance state (three-state) for DMA activities.

**Status Latch:** The Am8228 • Am8238 stores the status information in the Status Latch when the $\overline{STSTB}$ input goes "LOW". The output of the Status Latch is connected to the Gating Array and is part of the Control Signal generation.

**Gating Array:** The Gating Array generates control signals ($\overline{MEM\ R}$, $\overline{MEM\ W}$, $\overline{I/O\ R}$, $\overline{I/O\ W}$ and $\overline{INTA}$) by gating the *outputs of the Status Latch Am9080A signals; i.e.,* DBIN, WE, and HLDA.

*The 8080A has an input requirement of 3.3V and can drive a maximum current of 1.9mA.

The "read" control signals (MEM R, I/O R and INTA) are derived by combinational logic from Status Bit and the DBIN input.

The "write" control signals (MEM W, I/O W) are similarly derived from the Status Bits and the WR input.

All Control Signals are "active LOW" and directly interface RAM, ROM and I/O components.

The $\overline{INTA}$ control signal is normally used to gate the "interrupt instruction port" onto the bus. It also provides a special feature in the Am8228 • Am8238. If only one basic vector is needed in the interrupt structure, the Am8228 • Am8238 can automatically insert a RST 7 instruction onto the bus. To use this option, connect the INTA output of the Am8228 • Am8238 (pin 23) to the +12 volt supply through a series resistor (1k ohms). The voltage is sensed internally by the Am8228 • Am8238 and logic is "set-up" so that when the DBIN input is active, a RST 7 instruction is gated on to the bus when an interrupt is acknowledged.

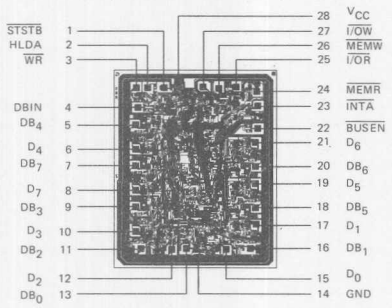
When using a multiple byte instruction as an Interrupt Instruction, the Am8228 • Am8238 will generate an INTA pulse for each of the instruction bytes.

The BUSEN (Bus Enable) input of the Gating Array is an asynchronous input that forces the data bus output buffers and control signal buffers into their high-impedance state if it is a "HIGH". If BUSEN is a "LOW", normal operation of the data buffer and control signals take place. This facilitates CPU independent bus operations such as direct memory access.

## DEFINITION OF FUNCTIONAL TERMS

| | |
|---|---|
| $D_7$-$D_0$ | Data bus to-from Am9080A/8080A |
| $DB_7$-$DB_0$ | Data bus to-from user system |
| $\overline{I/OR}$ | Input/output read strobe output active LOW |
| $\overline{I/OW}$ | Input/output write strobe output active LOW |
| $\overline{MEM\ R}$ | Memory read strobe, output, active LOW |
| $\overline{MEM\ W}$ | Memory write strobe, output, active LOW |
| DBIN | Data bus input strobe, input active HIGH |
| $\overline{INTA}$ | Interrupt acknowledge strobe, input, active LOW |
| HLDA | Hold input from Am9080A/8080A active HIGH |
| $\overline{WR}$ | Write input strobe, active HIGH |
| $\overline{BUSEN}$ | BUS ENABLE INPUT, input, 3-state output control, active LOW for 3-state out |
| $\overline{STSTB}$ | Status Strobe, input, strobes status on data bus into status latch, active LOW |

### Metallization and Pad Layout




DIE SIZE 0.110" X 0.136"

## LOADING RULES

| Signal | Pin No. | Input Load | Output Sink | Output Source |
|---|---|---|---|---|
| $D_0$ | 15 | 250μA | 2mA | −10μA |
| $D_1$ | 17 | 250μA | 2mA | −10μA |
| $D_2$ | 12 | 750μA | 2mA | −10μA |
| $D_3$ | 10 | 250μA | 2mA | −10μA |
| $D_4$ | 6 | 250μA | 2mA | −10μA |
| $D_5$ | 19 | 250μA | 2mA | −10μA |
| $D_6$ | 21 | 750μA | 2mA | −10μA |
| $D_7$ | 8 | 250μA | 2mA | −10μA |
| $DB_0$ | 13 | 250μA | 10mA | −1mA |
| $DB_1$ | 16 | 250μA | 10mA | −1mA |
| $DB_2$ | 11 | 250μA | 10mA | −1mA |
| $DB_3$ | 9 | 250μA | 10mA | −1mA |
| $DB_4$ | 5 | 250μA | 10mA | −1mA |
| $DB_5$ | 18 | 250μA | 10mA | −1mA |
| $DB_6$ | 20 | 250μA | 10mA | −1mA |
| $DB_7$ | 7 | 250μA | 10mA | −1mA |
| $\overline{STSTB}$ | 1 | 500μA | — | — |
| DBIN | 4 | 250μA | — | — |
| $\overline{WR}$ | 3 | 250μA | — | — |
| HLDA | 2 | 250μA | — | — |
| $\overline{MEM\ R}$ | 24 | — | 10mA | −1mA |
| $\overline{MEM\ W}$ | 26 | — | 10mA | −1mA |
| $\overline{I/OR}$ | 25 | — | 10mA | −1mA |
| $\overline{IOW}$ | 27 | — | 10mA | −1mA |
| $\overline{BUSEN}$ | 22 | 250μA | — | — |
| $\overline{INTA}$ | 23 | — | 10mA | −1mA |
| GND | 14 | | | |
| $V_{CC}$ | 28 | | | |

## STATUS WORD CHART

| | | TYPE OF MACHINE CYCLE | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Data Bus Bit | Status Information | Instruction Fetch | Memory Read | Memory Write | Stack Read | Stack Write | Input Read | Output Write | Interrupt Acknowledge | Halt Acknowledge | Interrupt Acknowledge While Halt | |
| | | ① | ② | ③ | ④ | ⑤ | ⑥ | ⑦ | ⑧ | ⑨ | ⑩ | Ⓝ STATUS WORD |
| $D_0$ | INTA | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | |
| $D_1$ | $\overline{WO}$ | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | |
| $D_2$ | STACK | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | |
| $D_3$ | HLTA | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | |
| $D_4$ | OUT | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | |
| $D_5$ | $M_1$ | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | |
| $D_6$ | INP | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | |
| $D_7$ | MEM R | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | |

CONTROL SIGNALS:
- $\overline{INTA}$
- (NONE)
- $\overline{INTA}$
- $\overline{I/O\ W}$
- $\overline{I/O\ R}$
- $\overline{MEM\ W}$
- $\overline{MEM\ R}$
- $\overline{MEM\ W}$
- $\overline{MEM\ R}$
- $\overline{MEM\ R}$

8

## LOADING RULES

| Signal | Pin No. | Input Load | Output Sink | Output Source |
|---|---|---|---|---|
| $D_0$ | 15 | 250µA | 2mA | −100µA |
| $D_1$ | 17 | 250µA | 2mA | −100µA |
| $D_2$ | 12 | 250µA | 2mA | −100µA |
| $D_3$ | 13 | 250µA | 2mA | −100µA |
| $D_4$ | 6 | 250µA | 2mA | −100µA |
| $D_5$ | 19 | 250µA | 2mA | −100µA |
| $D_6$ | 21 | 250µA | 2mA | −100µA |
| $D_7$ | 8 | 250µA | 2mA | −100µA |
| $DB_0$ | 13 | 250µA | 10mA | — |
| $DB_1$ | 16 | 250µA | 10mA | — |
| $DB_2$ | 11 | 250µA | 10mA | — |
| $DB_3$ | 9 | 250µA | 10mA | — |
| $DB_4$ | 5 | 250µA | 10mA | — |
| $DB_5$ | 18 | 250µA | 10mA | — |
| $DB_6$ | 20 | 250µA | 10mA | — |
| $DB_7$ | 7 | 250µA | 10mA | — |
| $STSTB$ | 1 | 500µA | — | — |
| $\overline{OBIN}$ | 4 | 250µA | — | — |
| $\overline{WR}$ | 3 | 250µA | — | — |
| HLDA | 2 | 250µA | — | — |
| $\overline{MEM\ R}$ | 24 | — | 10mA | — |
| $\overline{MEM\ W}$ | 26 | — | 10mA | — |
| $\overline{I/OR}$ | 25 | — | 10mA | — |
| $\overline{I/OW}$ | 27 | — | 10mA | — |
| $\overline{BUSEN}$ | 22 | 250µA | — | — |
| $\overline{INTA}$ | 23 | — | 10mA | — |
| GND | 14 | | | |
| $V_{CC}$ | 28 | | | |

## DEFINITION OF FUNCTIONAL TERMS

| | |
|---|---|
| $D_7$-$D_0$ | Data bus to-from Am8080A\8080A |
| $DB_7$-$DB_0$ | Data bus to-from user system |
| $\overline{I/OR}$ | Input/output read strobe output active LOW |
| $\overline{I/OW}$ | Input/output write strobe output active LOW |
| $\overline{MEM\ R}$ | Memory read strobe, output, active LOW |
| $\overline{MEM\ W}$ | Memory write strobe, output, active LOW |
| $\overline{OBIN}$ | Data bus input strobe, input active HIGH |
| $\overline{INTA}$ | Interrupt acknowledge strobe, input, active LOW |
| HLDA | Hold input from Am8080A\8080A active HIGH |
| $\overline{WR}$ | Write input strobe, active HIGH |
| $\overline{BUSEN}$ | BUS ENABLE INPUT, input, 3-state output control, active LOW for 3-state out |
| $\overline{STSTB}$ | Status Strobe, input, strobes status on data bus into status latch, active LOW |

## Metallization and Pad Layout



DIE SIZE 0.110" X 0.139"

## STATUS WORD CHART

| Data Bus Bit | Status Information | TYPE OF MACHINE CYCLE: Instruction Fetch | Memory Read | Memory Write | Stack Read | Stack Write | Input Read | Output Write | Interrupt Acknowledge | Halt Acknowledge | Interrupt Acknowledge While Halt | (W) STATUS WORD |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | (7) | (3) | (2) | (4) | (5) | (6) | (1) | (8) | (9) | (10) | |
| $D_0$ | INTA | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | |
| $D_1$ | $\overline{WO}$ | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | |
| $D_2$ | STACK | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | |
| $D_3$ | HLTA | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | |
| $D_4$ | OUT | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | |
| $D_5$ | $M_1$ | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | |
| $D_6$ | INP | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | |
| $D_7$ | MEM R | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | |

# Application Notes

## NUMERICAL INDEX


| | Page |
|---|---|
| Am9130/Am9140 | 9-1 |
| First-In First-Out Memories | 9-17 |
| Am9511 | 9-26 |
| Am9519 | 9-49 |

# Application Notes


NUMERICAL INDEX

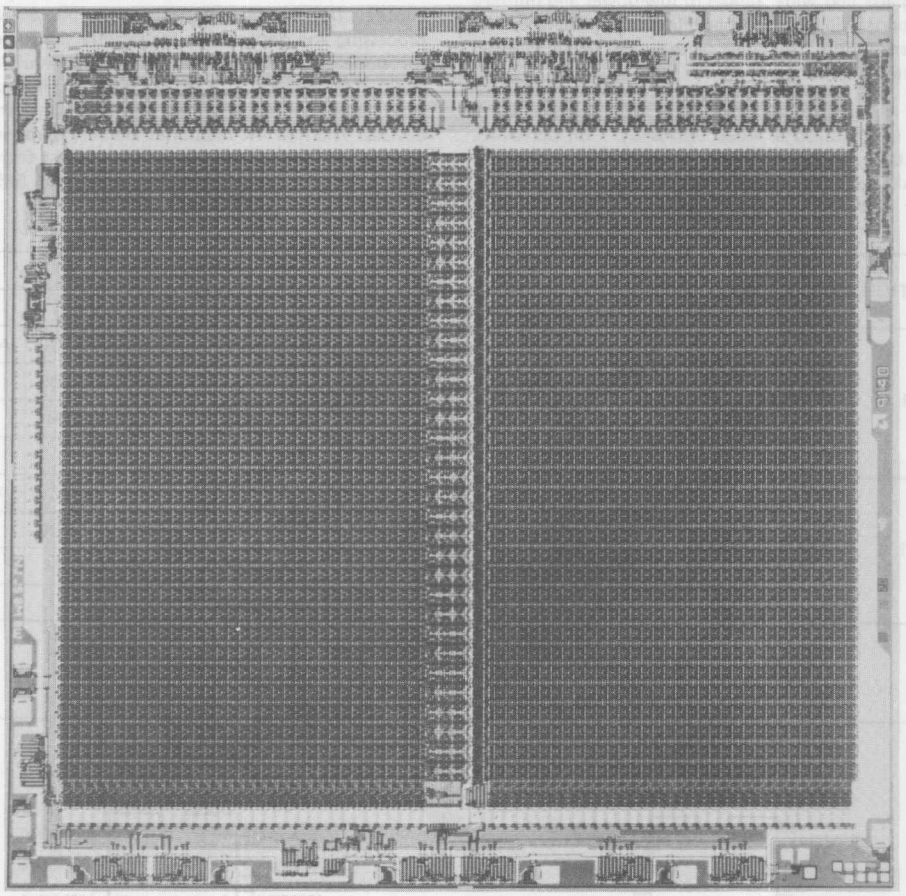
Page

Am9130/Am9140 ..... 9-1
First-In First-Out Memories ..... 9-17
Am9511 ..... 9-29
Am9519 ..... 9-49

# Am9130/Am9140

## DESIGNING WITH SELF-CLOCKING, ADAPTIVE 4K STATIC R/W RANDOM ACCESS MEMORIES

By Joseph H. Kroeger



9

### TABLE OF CONTENTS


GENERAL CHARACTERISTICS
- Introduction ... 9-2
- Design Philosophy ... 9-3
- Interface Considerations ... 9-3
- Power Supply ... 9-3

INTERFACE SIGNALS ... 9-4
- Signal Flow ... 9-4
- Chip Enable ... 9-4
- Address and Chip Select ... 9-5
- Write Enable ... 9-6
- Data In and Data Out ... 9-6
- Output Enable and Output Disable ... 9-7
- Memory Status ... 9-7

INTERNAL CIRCUITRY
- Address Register ... 9-7
- Address Decoding ... 9-8
- Memory Cell ... 9-8
- Bit and Data Lines ... 9-8
- Sense Amplifier ... 9-9
- Data I/O Stages ... 9-10
- Memory Status Circuit ... 9-10

SYSTEM DESIGNS
- Interface Timing ... 9-11
- Small Memory Arrays ... 9-12
- Memory Status Timing ... 9-13
- Memory Status Coordination ... 9-14
- Handshaking Control ... 9-15
- Interleaved Operation ... 9-15

## GENERAL CHARACTERISTICS

### Introduction

The Am9130 and Am9140 products from Advanced Micro Devices are 4K-bit, static, self-clocking, adaptive, read/write random access memories. Both types of devices use only a single +5 volt power supply, yet offer high speed performance and low power dissipations. Figure 1 lists the appropriate part numbers for the combinations of variables available at press time. As product enhancement proceeds, it is anticipated that higher speed parts and wider ranges of low-power and military temperature parts will be available. Plastic DIP packages will also become an option. The latest factory data sheets show all available variations of parts.

The Am9130 is organized as 1024 words by 4 bits per word; the Am9140 is organized as 4096 words by 1 bit per word. Parts are available in both commercial and military temperature ranges. Although the standard power parts offer quite low per-bit power dissipation, there is also a family of low-power parts available. As usual at AMD, all parts are 100% reliability assurance tested to the requirements of MIL-STD-883.

Figure 2 shows the pin assignments for the two memories. The package for both parts is a standard 22-pin dual in-line. Both memory configurations are manufactured from the same basic chip and use only specialized metal interconnect layers to define the structural differences. This approach allows several manufacturing efficiencies to be realized and permits each part to benefit from the combined volume of both parts.

The Am9130 and Am9140 memories are implemented with AMD's LINOX N-channel silicon gate MOS technology. The processing and design rules are exactly the same as those used for some time to produce the popular Am9102 line of 1K static R/W memories. LINOX features physically flat structures, triple ion-implantation, and low capacitance, high-speed devices. The new 4K memories are very dense with more than 27,500 active transistors in an area of less than 37,800 $mil^2$. The chip measures 192 x 197 mils with 58% of the area devoted to the 4096 storage cells.

| ORGANIZATION | AMBIENT TEMPERATURE | POWER | ACCESS TIME | | | |
|---|---|---|---|---|---|---|
| | | | 500ns | 400ns | 300ns | 200ns |
| 1024 x 4 | $0°C \leq T_A \leq 70°C$ | STANDARD | AM9130ADC | AM9130BDC | AM9130CDC | AM9130EDC |
| | | LOW | AM91L30ADC | AM91L30BDC | AM91L30CDC | |
| | $-55°C \leq T_A \leq 125°C$ | STANDARD | AM9130ADM | AM9130BDM | AM9130CDM | |
| | | LOW | AM91L30ADM | AM91L30BDM | | |
| 4096 x 1 | $0°C \leq T_A \leq 70°C$ | STANDARD | AM9140ADC | AM9140BDC | AM9140CDC | AM9140EDC |
| | | LOW | AM91L40ADC | AM91L40BDC | AM91L40CDC | |
| | $-55°C \leq T_A \leq +125°C$ | STANDARD | AM9140ADM | AM9140BDM | AM9140CDM | |
| | | LOW | AM91L40ADM | AM91L40BDM | | |

**Figure 1. Part Number Matrix.**

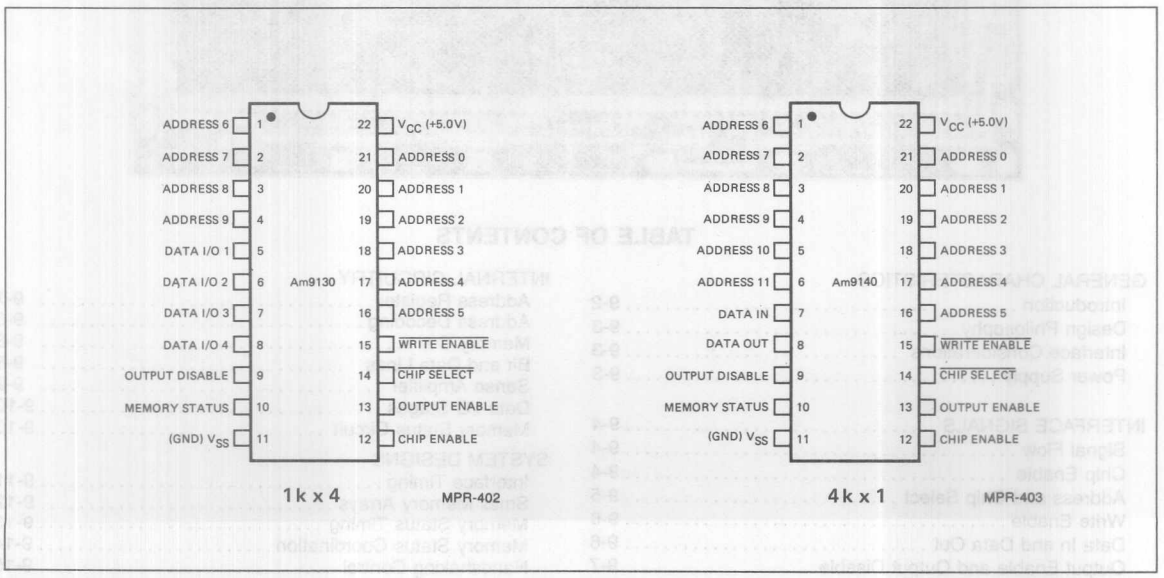



**Figure 2. Pin Assignments.**

## Design Philosophy

Read/write random access memories are customarily divided into two categories based on the storage mechanism used in the memory cells. **Dynamic** memories use dynamic cells that store information in the form of charge on small capacitors. **Static** memories use static cells that store information in the form of latched currents flowing through transistors. Dynamic memories must be periodically refreshed in order to maintain the stored information. Static memories maintain the stored data without refreshing as long as power is applied. (Both types are volatile — that is, stored information is lost when power is removed.)

The basic storage mechanisms of the cells contribute significantly to the characteristics of the overall memory, but an important contribution is also made by the access method used with a particular cell. Dynamic storage has conventionally been used with dynamic decoding and control circuitry. Similarly, static storage has traditionally used static support circuitry. But those associations are not necessary. Other combinations are possible and provide different overall specifications. One example is provided by Advanced Micro Devices' 4K dynamic memories, the Am9050 and Am9060. They use static circuitry on some input signals in order to significantly improve several timing characteristics. There also exist several types of read-only memories that use dynamic decoding for improved performance.

The Am9130 and Am9140 memories take advantage of a new combination that provides static storage together with a novel type of clocked access method. The storage cells use a conventional, fully static design. The decoding and sensing circuits use a clocked static approach that has no dynamic nodes. The clocked circuitry allows the addition of several new features, increases speed and decreases power dissipation relative to an analogous non-clocked design. At the same time, the usual disadvantages of a clock have been either eliminated or minimized in these new memories.

This philosophy, combined with Advanced N-channel MOS technology, has produced these new combinations of features, including:

- Fully static storage
- Fast access and cycle times
- Low operating power dissipation
- Self-clocking mode of operation
- Single phase, low voltage, low capacitance clock
- Static clock that may be stopped in either state
- Address register on-chip
- Output data register on-chip
- Single +5 volt power supply requirement
- Interface logic levels identical to TTL
- High output drive capability
- Nearly constant power drain; no large current surges
- DC standby mode for reduced power consumption
- Operation over full military temperature range

## Interface Considerations

In common with other AMD static R/W RAM's, all of the input and output signals for the Am9130 and Am9140 memories are specified with logic levels identical to those of standard TTL circuits. The worst-case input high and low levels are 2.0V and 0.8V, respectively; the worst-case output high and low levels are 2.4V and 0.4V, respectively. Thus, with TTL interfacing, the normal worst-case noise immunity of at least 400mV is maintained.

All inputs include protection networks designed to prevent damaging accumulations of static charge. During normal operation, the protection circuitry is inactive and may be modeled as a simple series RC. See Figure 3. The first functionally active connection for every input is the gate of an MOS transistor. No active sources or drains are connected to the inputs so that no transient or steady-state currents are impressed on the driving signals other than the simple charging or discharging of the input capacitance, plus the accumulated leakage associated with the protection network and the input gate. Input capacitances are usually around 5pF and leakage currents are usually less than 1$\mu$A.

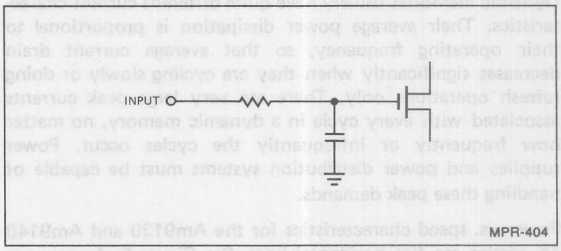



**Figure 3. Equivalent Input Circuit.**

The output buffers can source at least 200$\mu$A worst-case and can sink at least 3.2mA worst-case, while still maintaining TTL output logic levels. Thus, the memories can drive two standard TTL loads or nine standard Low-Power Schottky TTL loads. This unusually high output drive capability allows not only improved fan-out, but also better capacitive drive and noise immunity.

Delays in the output circuits show little variation with changes in the DC loads being driven. Changes with capacitive loading are shown by the curve in Figure 4. Access times are specified for a total load of one TTL gate plus 50pF of capacitance.

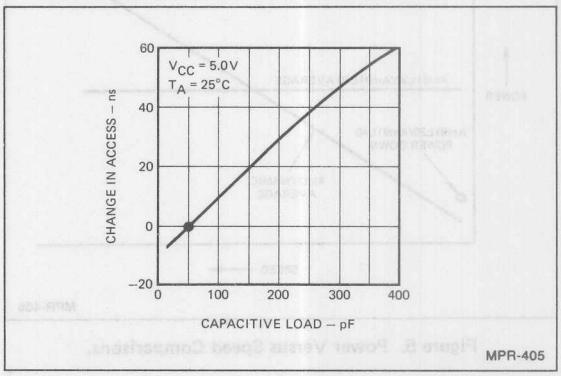



**Figure 4. Access Change Versus Load.**

## Power Supply

The Am9140 and Am9130 memories require only a single supply voltage. They perform their normal operations at a $V_{CC}$ of +5 volts. The commercial temperature range parts have a voltage tolerance of ±5%; the military temperature range tolerance is ±10%. The worst-case current drains are specified in the data sheets at the high side of the voltage tolerance and the low end of the temperature range. In addition, the current

9

specifications take into account the worst-case distribution of processing parameters that may be encountered during the manufacturing life of the product.

The current drain for these parts is relatively quite constant over their various operating cycles. Since the basic storage mechanism involves latched currents in each cell, there is a necessary cumulative current flowing at all times, even when the memory is not being actively accessed. The average currents specified are largely independent of the CE input state, or the condition of any of the input signals. At the falling edge of the CE clock, there is a brief current surge of an additional 4 to 8mA that occurs as the decoders are being preset.

Dynamic memories usually have quite different current characteristics. Their average power dissipation is proportional to their operating frequency, so that average current drain decreases significantly when they are cycling slowly or doing refresh operations only. There are very large peak currents associated with every cycle in a dynamic memory, no matter how frequently or infrequently the cycles occur. Power supplies and power distribution systems must be capable of handling these peak demands.

Power vs. speed characteristics for the Am9130 and Am9140 4K statics are flat horizontal lines. See Figure 5. A representative 4K dynamic has a rising line as shown. The dynamic dissipation becomes higher than the regular-power static parts out near the high end of the speed range. The cross-over occurs much earlier for the low-power statics.

The power-down mode is entered by simply bringing both CE and OE low and then ramping $V_{CC}$ down as low as 1.5V. Power dissipation will fall by more than 80%. Normal cycles may resume when $V_{CC}$ has been returned to its operating range. See specification sheets for further details.

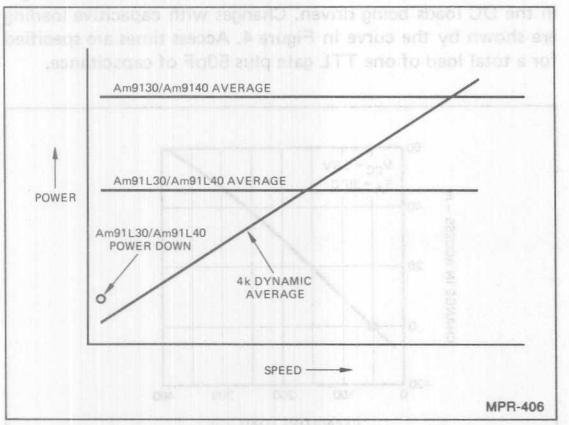



Figure 5. Power Versus Speed Comparisons.

## INTERFACE SIGNALS

### Signal Flow

Figure 6 is the block diagram for the Am9130 version and shows the interface connections along with the general signal flow. There are ten address lines (A0 through A9) that are used to specify one of 1024 locations, with each location containing four bits. The Chip Select signal acts as a high order address for multiple chip memory configurations. The Chip Enable clock latches the addresses into the address registers and controls the sequences of internal activities.

The row address signals (A0 through A5) and their inversions are distributed to the 64 row address decoders where one of the rows is selected. The 64 cells on the selected row are then connected to their respective bit line columns. Meanwhile, the column address signals (A6 through A9) have been decoded and used to select one of 16 columns for each of the four sense amplifiers. The end result is that one cell is connected to one sense amplifier.

During read operations, the sensed data is latched into the output register and is available for the balance of the operating cycle. During write operations, the write amplifier is turned on and drives the input data onto the sense lines, up the column bit lines and into the selected cells. Input and output data signals share common interface pins.

The output buffers use a three-state design that simplifies external interfacing. Unselected chips have the outputs turned off so that several chips may be wire-ored together easily. The Output Enable and Output Disable signals provide fully asynchronous controls for turning off the output buffers when desired.

Within the storage matrix, there is an extra row of simulated cells. This reference row is selected on every operating cycle in addition to the addressed row and provides internal timing signals that help control the data flow through the part. The Memory Status output signal is derived from the reference row and uses the same designs for its sense and buffer circuits as used by the data bits. Memory Status specifies when output data is available and simplifies generation of Chip Enable.

Figure 7 is the block diagram for the Am9140 version. The basic operation and signal flows are similar to the Am9130. There are two additional address lines (A10, A11), allowing selection of one of 4096 locations. Each location contains one bit so only one set of data I/O circuits are needed. Input and output data signals use separate interface pins.

### Chip Enable

The Chip Enable input is a control clock that coordinates all internal activities. All active memory functions are initiated when CE goes high. At the completion of the active operation, CE goes low to preset the memory for the next cycle. There are no restrictions on the maximum times that CE may remain in either state so the clock may be extended or stopped whenever convenient. After power-up and before beginning a valid operation, the clock should be brought low to initially preset the memory.

Figure 8 illustrates a basic operating cycle for either of the memories. The rising edge of CE begins each cycle and strobes the Address and Chip Select signals into the on-chip register. Internal timing signals are derived from CE and from transitions of the address latches and the reference cells. Various control functions are activated by these timing signals as the addresses and data flow through the memory.

When the actual access time of the part has been reached (or a write operation is complete), CE may be switched low if desired. The worst-case time as specified in the data sheet may be used to determine the access. Alternatively, the access or write complete time indicated by the rising edge of the Memory Status output signal may be used. (See the Memory Status section of this Note.) It is perfectly acceptable to leave the CE clock high following the access time; some system operating modes will find it convenient to do so. A Read/Modify/Write cycle, for example, will keep CE high after the access until the modify and write portions of the cycle are finished.

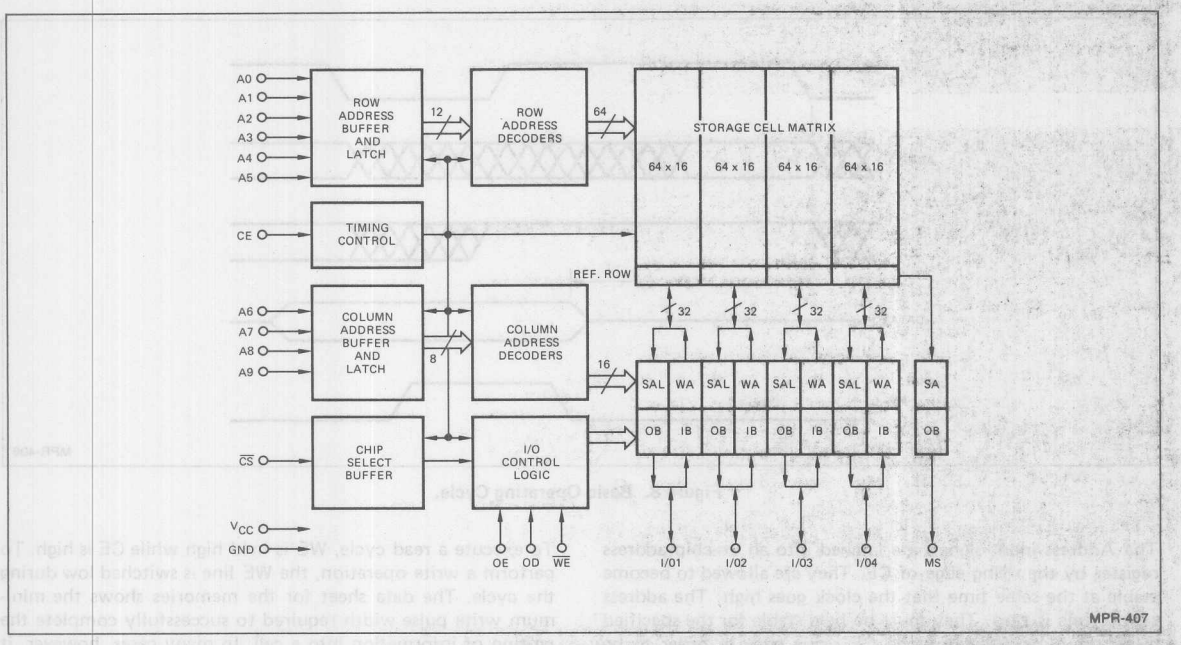



**Figure 6. Am9130 Block Diagram.**

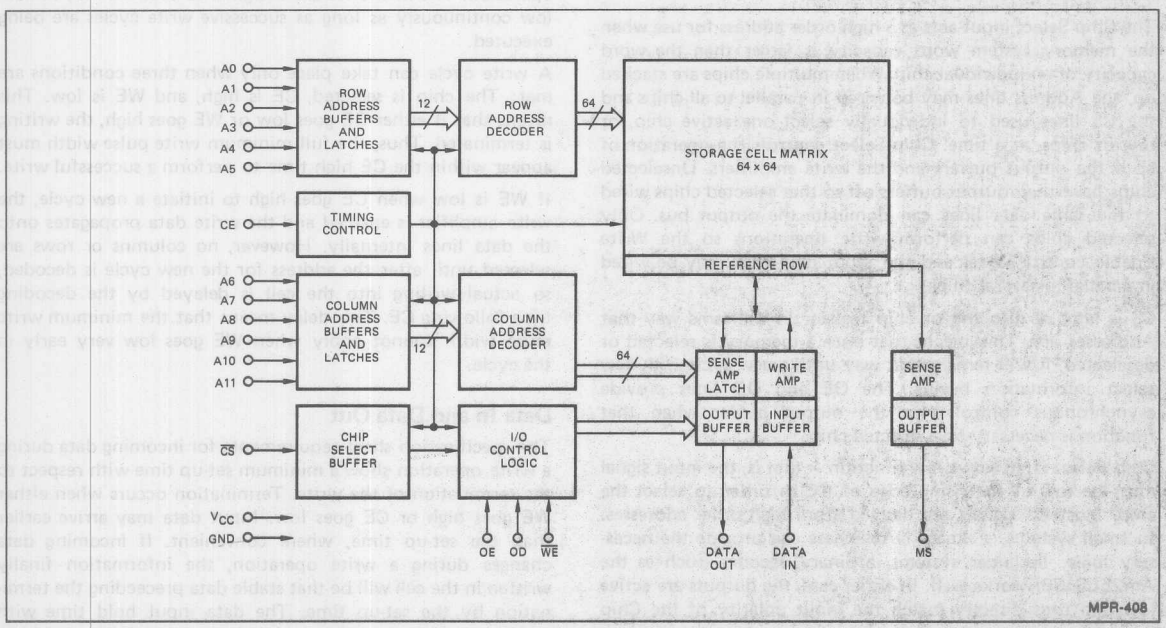



**Figure 7. Am9140 Block Diagram.**

When CE does go low, the internal preset operation begins. The memory is ready for a new cycle only after the preset is complete. The worst-case CE low time specified in the data sheet may be used to determine the preset interval. Alternatively, the actual preset time is indicated as complete as soon as Memory Status goes low. CE may remain low as long as desired.

## Address and Chip Select

The Address inputs are binary coded lines that specify the word location to be accessed within the memory. The Am9130 has 1024 word locations, any one of which may be selected by a ten-bit binary address ($2^{10}$ = 1024). The Am9140 has 4096 locations and so uses a 12-bit address ($2^{12}$ = 4096).

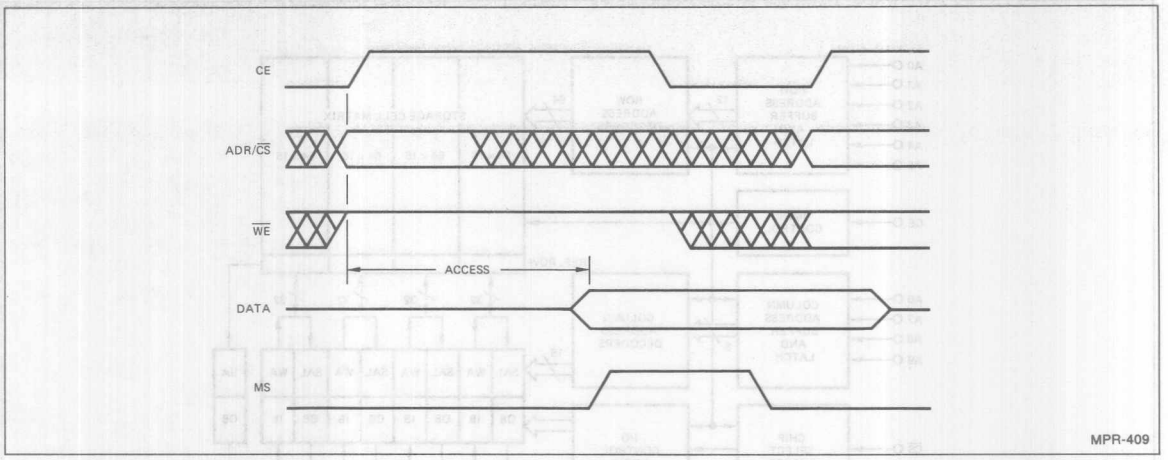



**Figure 8. Basic Operating Cycle.**

The Address input signals are latched into an on-chip address register by the rising edge of CE. They are allowed to become stable at the same time that the clock goes high: The address set-up time is zero. They must be held stable for the specified minimum time following the CE rising edge in order to be properly loaded into the register. Once the address hold time has been observed, the address inputs are ignored by the memory until the next cycle is initiated.

The Chip Select input acts as a high order address for use when the memory system word capacity is larger than the word capacity of an individual chip. When multiple chips are stacked up, the Address lines may be wired in parallel to all chips and the CS lines used to individually select one active chip, or row of chips, at a time. Chip Select controls the operation of both the output buffers and the write amplifiers. Unselected chips have their output buffers off so that selected chips wired to the same data lines can dominate the output bus. Only selected chips can perform write operations so the Write Enable control signal and the input data lines may be wired in parallel to several chips.

CS is latched into the on-chip register in the same way that Addresses are. This means that once a memory is selected or deselected, it will remain that way until a new cycle with new select information begins. The OE and OD lines provide asynchronous control over the output buffer when that function is necessary on a selected chip.

Chip Select is an active low function – that is, the input signal must be low at the rising edge of CE in order to select the chip. Most CS signals are derived from high order addresses. In small systems, a simple NAND gate can provide the necessary logic. In larger systems, a binary decoder (such as the Am25LS138) works well. In either case, the outputs are active low and thus directly match the input polarity of the Chip Select.

## Write Enable

The Write Enable line controls the read or write status of the devices. When the CE clock is low, the WE signal may be any *value without affecting the memory. This allows the line to be* indeterminant while the using system is deciding what the next cycle will be. WE does not affect the status of the output buffer.

To execute a read cycle, WE is held high while CE is high. To perform a write operation, the WE line is switched low during the cycle. The data sheet for the memories shows the minimum write pulse width required to successfully complete the writing of information into a cell. In many cases, however, it will be convenient to leave the WE line low during the whole cycle so that no intra-cycle timing is necessary for a write operation. The memories are designed so that WE may remain low continuously as long as successive write cycles are being executed.

A write cycle can take place only when three conditions are met: The chip is selected, CE is high, and WE is low. This means that if either CE goes low or WE goes high, the writing is terminated. Thus, the full minimum write pulse width must appear within the CE high time to perform a successful write.

If WE is low when CE goes high to initiate a new cycle, the write amplifier is enabled and the write data propagates onto the data lines internally. However, no columns or rows are selected until after the address for the new cycle is decoded, so actual writing into the cell is delayed by the decoding time following CE. This delay means that the minimum write pulse width cannot apply when WE goes low very early in the cycle.

## Data In and Data Out

The specification sheet requirements for incoming data during a write operation show a minimum set-up time with respect to the termination of the write. Termination occurs when either WE goes high or CE goes low. Input data may arrive earlier than the set-up time, where convenient. If incoming data changes during a write operation, the information finally written in the cell will be that stable data preceeding the termination by the set-up time. The data input hold time with respect to the termination of write is zero. If the Am9140 is used with the Data In and Data Out lines remaining separate, the input data may occupy the bus at all times, if desired. The valid written data is then determined by the timing of WE.

If the Am9140 is used with the Data In and Data Out tied together, or if the Am9130 is used, care should be taken to avoid conflict between incoming and outgoing data on the shared lines. It is important to note that when WE is low, it does **not** turn off the output buffers; the potential conflict must be resolved in other ways. One convenient method is

to tie the Output Enable line to the WE line. Then, whenever WE goes low to write, it also turns off the output buffer. After a delay long enough for the output to reach its high impedance state, the input data can be introduced without conflict. The time that WE is low should be long enough to cover the output turn-off delay as well as the input data set-up time.

Since the data being written during a write cycle is impressed on the sense amplifier inputs, the output data will be the same as the input once the write is established. The conflicts occur with old output data that remains from a previous cycle or with new data that may be accessed before the write is established. If the write (and the associated input data) can be initiated while the output buffers are turned off, the conflict is eliminated; even if the outputs turn on, the output data will match the input data.

During a read cycle, once all of the addressing is complete and the cell information has propagated through the sense amplifier, it enters an output data register. The read information can also flow through to the output if the buffer is enabled. As long as CE is high, the addressing remains valid and the output data will be stable. When CE goes low to begin the internal preset operation, the output information is latched into the data register. It will remain latched and stable as long as CE is low.

At the start of every cycle when CE goes high, the output data latch is cleared in preparation for new information to come from the sense amplifier, and the output buffer is turned off. This is done so that in multiple chip systems with the outputs bussed together, old data from one chip will not interfere with new data being accessed on another.

### Output Enable and Output Disable

The OE and OD control lines perform the same internal function except that one is inverted from the other. If either OE is low or OD is high, the output buffer will turn off. If the CS input is latched low and OE is high and OD is low, then the output buffer can turn on when data is available.

OE and OD are designed to provide asynchronous control of the output buffer independent of the Chip Select control. This capability makes it easy to tie together the Data In and Data Out lines on the Am9140 where bussed operation is desired, and simplifies operation of the Am9130 which has the Data I/O signals internally tied.

OD and OE will often be used to resolve contention on data busses, but there are other convenient uses as well. The nature of these memories is such that it is easy to individually clock each row in a memory system and to achieve an interleaved mode of operation that effectively shortens the average cycle time. In such designs, the output buffers must be controlled to prevent overlap of read information from two rows that are tied together but clocked at different times.

### Memory Status

Memory Status is a new, unique output signal that offers several important features for the memory system designer. It indicates when data is valid at the outputs, when CE may be brought low, and when preset is complete so that a new cycle may begin. The Memory Status signal may be completely ignored without affecting the operation of the memory. On the other hand, it has several implications that make it a potentially interesting and useful signal.

A major function of the MS concept is to indicate actual performance of the memory rather than worst-case performance. Thus, the access time indicated by Memory Status will always be better than the worst-case specification as long as the conditions and assumptions on which the worst-case numbers are predicated are better. Further, real operating results change with changing conditions and Memory Status follows those changes. Thus, for example, as temperature decreases, access time also decreases and MS tracks the change in access exactly.

There are many different ways to use the Memory Status signal and several are illustrated in this Note. Basically it offers improved performance and self-timed operation, along with other related implications.

## INTERNAL CIRCUITRY

### Address Register

The circuitry for the address register is shown in Figure 9. Inverters K and L isolate the register from the input pin and convert the TTL input levels to the wider logic swings used internally. M inverts the address so that both A and $\overline{A}$ propagate to the inputs of the register.

Transistors 1, 3 5, and 7 are depletion devices. Transistor pairs 1, 2 and 3, 4 form two inverters that are cross-coupled to provide the basic latch. Transistor pairs 5, 6 and 7, 8 are used to enter information into the latch. If point A goes high, then 5 and 6 turn on and 7 and 8 turn off, forcing the latch to one polarity. Notice that the circuit would work without transistors 5 or 7. They are added to minimize the propagation delay through the register.

When transistors 9 and 10 are turned on, 5, 6, 7 and 8 are turned off and the latch is isolated from the input signal. When transistors 11 and 12 are turned on, the outputs from the register are held low and the following address decoders are in their preset state.

The timing for the address register operation is shown in Figure 10. $\phi$B and $\phi$C are simply delayed inversions of CE. $\phi$A is derived from the outputs of the slowest bit position in the address register. During the preset state of the memory when the CE clock is low, both $\phi$B and $\phi$C are high and $\phi$A is low. In that condition, transistors 9, 10, 11 and 12 are all turned on and no signals can travel into or out of the register.

When CE goes high to start a cycle, $\phi$B goes low after a brief delay. This turns off 9 and 10 and opens a window that allows the address information at the input to proceed into the latch. The path that generates $\phi$B is slightly longer than the path that the address follows to the register. This is done so that the address setup time relative to CE can be specified as zero.

Next, $\phi$C also goes low, permitting the latch to set and the register outputs to travel on to the decoders. The delay from $\phi$B to $\phi$C prevents any address spiking from disturbing the decoding circuits.

During the preset time, both X5 and $\overline{X5}$ are held low, keeping $\phi$A low. After the active cycle starts, either X5 or $\overline{X5}$ will make a transition high, depending on the state of the Address 5 input. Thus, $\phi$A will go high in every memory cycle. When it does, transistors 9 and 10 will turn on again, closing the window into the latch. This prevents any changes in external address information from affecting the stored address. Notice that $\phi$A is dependent on the presence of address information and only occurs after the address has reached the register outputs.

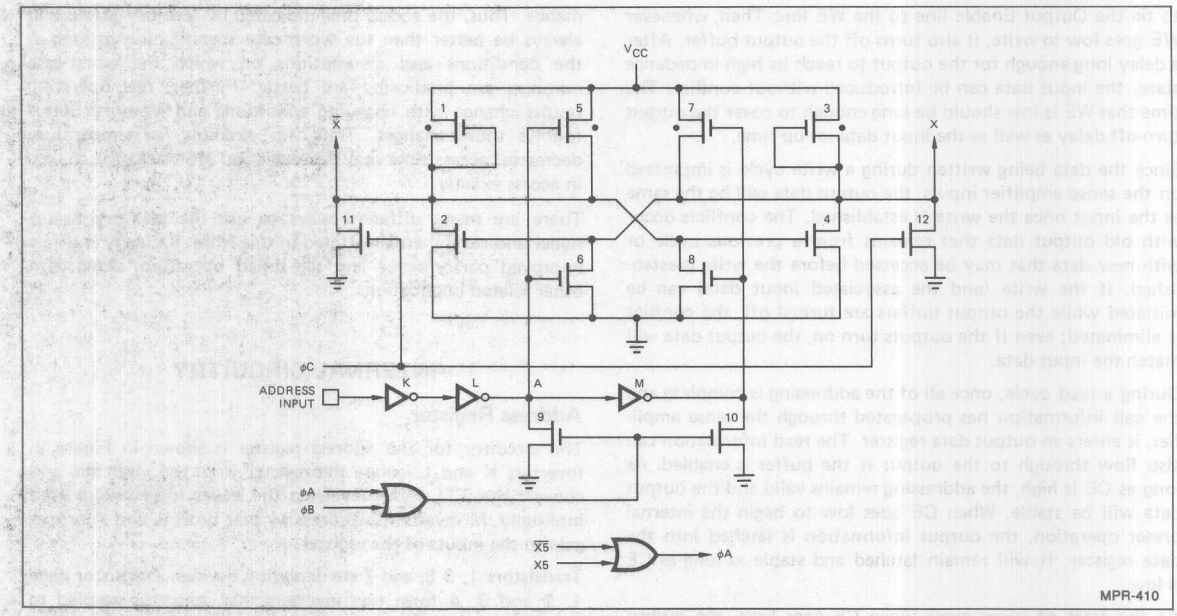



**Figure 9. Input Latch Circuit.**

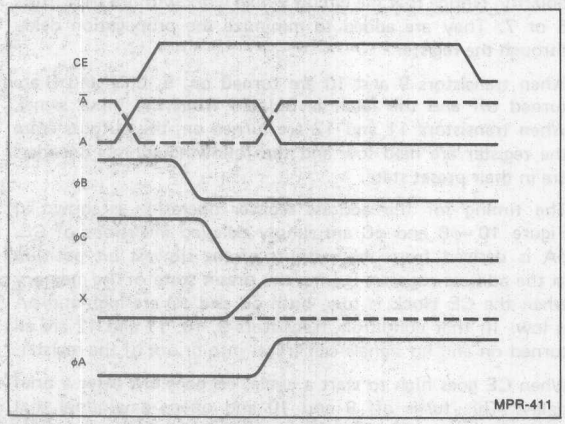



**Figure 10. Input Latch Timing.**

## Address Decoding

There are 64 of the row decoder circuits shown in Figure 11. The decoding is done by a simple six-input gate that is selectively wired to the outputs from the six low order bits of the address register. Each has a unique combination of X and $\overline{X}$ signals on its inputs ($2^6 = 64$). Only one decoder will have all of its inputs low during the decoding. The other 63 gates have at least one input high, thus keeping the decoder output low and the row driver, T, off. The single selected gate allows its row driver to turn on.

ϕA, which is derived from the transitions of the X5 signals, is buffered and used as ϕDEC, the decoder clock. When ϕDEC goes high, it passes through the selected row driver and brings the associated row select line high. All the other row select lines remain low. During the preset time when CE is low, all of the decoders have all of their inputs held low by ϕC, thus enabling all of the row drivers. To keep all the rows unselected, ϕDEC is low during the preset time and keeps all the select lines low.

There is a simple latch connected to each of the 64 select lines. It holds its select line low and prevents it from floating when the row driver is turned off. An active (high) row select line flips and holds the latch in addition to driving the 64 cells in the row.

## Memory Cell

The storage cells that are the heart of the memories use a conventional static design with six transistors. See Figure 12. Transistor pairs 1, 5 and 2, 6 are connected as simple inverters that are cross-coupled to form a bistable latch. Either transistor 1 or 2 is turned on and defines the data state of the cell. Transistors 5 and 6 are depletion-mode devices that act as pull-ups and maintain the state of the latch as long as power is applied.

The access devices permit the cell to be attached to its bit lines. When the cell's row select line is low, 3 and 4 are off and the cell is isolated from all other circuitry. When the select line is high, 3 and 4 are on and the cell is connected to the bit lines. If a read operation is in progress, the cell then pulls one of the bit lines low. If a write operation is being performed, the bit lines are driven by the data to be written and the cell is forced into the desired state.

## Bit and Data Lines

Figure 13 shows the bit line column and data line organization. A total of 64 cells — one from each row — are connected to one bit line pair to form a column of cells. Columns are connected in parallel through the column select transistors to form the data lines. The data lines feed into a sense amplifier or are fed from the write amplifier. For the Am9140, all 64 columns are connected to one pair of data lines and one set

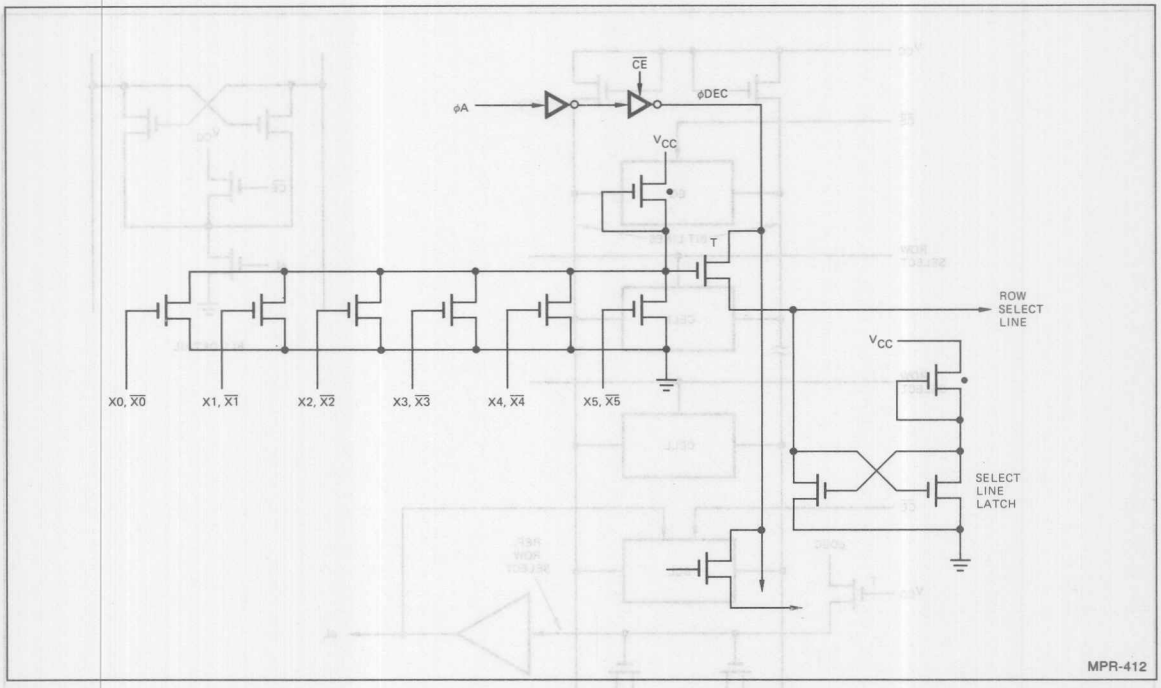



**Figure 11. Row Decoder Circuit.**

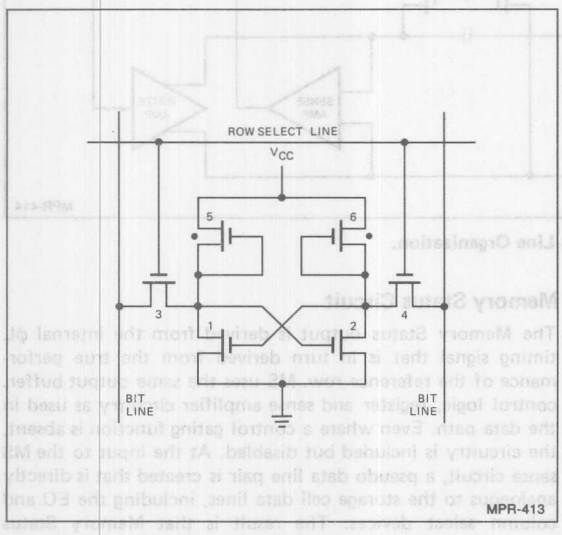



**Figure 12. Cell Circuit.**

of I/O circuits. For the Am9130, there are four pairs of data lines with four sets of I/O circuits and 16 columns are connected to each pair of data lines.

In addition to the storage cells, each column contains the reference row transistors and two other circuits labeled in the figure as EQ and BLL. The EQ circuit is active only during the preset time when CE is low. It is used to balance and equalize the bit lines and bring them to a voltage level somewhat below $V_{CC}$. The same EQ circuit is also used with the data lines.

The BLL circuit is a Bit Line Latch that is inactive during preset and is used during the active portion of the cycle to help the selected cell discharge the capacitive load presented by the bit and data lines. It is controlled by $\phi$L, a timing signal derived from the reference row.

The row driver, T, for the reference row is always enabled and the reference row is therefore selected by $\phi$DEC on every cycle. The two reference transistors in each column are the same as the access devices in each cell that are driven by the other row select lines. When the reference row select signal has propagated all the way to the end of the row, it is buffered and used to generate $\phi$L. When $\phi$L is true, the BLL is enabled and follows the state of the bit lines as set by the selected cell in that column.

The column decoders work much the same way as the row decoders, except that they are not turned on and off by a decode clock. During an active cycle, only one column is connected to one pair of data lines.

## Sense Amplifier

A unique feedback amplifier detects the state of the data lines to provide read data for the output. The circuit in Figure 14 shows a simple differential amplifier (transistors 2, 3, 4, 5) with a pedestal voltage established by transistor 1. The output from the differential stage is fed back to influence the pedestal via transistors 6, 7 and 8. Notice that differential signals are balanced out and eliminated from the feedback loop. But supply voltage, temperature and process variations cause common mode shifts that are compensated for.

The output of the differential stage also goes to a latch circuit that squares and buffers the amplified signal. The latch simply follows the data that flows into it and feeds information to the output data register.

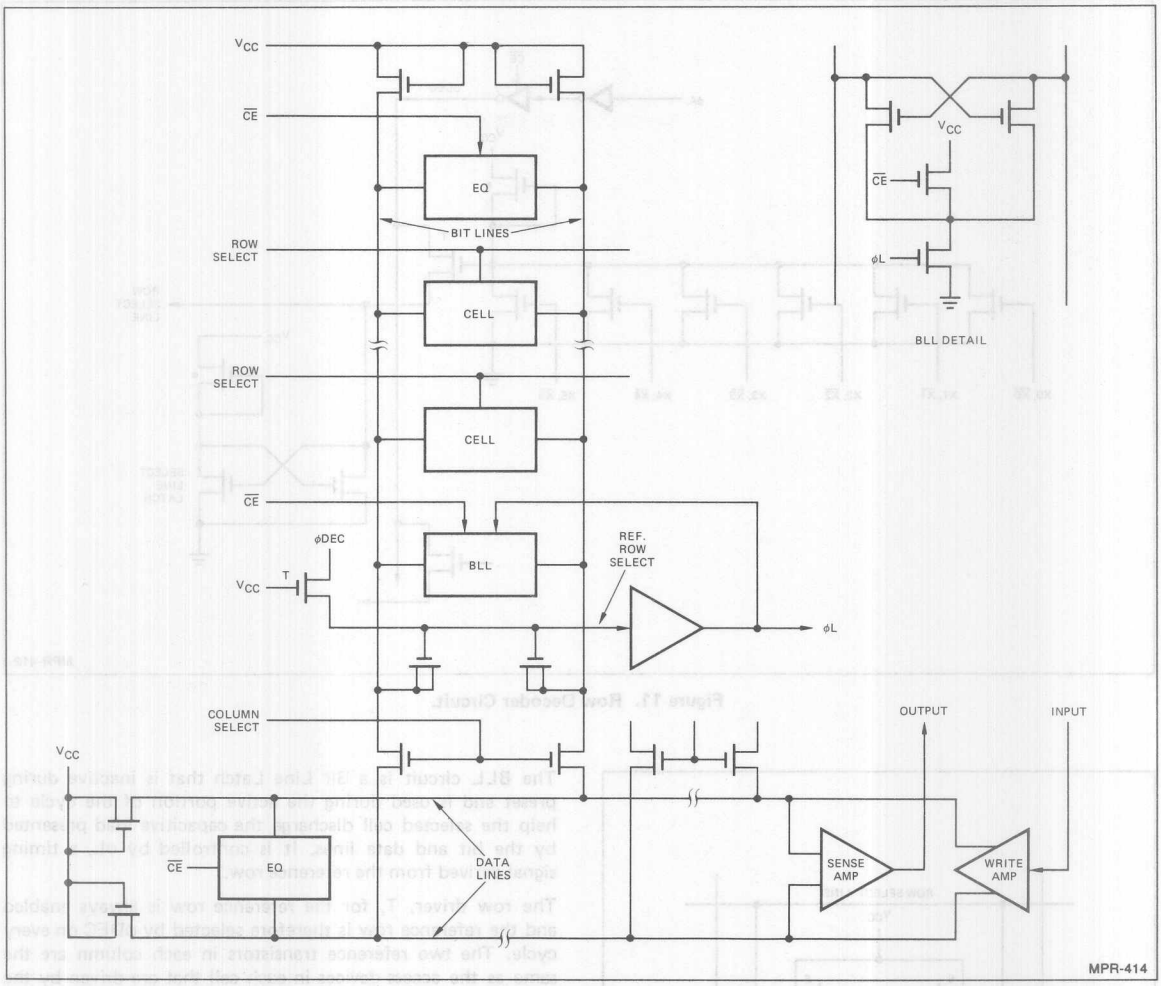



**Figure 13. Bit and Data Line Organization.**

## Data I/O Stages

The output stage shown in Figure 15 includes the output data register plus the output control logic plus the output buffer. Information from the sense amplifier can flow into and through the register and on to the output pin at the access time. As long as the CE clock is high, the cell addressing will be valid and the sense amplifier and output can remain stable. When CE goes low, the register inputs are isolated from the sensed data and the output can stay valid until CE next goes high.

There are several signals that can turn off the output buffer. Only when they are all simultaneously in the necessary state will the output turn on. When CE goes high, the output will turn off until the access time arrives as indicated by $\phi$L. When $\overline{CS}$ is latched high, the output will be off. When OE is low the outputs will be off. When OD is high the outputs will be off.

The write amplifier control logic only allows a write to take place on a selected chip with the CE high and the Write Enable low. Note that the WE line does not affect the output buffer. On the Am9130, the data input and output signals are tied together and share common interface pins.

## Memory Status Circuit

The Memory Status output is derived from the internal $\phi$L timing signal that is in turn derived from the true performance of the reference row. MS uses the same output buffer, control logic, register and sense amplifier circuitry as used in the data path. Even where a control gating function is absent, the circuitry is included but disabled. At the input to the MS sense circuit, a pseudo data line pair is created that is directly analogous to the storage cell data lines, including the EQ and column select devices. The result is that Memory Status tracks the output data very closely under all operating conditions.

Since the final output circuits are the same for both MS and Data, they respond identically to variations in loading. If the data output is heavily loaded, then similar equivalent loading should be used on the Memory Status output in order to maintain their responses relative to each other.

The MS output is always enabled and never enters a three-state off mode. Even on an unselected chip, the MS signal continues to reflect the status of the memory.

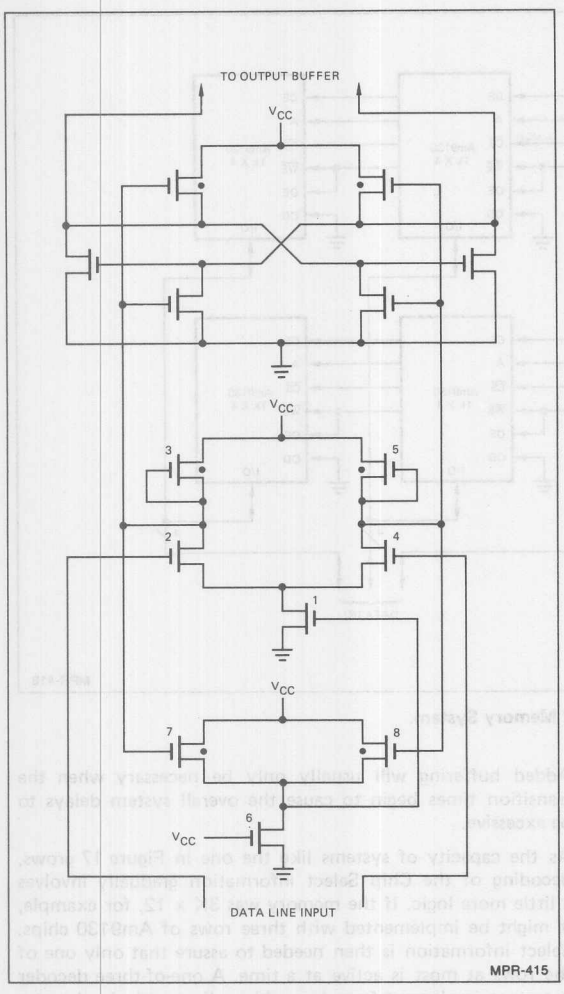



Figure 14. Sense Amplifier Circuit.

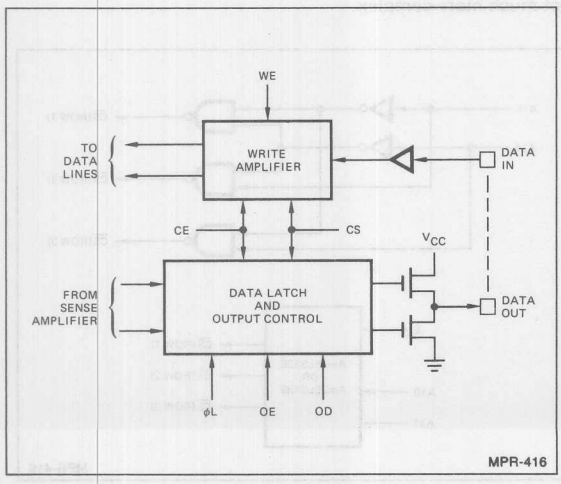



Figure 15. Data I/O Stages.

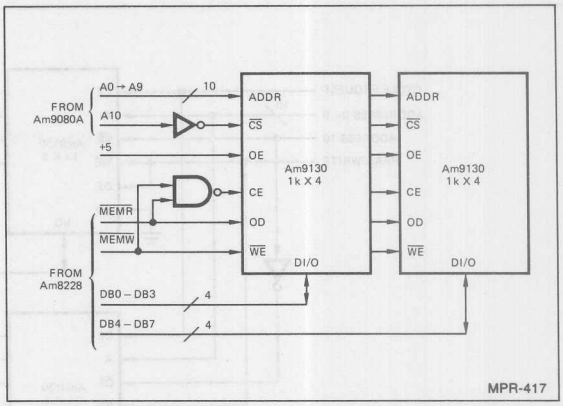



Figure 16. 1k x 8 R/W Memory for Am9080A.

## SYSTEM DESIGNS

### Interface Timing

The specification sheets for the Am9130 and Am9140 show the various input requirements and output responses for the memories. In each case, the parameters shown are worst-case in order to fully describe the operational limits of the parts. But many system situations allow the timings to be greatly simplified. For example, in small memories that are only one chip deep, the Chip Select signal may not be required and $\overline{CS}$ may be tied low. Similarly, in many instances OD may be tied low or OE may be tied high or both.

In some circumstances, it may be quite convenient to leave the addresses stable longer than the parts require. The falling edge of CE might be used by the associated system to initiate the derivation of a new address and the decision about reading or writing the next cycle. Those signals can then stay stable until the following decision time.

It will quite often be easy to leave the Write Enable line low during all of the CE high time of a write cycle. This eliminates some intra-cycle timing of the write pulse. The WE line may be any value as long as CE is low. Similarly, it will also be easy to have the Data In information available during the time that WE is low – indeed, WE will often be useful as the control line for gating the incoming data on and off.

Many times CE can be easily and directly derived from other signals in the using system. Figure 16 shows an example of a small memory for a microprocessor. Two Am9130 parts form a 1K x 8 memory for an Am9080A. The processor supplies the Addresses and the chip select signals. The Am8228 System Controller associated with the processor supplies the $\overline{MEMR}$ and $\overline{MEMW}$ control lines as well as a buffered data bus. A10 is inverted and used for the Chip Select signal, placing the addressing range in the second 1K of system memory. For larger systems or different configurations, other select logic may be required.

The Controller can request a Memory Read or a Memory Write operation. The NAND gate shown generates a CE when either request is made. When $\overline{MEMR}$ is high, the output buffers are turned off via the OD control. When $\overline{MEMR}$ is true the memory output will be connected to the data bus. When $\overline{MEMW}$ is low, a write operation is performed at the specified address. There is always sufficient time between operation requests for the memory to be fully preset.

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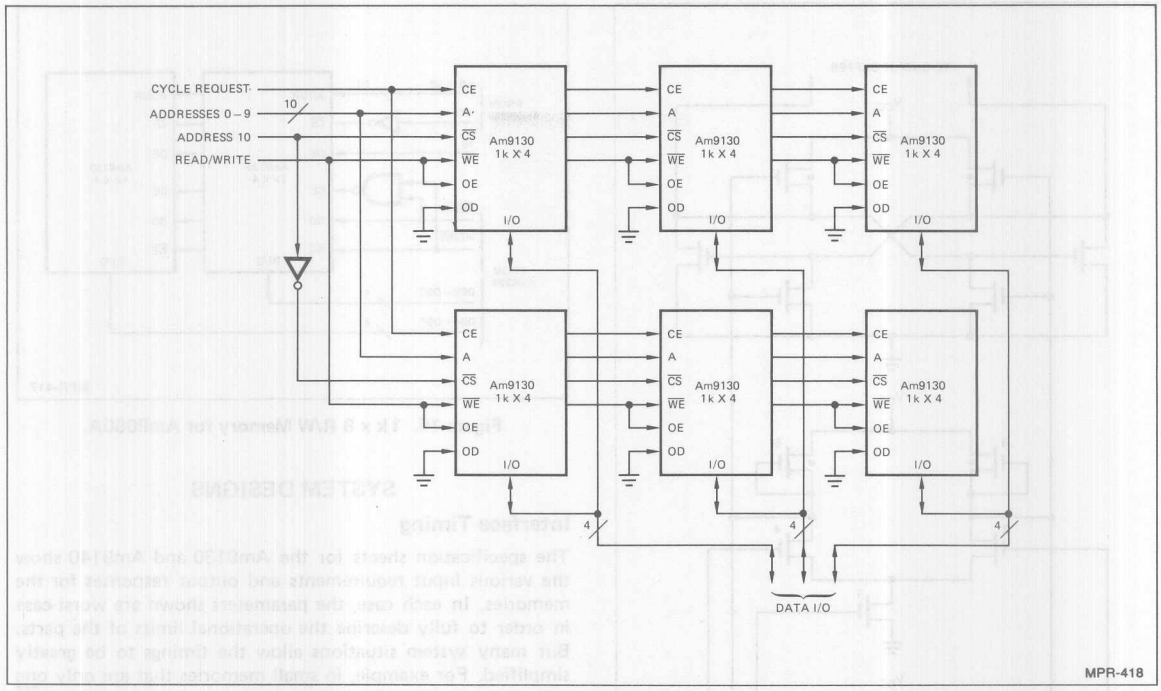



Figure 17. 2k x 12 Memory System.

## Small Memory Arrays

As an illustration of a conventional approach for operating multiple chips, Figure 17 shows a convenient way to connect six Am9130 chips to make a 2K x 12 memory. The Chip Enable clock is wired in parallel to all six chips, as are the ten Address lines and the R/W control line. Output Disable is tied to ground, allowing Output Enable to provide asynchronous external control of the output buffer status. OE is tied to Write Enable so that the R/W line turns off the output buffers when it goes low during a write cycle.

Address 10 and its inversion are used to select one of the two rows of chips for each operating cycle. As long as A10 is low, the upper row will respond to the clock and will communicate on the data bus while the lower row is deselected and can neither read nor write. When A10 is high the row roles are reversed.

The Data I/O lines have corresponding bits tied together in vertical columns. The control logic is arranged so that only one of the output buffers at a time will drive an I/O line, and only one chip at a time will write from an I/O line.

The type of memory illustrated is easily expanded to many different capacities. An 8K x 16, for example, could be implemented with 32 Am9140 chips (16 in each row), using the same control line configuration, plus two more address lines.

Driving and buffering limitations for both the inputs and the outputs will be dictated by a) accumulated leakage currents and b) accumulated capacitance. On an address line, for example, many chips may be driven in parallel from a standard TTL output. As the number of chips goes up, the leakage currents in the MOS memory gradually become a significant load for the TTL output especially in the high logic level state. Similarly, many parallel inputs will present a capacitive load that will degrade the rise and fall characteristics of the signal. Added buffering will usually only be necessary when the transition times begin to cause the overall system delays to be excessive.

As the capacity of systems like the one in Figure 17 grows, decoding of the Chip Select information gradually involves a little more logic. If the memory was 3K x 12, for example, it might be implemented with three rows of Am9130 chips. Select information is then needed to assure that only one of the rows at most is active at a time. A one-of-three decoder is easy to implement from two address lines with simple gates as shown in Figure 18. As the number of rows to be selected grows, however, both the wiring and the gate count tend to get much more complex.

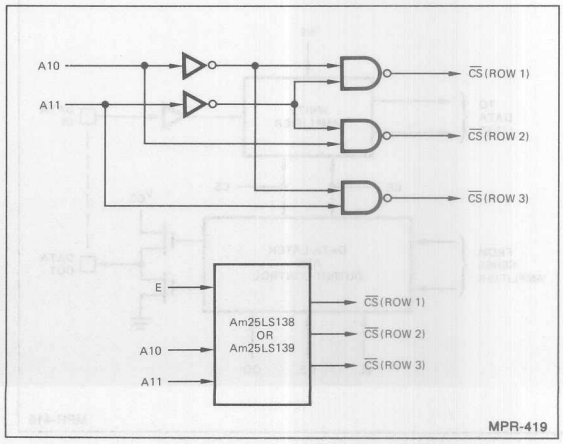



Figure 18. Chip Select Decoding.

Another approach (also shown in the Figure 18) takes advantage of MSI binary decoders like the Am25LS138 or Am25LS139. Both offer package count advantages, especially as the system gets bigger, and control logic is included that permits deselection of all rows. This can be handy for power-down situations and some other circumstances. Notice that the output polarity is such that the decoders interface directly with the memory chips.

The Am9140 can be converted to a common I/O instead of a separate I/O device simply by wiring together the Data In and the Data Out lines. When that is done, the same precautions suggested for the Am9130 concerning bus contention should be observed. Conversion of the Am9130 from common to separate I/O is only slightly more complex. The Am2915 (or Am2905) is a quad three-state bus transceiver. When connected as illustrated in Figure 19, it serves to create the bus needed by the Am9130 from separate input and output data. It even includes convenient registers on both sides. For a circuit without the registers and other control features of the Am2915, try the Am8T26. Both are four bits wide and so match up nicely with a column of Am9130 chips operating in parallel.

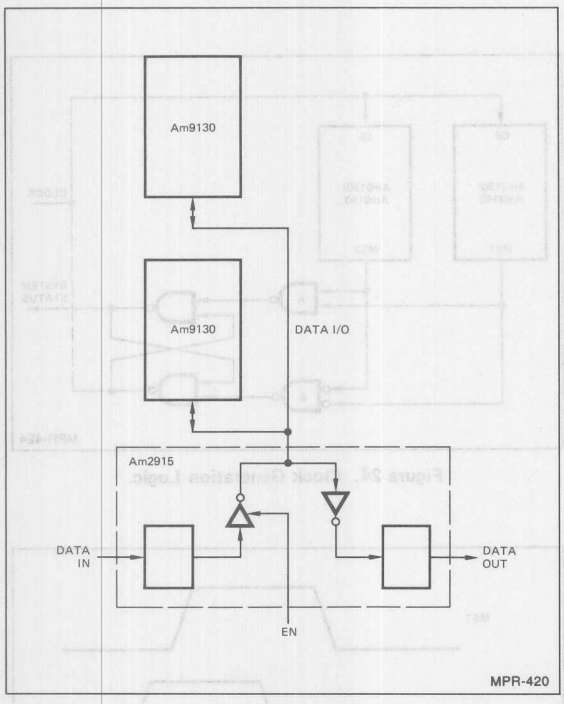



Figure 19.

## Memory Status Timing

Figure 20 shows the timing information conveyed by the MS output. The rising edge indicates that output data is valid and makes a convenient strobe for output to the rest of the system. See Figure 20a. When several chips are being used in parallel, the Memory Status signal from the slowest chip should be the strobe in order to assure that all the data bits are available and valid. There is a brief nominal delay from the worst-case output data to the rising edge of MS. That time is always greater then zero under similar loading conditions for the two signals.

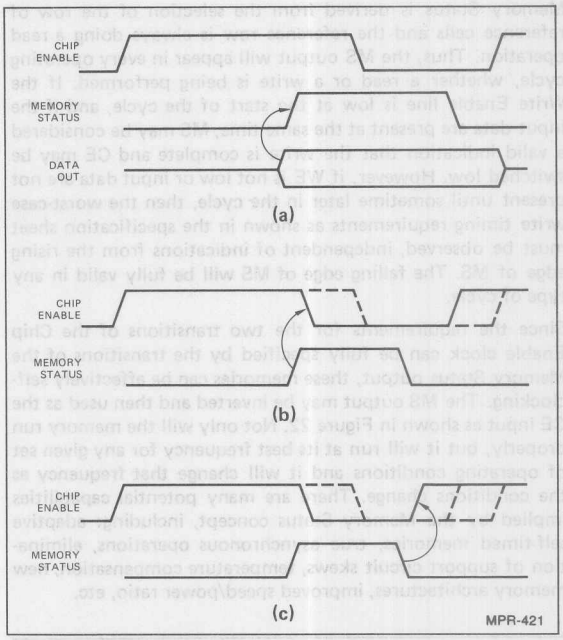



Figure 20. Memory Status Information.

The front edge of MS also specifies the end of the time that CE must be held high for that operation. See Figure 20b. Though CE may be high as long as desired, it may safely go low any time after MS goes high. MS will stay high until the internal preset operation is complete. Thus, it will not go low until some time after CE goes low and the total time that MS is high depends not only on the actual operating conditions of the memory, but also the delay from MS high to CE low.

The falling edge of MS specifies that the memory is ready for a new operation to be initiated. See Figure 20c. When several chips are operated in parallel, the latest falling edge will indicate the earliest time that their CE should go high. The chip with the longest access time will also be the chip with the longest preset time. The picture in Figure 21 shows an MS waveform during a simple read cycle.

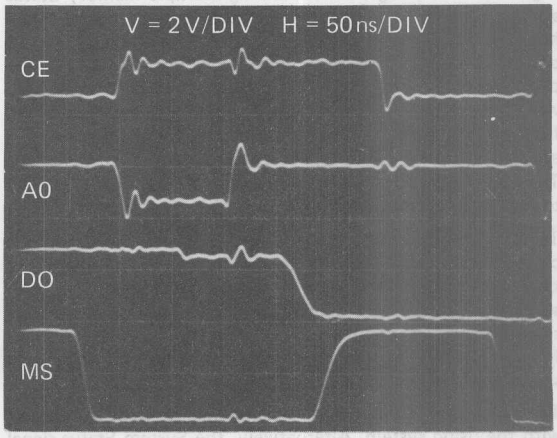



Figure 21. Read Cycle Waveforms.

9

Memory Status is derived from the selection of the row of reference cells and the reference row is always doing a read operation. Thus, the MS output will appear in every operating cycle, whether a read or a write is being performed. If the Write Enable line is low at the start of the cycle, and if the input data are present at the same time, MS may be considered a valid indication that the write is complete and CE may be switched low. However, if WE is not low or input data are not present until sometime later in the cycle, then the worst-case write timing requirements as shown in the specification sheet must be observed, independent of indications from the rising edge of MS. The falling edge of MS will be fully valid in any type of cycle.

Since the requirements for the two transitions of the Chip Enable clock can be fully specified by the transitions of the Memory Status output, these memories can be effectively self-clocking. The MS output may be inverted and then used as the CE input as shown in Figure 22. Not only will the memory run properly, but it will run at its best frequency for any given set of operating conditions and it will change that frequency as the conditions change. There are many potential capabilities implied by the Memory Status concept, including: adaptive self-timed memories, true asynchronous operations, elimination of support circuit skews, temperature compensation, new memory architectures, improved speed/power ratio, etc.

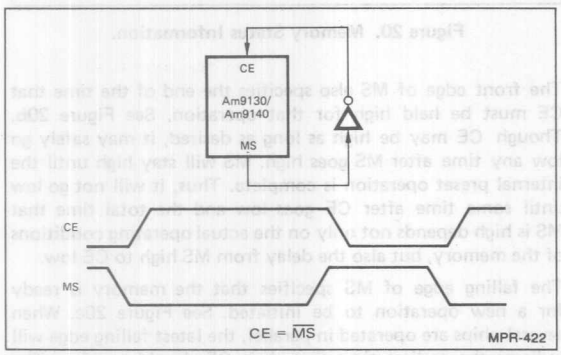



Figure 22. The Self-Clocking Memory.

## Memory Status Coordination

Figure 23 shows logic for combining multiple Memory Status signals. Gate A is used to detect when **both** MS outputs are high indicating that output data is available. Similarly, gate B detects that **both** MS outputs are low, indicating that the preset period is complete for both chips. The system associated with the memory can use this information to coordinate the flow and the generation of the CE clock. Essentially, this logic allows the slowest chip to govern the overall memory speed. The inputs to the coordinating logic can of course be expanded to handle as many chips as desired.

To combine these two pieces of status information, a simple cross-coupled latch can be added as shown in Figure 24. Since there are times when neither condition is true, the latch serves to maintain the previous status indication until a new state is valid. The result is a System Status signal that specifies for the system the same information that each MS signal specifies for an individual chip.

The clock may be derived independently for synchronization with the using system. Alternatively, the System Status signal may be inverted and used for the CE clock as indicated by the dotted line. The timing for this arrangement is shown in Figure 25. The memory will free-run at its best speed and the System Status will provide a synchronizing signal for use by the rest of the system.

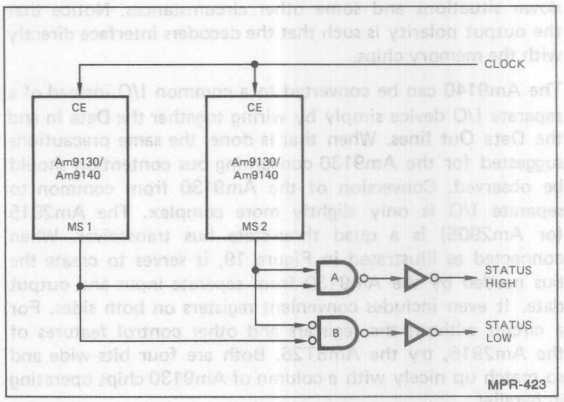



Figure 23. Status Coordination Logic.

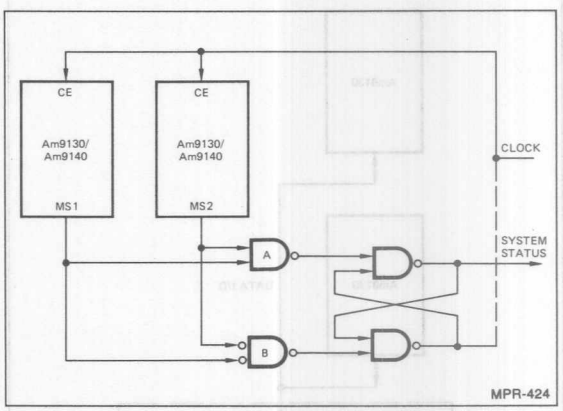



Figure 24. Clock Generation Logic.

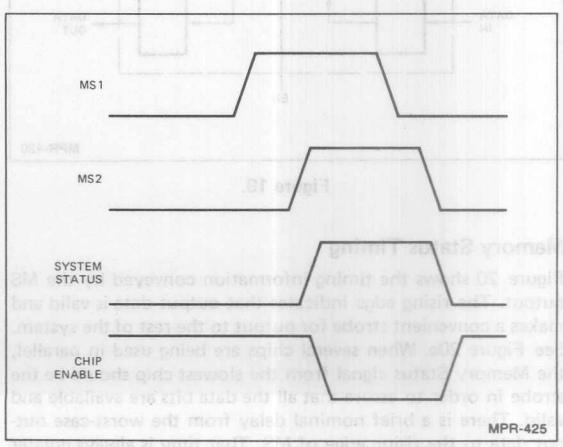



Figure 25. Status Timing.

## Handshaking Control

For systems that cannot be memory-driven, some means of controlling the clocking is needed. To permit the memory to single-step, a gate can be inserted in the dotted line of Figure 24 with a control line to turn the clock on or off. A more versatile and more asynchronous approach is illustrated in Figure 26. An additional latch is added to generate the clock so that the status information is derived independent of the clock control.

When the Cycle Request input is low, the memory will preset and prepare for an active cycle. When all is ready, Status Acknowledge will go low. When CR goes high, the memory will execute a cycle and will acknowledge conditions of access by bringing SA high. CR and SA then form a simple asynchronous handshaking pair for memory control. Notice that CR may go high at any time to start a cycle. If the chips are ready (SA low), the clock will proceed, but if preset is not complete (SA high) the memory will wait before initiating the requested cycle.

The timing for CR is quite simple. It should be held high until SA goes low. If SA is already low, a narrow CR pulse will suffice. Thus, a brief Cycle Request will cause the memory to execute one complete cycle and stop. If CR is held high, the memory will access (SA goes high) and then will leave the clock high until CR goes low. This allows Read/Modify/Write operations to be performed quite easily.

## Interleaved Operation

With the clock derived locally within the memory from the MS signals, and with the clocking logic integrated on a single chip, it becomes convenient to individually clock each row of a memory system. An example configuration is shown in Figure 27, with each support logic block being similar to the circuitry previously discussed. Each row is clocked only when it is addressed by the Chip Select signal (A0 or $\overline{A0}$). Unselected rows wait in their preset state until they are selected and clocked. The Cycle Request input is steered to the selected row by added logic. The Status Acknowledge outputs are three-state and only the SA for the selected row is turned on. The selected row will proceed when its preset is complete. When the data from the requested operation is available, the Status Acknowledge output goes high. The using system can then request another operation immediately once a new address is ready.

Independent clocking of each row adds little support circuit complexity while providing increased overall performance in two ways. First, the speed of each access is limited only by the slowest device in the selected row rather than the slowest device in the whole array. Secondly, successive operations in different rows will be faster because the wait for preset is eliminated; one row will preset while another is being accessed. Notice that the low order bit is used as the Chip Select address. In many systems, this will improve the distribution of alternate accesses for sequential information by mapping even addresses in one row and odd addresses in the other.

In any event, no matter where the operation is addressed or when it is requested, the memory will respond in the best possible time. The Cycle Request and Status Acknowledge signals form a true asynchronous handshaking pair. All of the variations in performance caused by the timing of the request, the row addressing patterns, the speeds of the individual chips and the memory operating conditions are automatically reflected in the response of the Acknowledge signal. An interesting challenge will be to design using systems that can take advantage of this unusual capability.

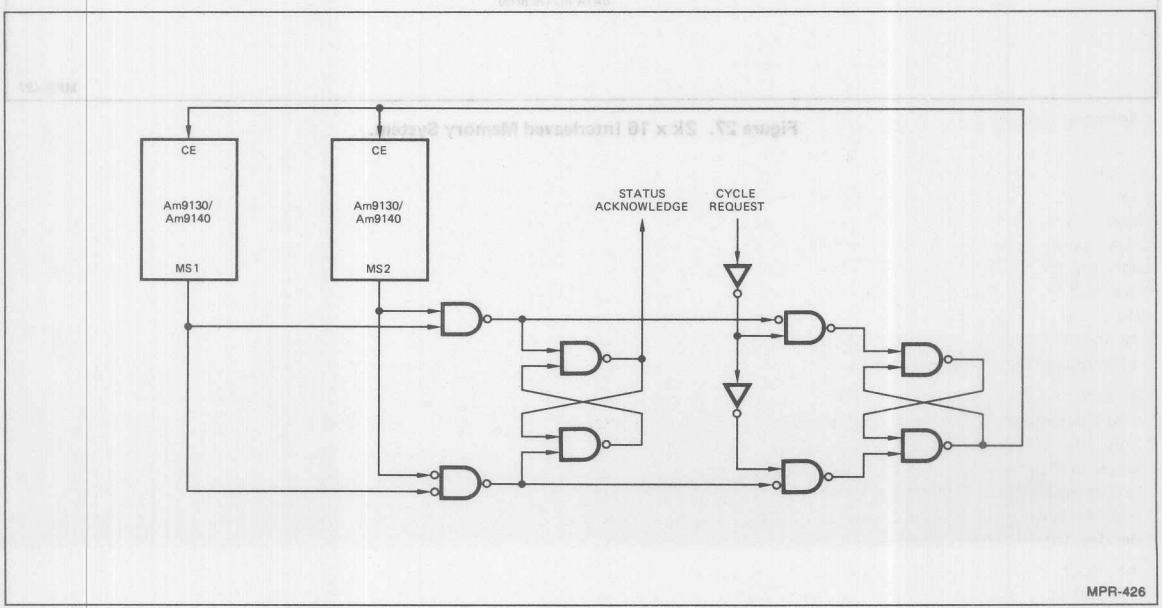



**Figure 26. Handshaking Control.**

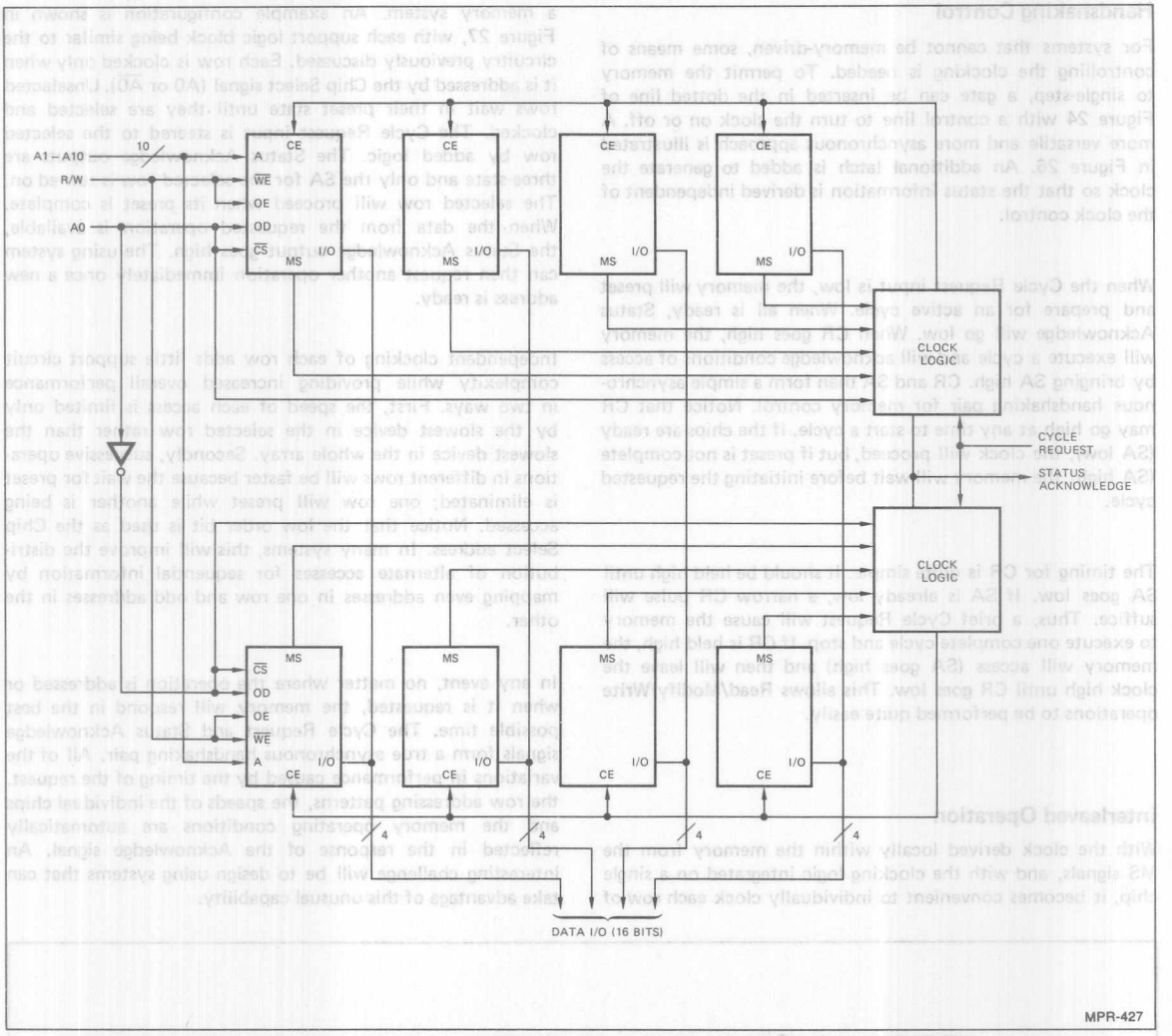



Figure 27. 2k x 16 Interleaved Memory System.

# APPLICATION OF FIRST-IN FIRST-OUT MEMORIES

By John Springer, Digital Applications

The Am3341/2841, Am2812 and Am2813 are asynchronous first-in first-out memories using P-channel silicon gate MOS technology. All use the same fundamental storage mechanism, but are organized differently. The Am3341/2841 contains up to 64 four-bit words; the Am2812 holds up to 32 eight-bit words; the Am2813 holds up to 32 nine-bit words. All devices can easily be expanded to hold either more words or wider words. The Am2841 is functionally identical to the Am3341, but is faster. The logic symbols for these devices are shown in Figure 1.

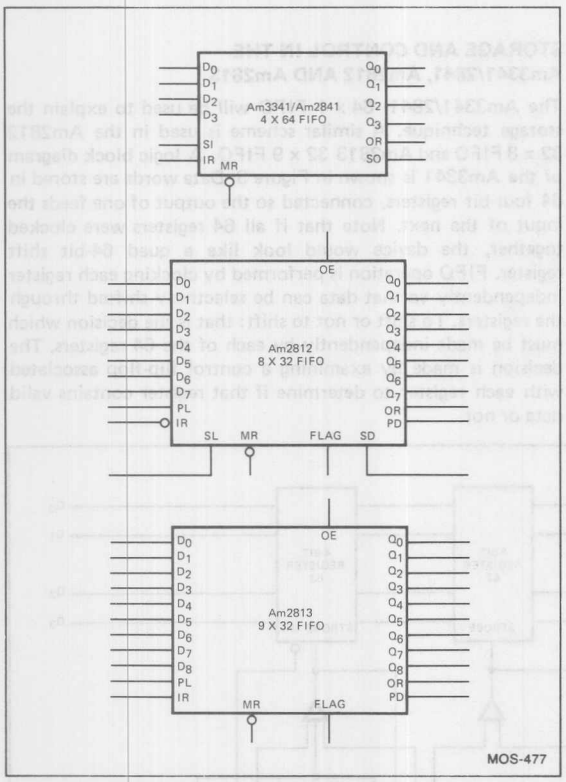



Figure 1. Logic Symbols

## THE FUNCTION OF A FIRST-IN FIRST-OUT MEMORY

A first-in first-out memory (FIFO) is a read/write data storage unit that automatically keeps track of the order in which data was entered into the memory, and reads the data out in the same order. It behaves like a shift register whose length is always exactly equal to the number of words stored. The most common application of a FIFO is as a buffer memory between two pieces of digital equipment operating at different speeds. Such an application is illustrated in Figure 2, where machine 1 might be a relatively slow electromechanical input device and machine 2 might be a digital computer (or vice-versa). Data is frequently handled in a configuration like this by having machine 1 generate an interrupt requesting service from machine 2 every time a data word is available. If machine 1 transmits only a single word infrequently then the interrupt-oriented approach is reasonable, but if machine 1 is going to transmit 20 or 30 words, then the interrupt approach is inefficient. As each of the words becomes available, an interrupt must be generated, machine 2 must react, cleaning up its active processing, locate the interrupt, store the new data word, and return to its active processing only to receive another interrupt milliseconds later.

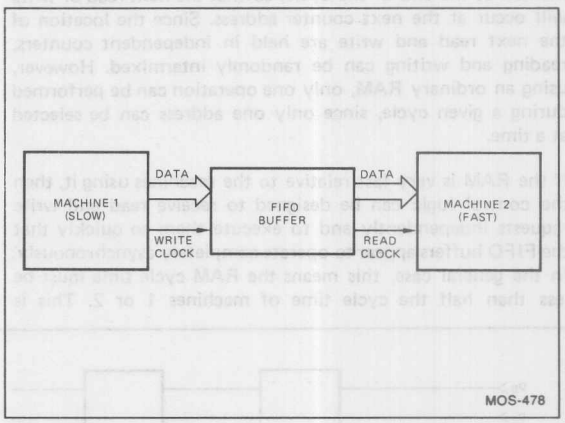



Figure 2. Asynchronous Interface between Two Digital Machines

An alternative processing method is cycle stealing on a direct memory access (DMA) channel. In this configuration the system is designed so that machine 1 has direct access to the memory of machine 2. As data becomes available from machine 1, it is inserted into machine two's memory during time periods when machine 2 is not using the memory. This method is fairly efficient, especially for transfer of large blocks of data from a disc or tape, but it also can result in interference with the active processing of machine 2 due to contention for the memory channel.

The most efficient way to handle the interface between these two machines is by using a special memory between the machines to temporarily store the data from machine 1 until machine 2 is ready to accept it. The memory must be large enough to store all the data that machine 1 might generate in-between services by machine 2, and should be able to write the data at the speed of, and under control of, machine 1,

9

while reading the data at the speed of machine 2. An extremely useful feature in such a memory is the ability to perform read and write operations at the two different rates simultaneously and completely independently. This allows machine 1 to write new data into the memory at the same time that machine 2 is reading data from the memory without requiring any kind of synchronization between the two.

## METHODS OF CONSTRUCTING FIFO BUFFERS

There are a number of ways in which FIFO memories can be built. The design becomes trivial if there is no requirement for independent reading and writing. The data can be written into a shift register, for example, which is clocked by machine 1. When a block of data has been written, the register can be shifted until the first data word is available at the output, and then shift control can be handed to machine 2, which shifts the data out as required. This method requires that data transfer occur in blocks only, since once the data has been shifted to the output, a new word cannot be written until the last block has been completely read.

A somewhat more flexible FIFO can be built using a random access memory with counters used to generate the read and write addresses. A multiplexer is used to select the appropriate address counter for a read or write, and the counter is incremented at the end of the cycle, so that the next read or write will occur at the next counter address. Since the location of the next read and write are held in independent counters, reading and writing can be randomly intermixed. However, using an ordinary RAM, only one operation can be performed during a given cycle, since only one address can be selected at a time.

If the RAM is very fast relative to the machines using it, then the control logic can be designed to receive read and write requests independently and to execute them so quickly that the FIFO buffers appear to operate completely asynchronously. In the general case, this means the RAM cycle time must be less than half the cycle time of machines 1 or 2. This is necessary so that the buffer can perform alternate read and write operations at the maximum speed of both machines. The control logic to do this is fairly complex and requires an independent clock running at more than twice the frequency of machine 1 or 2.

The problem of handling read and write operations simultaneously is alleviated if a 2-port RAM is used. Such a device (e.g., the Am9338) has two independent sets of address inputs, one for reading and one for writing, so no synchronizing of read and write requests need occur. Unfortunately, two port RAMs are limited to small numbers of bits, and, therefore, are fairly expensive to use in a FIFO of reasonable size.

The Am3341/2841, Am2812 and Am2813 are totally integrated solutions to the problem of asynchronous FIFOs. A special unique control system is integrated into the device to make possible completely independent reading and writing. Because the control and data storage are intimately mixed on one LSI chip, a very efficient, cost-effective FIFO can be constructed. The three devices, all of which use the same basic control scheme, are organized into three different configurations to provide optimum flexibility for all applications.

## STORAGE AND CONTROL IN THE Am3341/2841, Am2812 AND Am2813

The Am3341/2841, 64 x 4 FIFO will be used to explain the storage technique. A similar scheme is used in the Am2812 32 x 8 FIFO and Am2813 32 x 9 FIFO. A logic block diagram of the Am3341 is shown in Figure 3. Data words are stored in 64 four-bit registers, connected so the output of one feeds the input of the next. Note that if all 64 registers were clocked together, the device would look like a quad 64-bit shift register. FIFO operation is performed by clocking each register independently so that data can be selectively shifted through the registers. To shift or not to shift: that is the decision which must be made independently by each of the 64 registers. The decision is made by examining a control flip-flop associated with each register to determine if that register contains valid data or not.

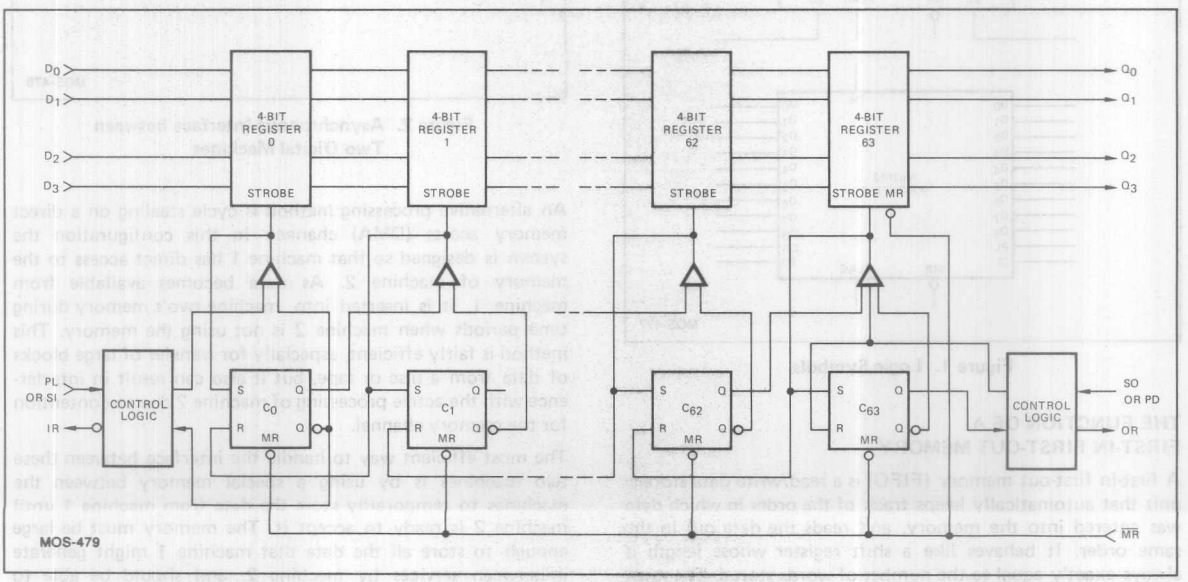



Figure 3

Initially, the FIFO is reset and there is no data anywhere in it. The control flip-flops are all reset to "0." A write command causes a 4-bit data word to be entered into the first register and sets the control flip-flop for that register, indicating valid data is present. The control flip-flop for the second register is a "0" and this causes it to continually examine the control flip-flop for the first register, looking for a "1." When the data is written into the first register, the second register sees the "1," and a clock is generated to it, copying the data from the first register into the second, setting the control flip-flop for the second register, and clearing the control flip-flop for the first register. In exactly the same fashion, the third register copies the data from the second, and the fourth from the third until finally the data ends up in the last location. At this point all 64 registers contain the same data, but only the last control flip-flop contains a "1," the others all having been reset as the data was copied into the next register.

As soon as the data moves from the first register to the second, the control flip-flop for the first register is cleared. A new data word can then be written into the first register. The first control bit is brought out as "input ready" (IR), and data can be entered anytime it is HIGH. When the data has been accepted, IR goes LOW (a "1" in the control bit) and when the data moves to the second register, IR goes HIGH again. The new data falls through the registers as long as there are "0s" in the corresponding control flip-flops. Eventually it reaches the register immediately behind a register already containing data. Since the control bit for that register is already a "1," the data is not moved any further and remains stacked up behind the existing data. A read command on the output causes the last control flip-flop to be cleared, creating a new empty location. The next to the last word is copied into the last word and the hole in the control register moves back toward the input as the data words move down one place. This process can continue until all data has been shifted out of the memory. When the last word has been read the external signal output ready (OR) remains LOW, indicating no more data is available.

This scheme allows the reading and writing of data to occur completely independently and even simultaneously. Data can be written into the device as rapidly as the device is capable of moving it away from the first register; it can be read at the same rate. The only constraint imposed by this scheme is that a certain amount of time is required for the first data word to propagate to the end of the register. This time is referred to as the "ripple-through" time and is the internal shift time multiplied by the number of bits from input to output.

## CONTROL SIGNALS TO THE Am3341/2841 AND Am2813

There are four signals used with the Am3341/2841 and Am2813 to control the reading and writing of data. These are parallel load (PL, or SI on 3341), input ready (IR), parallel dump (PD or SO on 3341) and output ready (OR).

The two outputs, IR and OR, are derived from the state of the first and last control flip-flops, respectively, and are used to indicate the presence or absence of data at the input and output of the FIFO. When IR is LOW (that is, input not ready) then there is data residing in the first data register. New data may not be entered until this data has moved to the second register, indicated by IR going HIGH. The OR signal goes HIGH whenever valid data is present on the FIFO output. Whenever a shift-out command is received, OR goes LOW while the data is being changed. If there is no more data, OR stays LOW, indicating the memory is empty. Otherwise OR returns HIGH as soon as the new data is on the outputs. Data is entered into the FIFO by a LOW-to-HIGH transition on shift-in (PL), while IR is HIGH. The fact that both these signals are HIGH causes a strobe to the first data register to be generated, loading the data on the data inputs into register and setting the first control flip-flop. When the control flip-flop is set, IR goes LOW, indicating the data has been accepted. The input data can be changed after IR has gone LOW. When SI is then brought LOW, the data is transferred to the next register (unless there is already data there) and IR goes back HIGH, indicating that the input is ready to receive more data. If the memory is full, then the data in the first register will not move to the second, and IR will stay LOW. Once data moves into the second register, it falls spontaneously through the FIFO until it stacks up behind data already present.

Data in the last FIFO location is presented on the data outputs. While data is there, OR is HIGH. The next data word is obtained by applying a LOW-to-HIGH transition on shift-out (SO). This results in OR going LOW. The data does not actually change until SO is brought LOW again. The new data, if any, will be brought to the output and, after the data is stable, OR will go HIGH again. If the memory is empty, OR will remain LOW until a new word falls through from the input. Note that anytime OR is HIGH, there is good, stable data on the outputs.

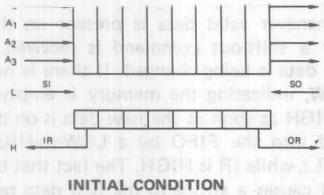
## MASTER-RESET

The master reset pin ($\overline{MR}$) is used to clear all data from the FIFO. When it goes LOW, all the control flip-flops are cleared and the output buffer is cleared. IR will be forced HIGH during this time. When the $\overline{MR}$ signal is removed the FIFO is ready to accept new data. Note that if SI is held HIGH as the master reset ends, then both SI and IR will be HIGH, resulting in immediate entry of the data on the data inputs into the FIFO. If this is not desired, then SI should be held LOW during the master reset and until new data is ready to be entered.

## EXPANSION METHODS USING THE Am3341/2841

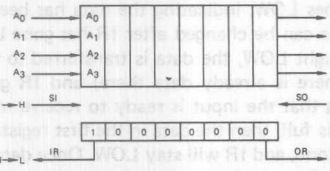
The four control signals on the Am3341 have been designed so that devices can be directly connected end-to-end, as in Fig. 6, and can thereby control each other. When data appears at the output of the first device OR goes HIGH. This causes an SI command to the second device which in turn causes IR to go LOW. Since IR is connected to SO, this causes a shift-out at the first device, driving OR LOW until new data is available, and the process repeats. Lengthening of the FIFO stack requires only this simple interconnection.

To make a wider FIFO devices are simply operated in parallel. Since each device is autonomous there need be no interconnection between paralleled devices, except that all the shift-ins at the front are connected together and all the shift outs at the end are connected together. Data then ripples independently through each row of FIFOs.

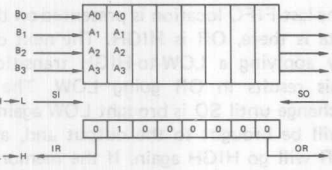



**INITIAL CONDITION**

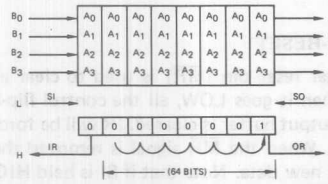
FIFO empty, SI LOW IR HIGH, word "A" on inputs.



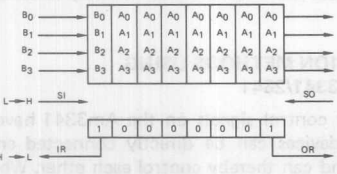

Write input into first stage by raising SI. (Δ = delay) IR goes LOW indicating data has been entered.



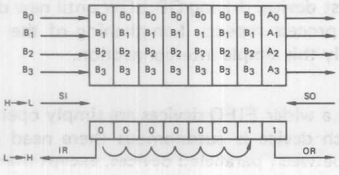

Release data into FIFO by lowering SI. After delay, data moves to second location, and IR goes HIGH indicating input available for new data word.



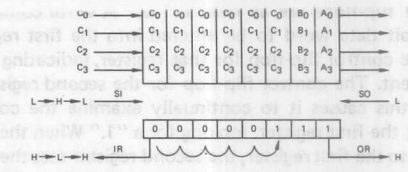

Data spontaneously ripple through registers to end of FIFO, causing OR to go HIGH. The time required for data to fall completely through the FIFO is the "Ripple-through Time".



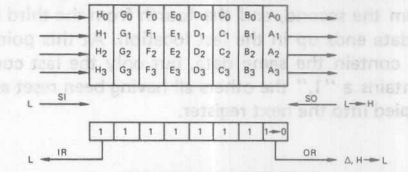

Word "B" written into FIFO




SI goes LOW allowing word "B" to fall through.

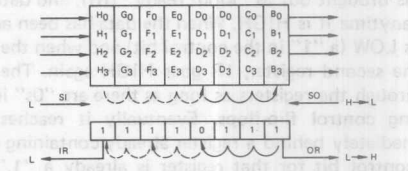



Word "C" written in same manner, and so on. When buffer is full, all control bits are 1's and IR stays LOW.

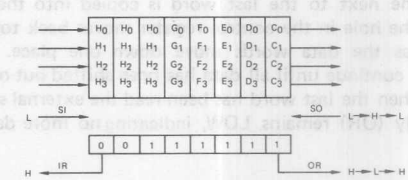



**FIRST READ OPERATION**

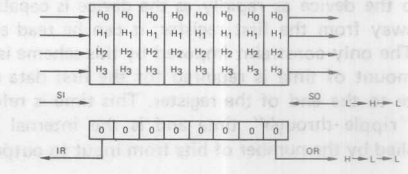
SO goes HIGH, indicating "Ready to Read". OR then goes LOW indicating "Data Read".




When SO goes LOW, the "0" in the last control bit bubbles toward the memory input. OR goes HIGH as the new word arrives at the output. IR goes HIGH when "0" reaches input.



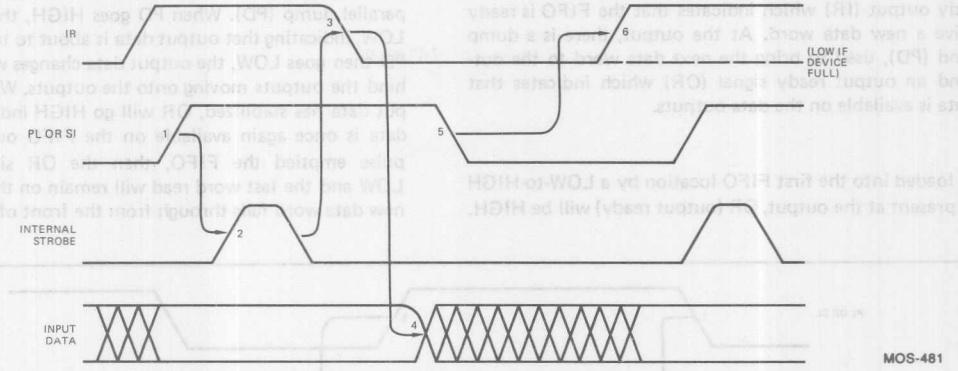

Read word "B" out, word "C" moves to output, and so on.




Read word "H". OR stays LOW because FIFO is empty. Word "H" remains in output until new word falls through.

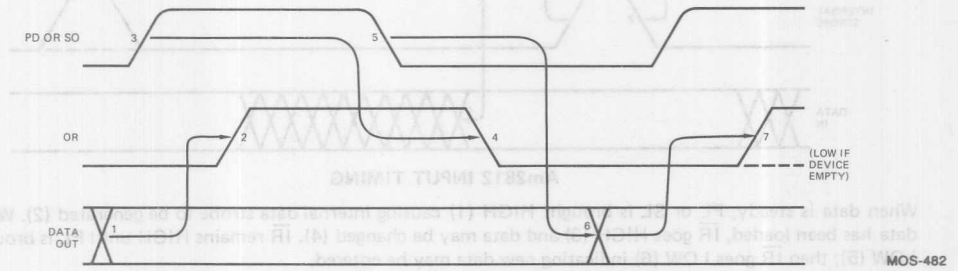
**Figure 4**

MOS-480




**INPUT TIMING SEQUENCE, Am3341/2841 AND Am2813**

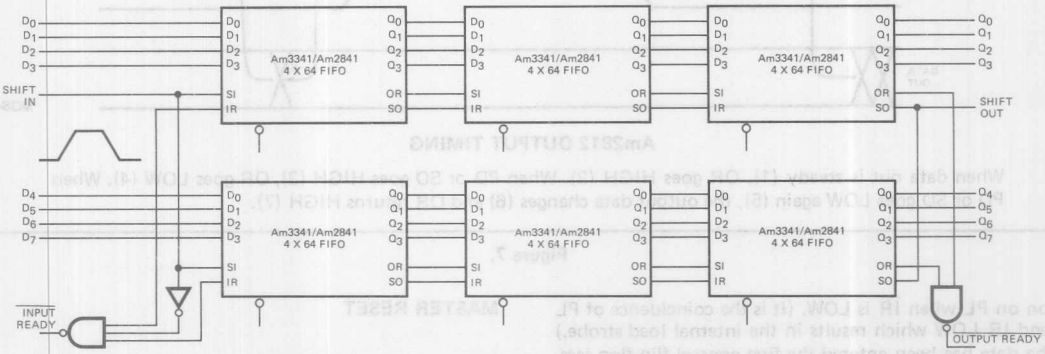
SI is brought HIGH (1) causing internal strobe (2) which loads data. When data has been loaded, IR goes LOW (3) indicating data can be changed (4). SI may then be brought LOW (5) causing IR to return HIGH (6).




**OUTPUT TIMING SEQUENCE, Am3341/2841 AND Am2813**

Data out changes (1); then OR goes HIGH (2). When SO goes HIGH (3), OR goes LOW (4) indicating data is about to change. After SO goes LOW (5) the data actually changes (6) and after it is stable, OR goes HIGH again (7).

**Figure 5**




The composite input ready indicates both devices are ready to receive data. The shift in pulse must be wide enough for all devices to load data under worst case conditions.

**Figure 6. 8 x 192 FIFO Buffer Using Am3341/2841**

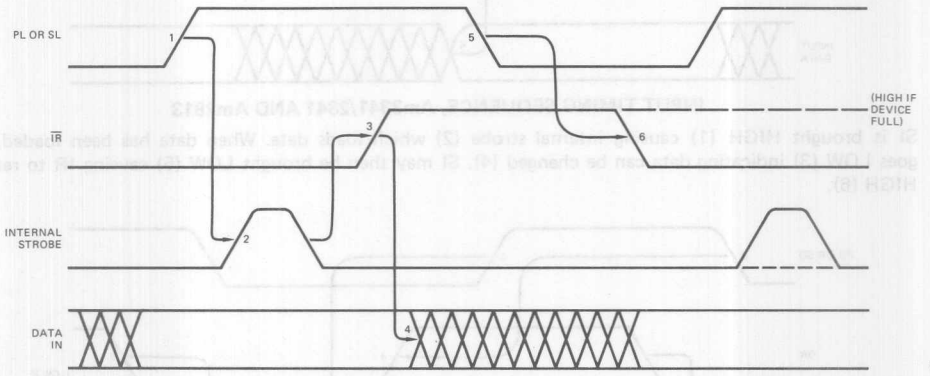
## CONTROL SIGNALS ON THE Am2812

The Am2812 is controlled exactly like the Am3341 and Am2813, except that the input ready signal is inverted. Internally operation is like the Am3341/2841. The control signals are slightly different, however, and there are some additional features. There is a parallel load (PL) input, used to

load an 8-bit word onto the first stage of the FIFO, and an input ready output ($\overline{IR}$) which indicates that the FIFO is ready to receive a new data word. At the output, there is a dump command (PD), used to bring the next data word to the outputs, and an output ready signal (OR) which indicates that good data is available on the data outputs.

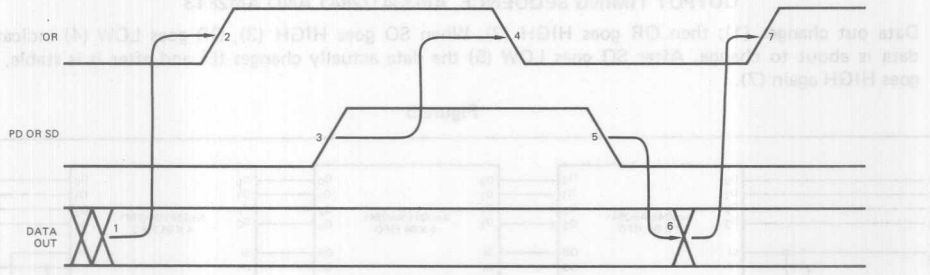
Data is loaded into the first FIFO location by a LOW-to-HIGH word is present at the output, OR (output ready) will be HIGH.

The next data word is shifted onto the outputs by a pulse on parallel dump (PD). When PD goes HIGH, the OR signal goes LOW, indicating that output data is about to be changed. When PD then goes LOW, the output data changes with the word behind the outputs moving onto the outputs. When the new output data has stabilized, OR will go HIGH indicating that good data is once again available on the FIFO outputs. If the PD pulse emptied the FIFO, then the OR signal will remain LOW and the last word read will remain on the outputs until a new data word falls through from the front of the FIFO.




**Am2812 INPUT TIMING**

When data is steady, PL or SL is brought HIGH (1) causing internal data strobe to be generated (2). When data has been loaded, $\overline{IR}$ goes HIGH (3) and data may be changed (4). $\overline{IR}$ remains HIGH until PL is brought LOW (5); then $\overline{IR}$ goes LOW (6) indicating new data may be entered.




**Am2812 OUTPUT TIMING**

When data out is steady (1), OR goes HIGH (2). When PD or SD goes HIGH (3), OR goes LOW (4). When PD or SD goes LOW again (5), the output data changes (6) and OR returns HIGH (7).

**Figure 7.**

transition on PL when $\overline{IR}$ is LOW. (It is the coincidence of PL HIGH and IR LOW which results in the internal load strobe.) When the data has been entered the first control flip-flop sets, causing $\overline{IR}$ to go HIGH. When PL goes LOW again, the data in the front of the FIFO begins falling through the stack toward the output, and $\overline{IR}$ goes LOW as soon as it has moved to the second register. If the FIFO was filled to capacity when the data was loaded, then $\overline{IR}$ will stay HIGH; new data cannot be entered, and any additional shift in command will be ignored until $\overline{IR}$ goes LOW after some data has been removed from the FIFO.

Data entered into the FIFO falls through the registers until it reaches either the output or another data word. When a data

## MASTER RESET

A direct clear signal can be applied to the FIFO by a LOW logic level on the $\overline{MR}$ input. This will clear all the internal control register bits and will clear the data from the outputs. $\overline{IR}$ will go LOW indicating the FIFO is ready to receive new data. If the PL input is held HIGH when the $\overline{MR}$ returns to a HIGH state, then an internal input strobe will be generated, and whatever data is on the inputs will be loaded into the FIFO. If this is not desired then PL should be held LOW at the end of the master reset. The master reset will cause OR to go LOW and remain LOW until new data falls through from the input.

## FLAG

A flag output is available on the Am2812 and Am2813 to indicate whether the FIFO is more or less than half full. The flag signal is generated by summing the "1s" in the control flip-flops, and therefore is not affected by the movement of data through the register. The flag signal goes HIGH when the 15th ±1 (i.e., the 14th, 15th, or 16th) word is loaded into the FIFO. It will remain HIGH until there are less than 15 ±1 words in the memory. It is always HIGH if there are more than 16 words in the FIFO.

## OUTPUT ENABLE

The Am2812 and Am2813 data outputs are 3-state signals. When OE is HIGH, they will be in either a HIGH or LOW state; if OE is LOW, they will go to a high-impedance OFF state. Outputs of several FIFO buffers can then be tied together onto a bus, and one of the buffers can be selected to drive the bus. When OE is LOW, the dump function (both SD and PD) is disabled.

## SERIAL INPUT AND OUTPUT (Am2812 ONLY)

The Am2812 also has the ability to read or write serial bit streams, rather than 8-bit words. The device then works like a 256 by 1-bit FIFO. A serial data stream can be loaded into the device by using SL clock input and applying data to $D_0$ input. Inputs $D_1$ – $D_7$ must be grounded. The SL signal operates just like the PL input, causing $\overline{IR}$ to go HIGH and LOW as the bits are entered. The data is simply shifted across the 8-bit input register until 8 bits have been entered; the 8 bits then fall through the register as though they had been loaded in parallel.

A corresponding operation occurs on the output, with clock pulses on SD causing successive bits of data to appear on the $O_7$ output. OR moves HIGH and LOW with SD exactly as it does with PD. When 8 bits have been shifted out, the next word appears at the output. If a PD command is applied after the 8 bits on the outputs have been partially shifted out, the remainder of the word is dumped and a new 8-bit word is brought to the output.

When one of the serial clocks is used, the corresponding parallel signal (PL or PD) should be grounded.

## EXPANSION OF THE Am2812 AND Am2813

The input and output shift and ready signals have been designed so FIFOs can be directly connected end-to-end to make a longer (i.e., more words) buffer memory, as shown in the applications in Figures 10 and 11. Wider words can be stored by using independent FIFO stacks, side by side, like the Am3341s in Figure 6. When FIFOs are connected end to end, the total number of words that can be stored is (31n+1) not 32n. This is due to the fact that when an SI command loads the 32nd word into a FIFO, the $\overline{IR}$ output stays HIGH, and no PD pulse is applied to the adjacent up-stream FIFO. As a result the word just written into the FIFO is duplicated at the output of the previous FIFO. When at least one word is removed from the downstream FIFO, the $\overline{IR}$ signal goes LOW, causing the duplicated word to be dumped from the up-stream device.

## SYSTEM INTERFACING

Normally the input and output of a stack of FIFOs are interfaced with TTL logic. A special interface circuit is used internally on the inputs of the AMD family of FIFOs to provide complete electrical compatibility with TTL outputs; no external components need be used. The circuit works by using an MOS transistor inside the chip as a pull-up resistor in the HIGH state. When the voltage applied to the input is LOW, the internal resistor is disabled and presents no loading to the TTL output. THE V-I characteristic of the input is shown in Figure 8.

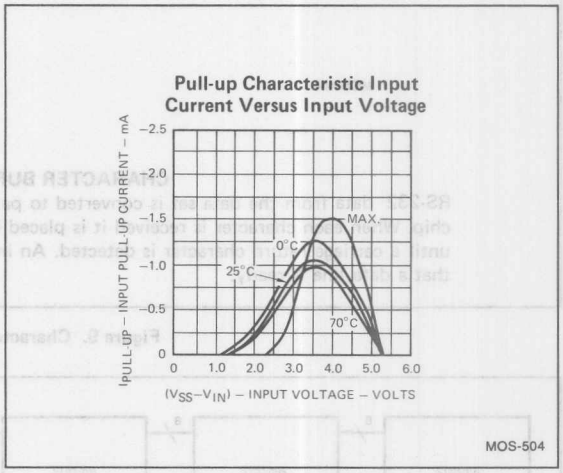
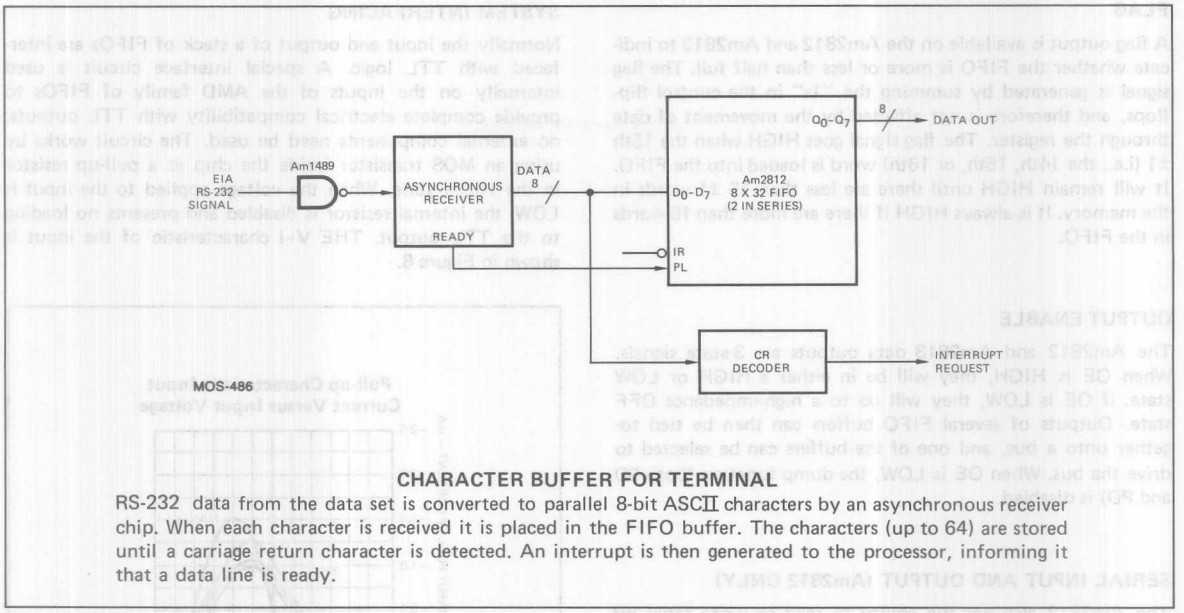



**Figure 8. Input Voltage Current Characteristics**

The logical interface between the FIFO inputs and the rest of the system must detect that all device inputs are ready, and then supply a shift in command when new data is available. Normally this is rather simple, since most data transfer interfaces contain a data strobe control and a not ready signal. Some caution must be exercised when a composite Input Ready signal for a parallel stack of FIFOs is formed. The inputs to the stack are ready to receive data only when PL is LOW and all input ready signals are HIGH (LOW on the Am2812. Data can be removed from the inputs to the stack only when all input ready signals have gone LOW (HIGH on the Am2812). The easiest way to handle this situation is to detect only that all inputs are ready to receive data, and then insure that data remains as long as is required by the worst case specification, rather than actually detecting that the data has been loaded into all devices.

The data on the data inputs must be held steady for about a 400ns period following the SI or PL LOW-to-HIGH transition. The internally generated data strobe will occur sometime during this period. The strobe will not occur, however, until at least 25ns after the SI transition. The rising SI signal may therefore also be a clock to a TTL register feeding the data inputs, as there is sufficient time available for the $t_{pd}$ of the register. However, it is preferable to change the input data on the falling edge of SI for additional timing margin in the system.

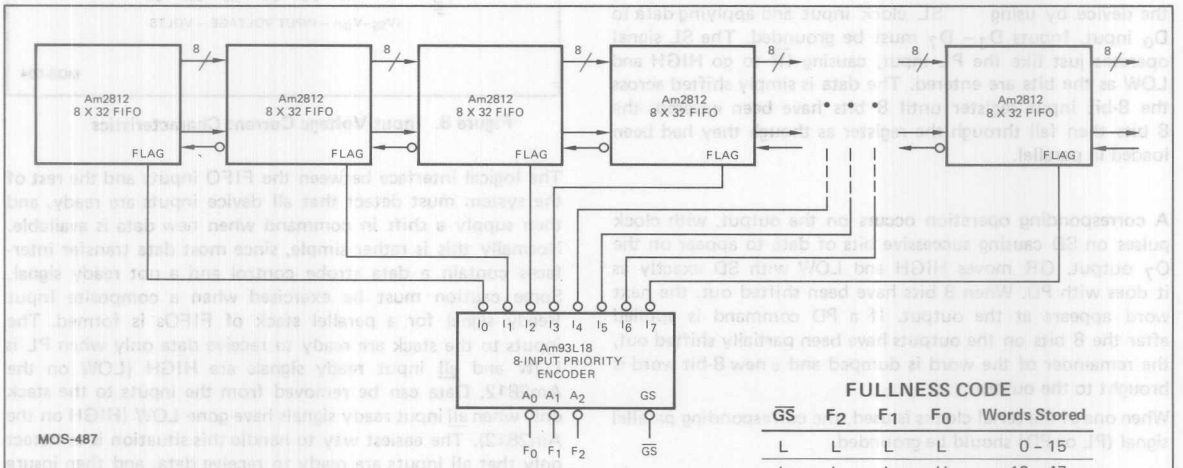
At the output of the FIFO, the logic must detect that all outputs are ready, and then supply the dump command when the data has been received by the system. Again, these two kinds of signals are normally available in systems.




**CHARACTER BUFFER FOR TERMINAL**

RS-232 data from the data set is converted to parallel 8-bit ASCII characters by an asynchronous receiver chip. When each character is received it is placed in the FIFO buffer. The characters (up to 64) are stored until a carriage return character is detected. An interrupt is then generated to the processor, informing it that a data line is ready.

**Figure 9. Character Buffer for Terminal.**

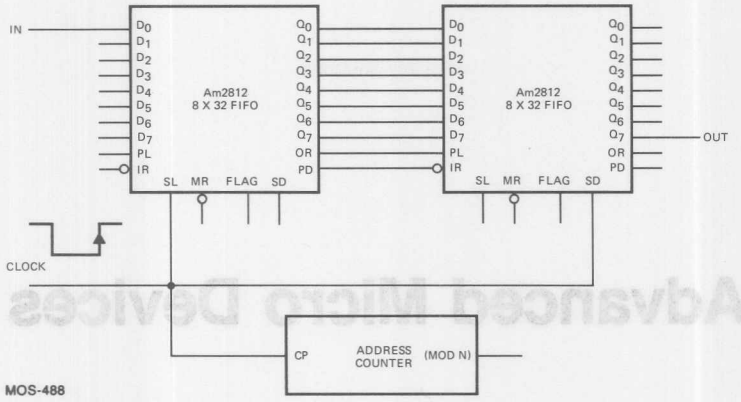



**FULLNESS CODE**

| $\overline{GS}$ | $F_2$ | $F_1$ | $F_0$ | Words Stored |
|---|---|---|---|---|
| L | L | L | L | 0 - 15 |
| L | L | L | H | 13 - 47 |
| L | L | H | L | 45 - 78 |
| L | L | H | H | 76 - 109 |
| L | H | L | L | 107 - 140 |
| L | H | L | H | 138 - 171 |
| L | H | H | L | 169 - 202 |
| L | H | H | H | 200 - 233 |
| H | H | H | H | 231 - 249 |

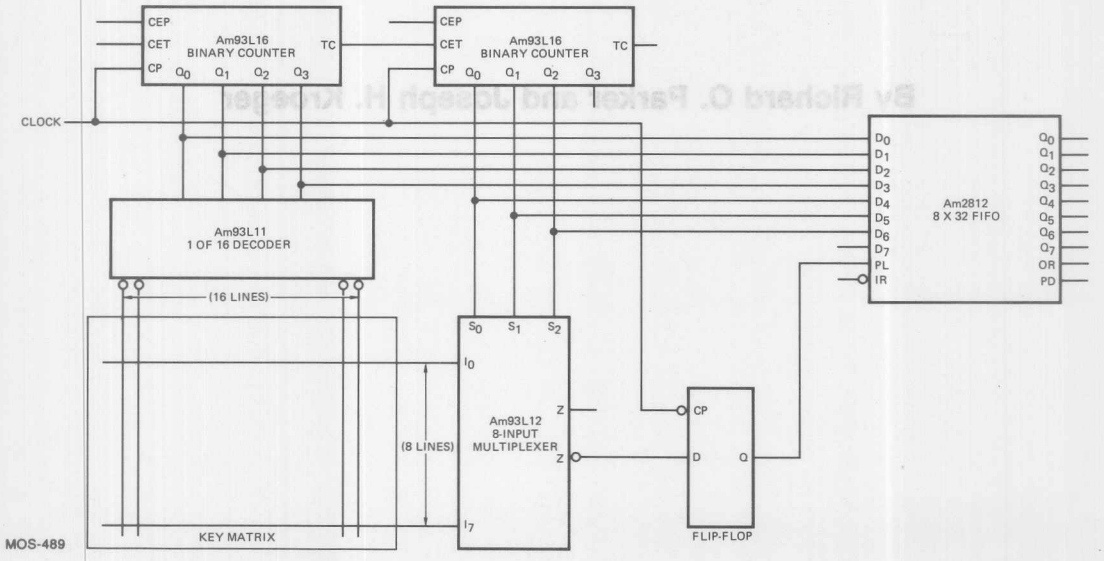
The Fullness Flags from Am2812 or Am2813 FIFOs can be encoded by an Am93L18 8-input priority encoder. The output code $F_0$-$F_2$ indicates the weight of the highest priority input which is LOW. GS is group signal; it is HIGH if all the inputs are HIGH. For the Am2813, the words stored starting with 47 will be one more than is indicated in the table.

**Figure 10**




The serial I/O of the Am2812 is used, with data clocked into the $D_0$ input by $CP_{IN}$ and clocked out of the $Q_7$ output by $CP_{OUT}$. Since data stacks up at the output end, the shift register appears to have a length corresponding to the number of words stored. For a 327-bit shift register, for example, it should be initialized with 327 O's. Data may then be entered or recirculated and the MOD 327 counter can be used to indicate the "address" of the current bit. A parallel transfer between devices is used.

**Figure 11. N-Bit Shift Register, N = 8 to 512.**



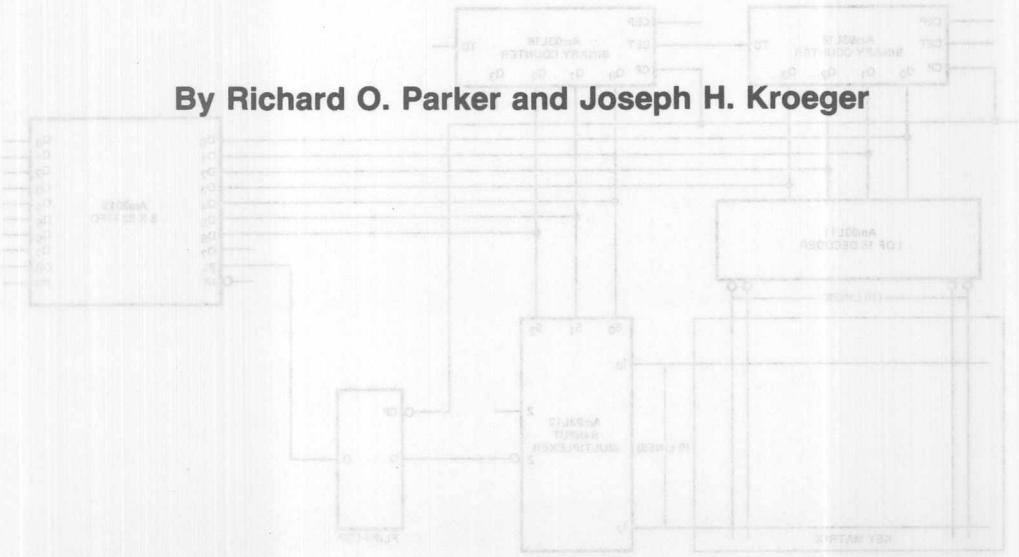

The combination of the counters and multiplexers act as a key encoder on the key matrix. A closure will produce a HIGH on the multiplexer output $\overline{Z}$ when the appropriate switch is scanned. The HIGH is stored in a flip-flop to provide a shift-in command to the FIFO one clock period wide. The flip-flop is clocked on the falling clock edge to insure the count is stable during the shift-in pulse.

**Figure 12. Storage of Switch or Key Closures.**

# Advanced Micro Devices

# Algorithm Details for The Am9511 Arithmetic Processing Unit

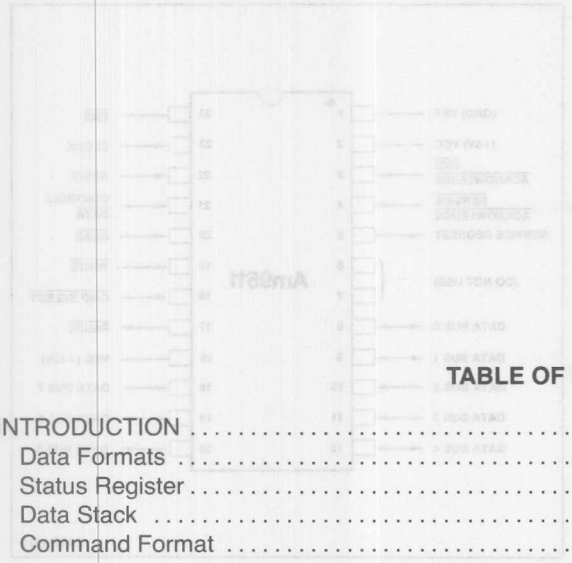
By Richard O. Parker and Joseph H. Kroeger



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AM-PUB072



## TABLE OF CONTENTS

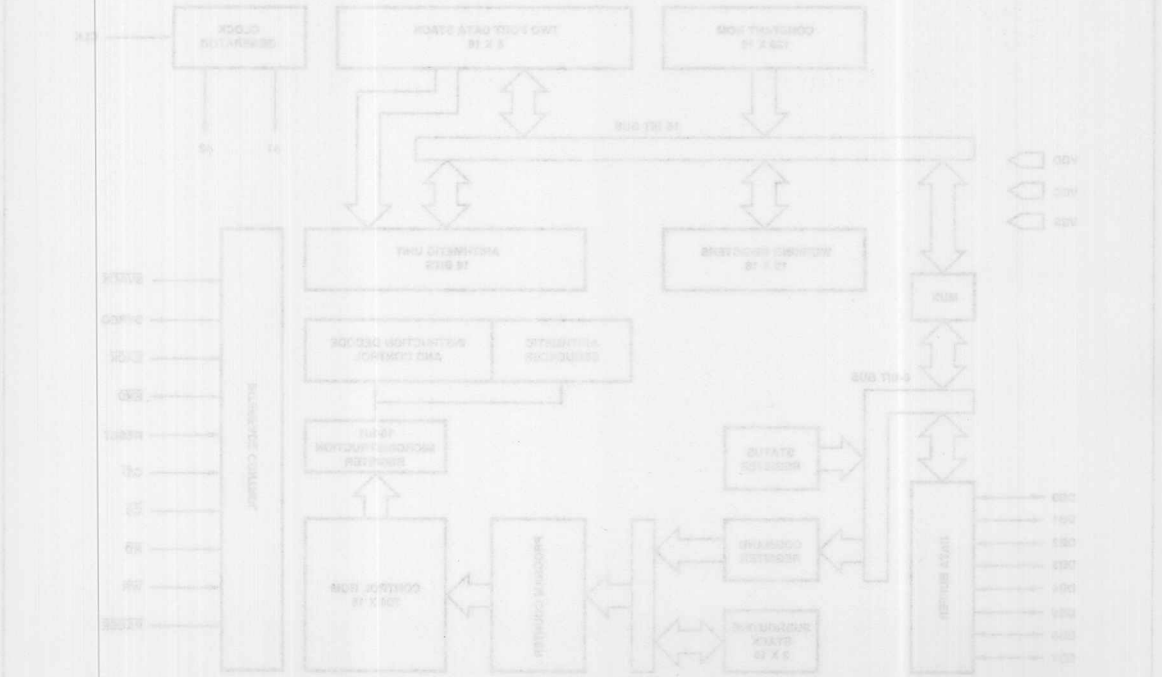

INTRODUCTION ..... 9-28
- Data Formats ..... 9-29
- Status Register ..... 9-29
- Data Stack ..... 9-29
- Command Format ..... 9-29

ALGORITHM DISCUSSION ..... 9-32

DERIVED FUNCTION ERROR PERFORMANCE ..... 9-32

COMMAND DESCRIPTIONS ..... 9-35

COMMANDS ..... 9-36

9

## INTRODUCTION

The Am9511 APU is a complete, high performance, complex arithmetic processor contained within a single chip. It is designed to enhance the number manipulation capability of a wide variety of processor systems. It includes not only floating-point operations but fixed-point as well; not only basic add, subtract, multiply and divide operations, but a group of transcendental derived functions plus control and conversion commands as well. This Application Brief provides detailed descriptions of all the commands that can be executed by the Am9511 and indicates the error performance of the derived functions.

The Am9511 is packaged in a standard, 24 pin, dual in-line package with .6 inch between rows. Figure 1 shows the package pin assignments. Details on the operation of each interface pin will be found in the data sheet.

The block diagram in Figure 2 shows the internal structure of the APU. The part is addressed as two ports selected by the C/$\overline{D}$ control line. When C/$\overline{D}$ is high (Control Port), a read op-

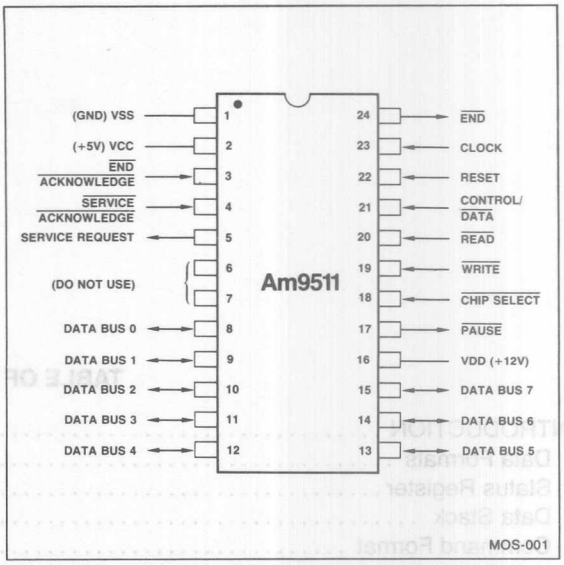



**Figure 1. Connection Diagram.**

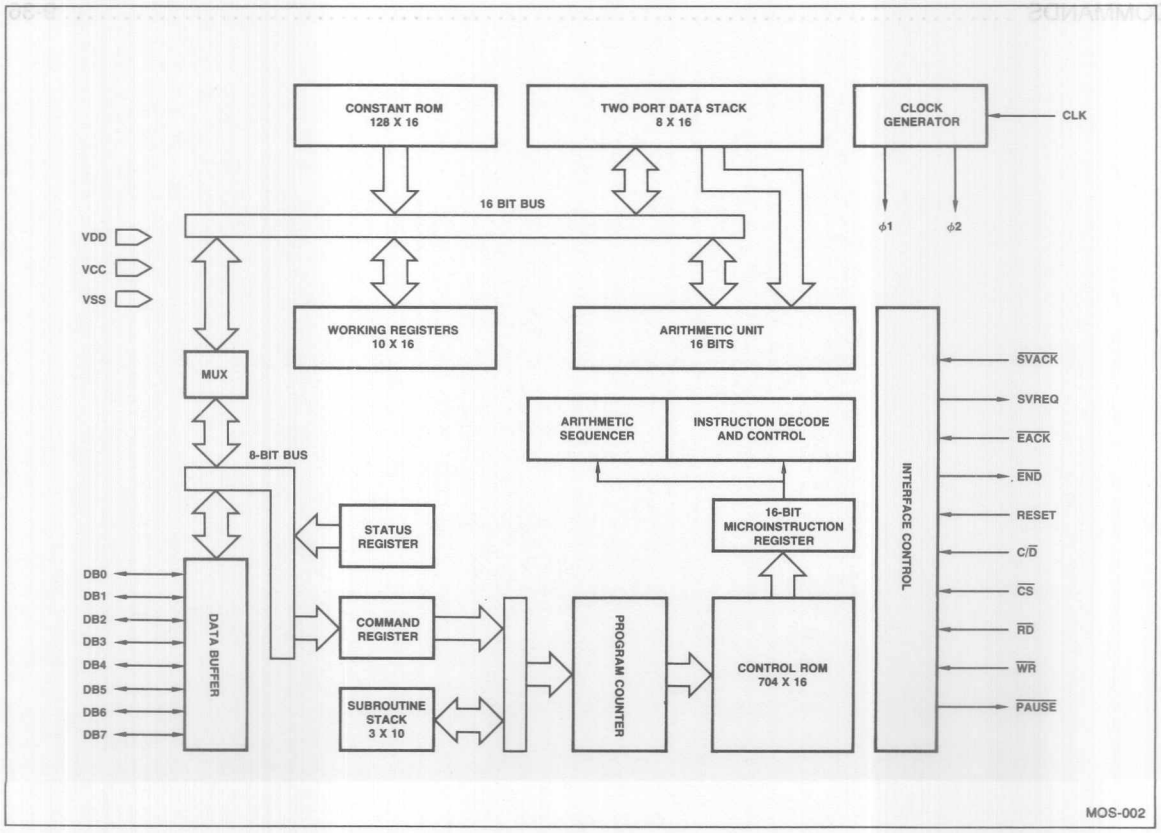



**Figure 2. Arithmetic Processing Unit Block Diagram.**

eration accesses the status register and a write operation enters a command. When C/$\overline{D}$ is low (Data Port), a read operation accesses data from the top of the data stack and a write operation enters data into the top of the data stack.

### Data Formats

The APU executes both 16- and 32-bit fixed-point operations. All fixed-point operands and results are represented as binary two's complement integer values. The 16-bit format can express numbers with a range of −32,768 to +32,767. The 32-bit format can express numbers with a range of −2,147,483,648 to +2,147,483,647.

The floating-point format uses a 32-bit word with fields as shown in Figure 3. The most significant bit (bit 31) indicates the sign of the mantissa. The next seven bits form the exponent and the remaining 24 bits form the mantissa value.

The exponent of the base 2 is an unbiased two's complement number with a range of −64 to +63. The mantissa is a sign-magnitude number with an assumed binary point just to the left of the most significant mantissa bit (bit 23). All floating-point values must be normalized, which makes bit 23 always equal to 1 except when representing a value of zero. The number Zero is represented with binary zeros in all 32 bit positions.

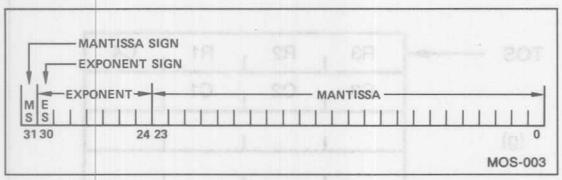



**Figure 3. Floating Point Format.**

### Status Register

The Am9511 Status register format is shown in Figure 4. When the Busy bit (bit 7) is high, the APU is processing a previously entered command and the balance of the Status register should not be considered valid. When the Busy bit is low, the operation is complete and the other status bits are valid.

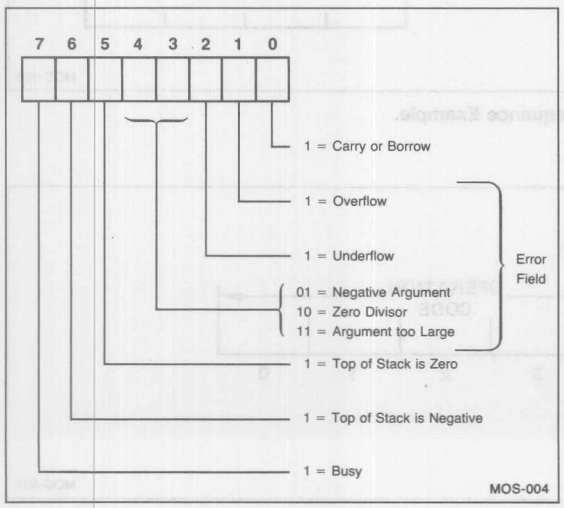



**Figure 4. Status Register.**

### Data Stack

Figure 5 shows the two logical organizations of the internal data stack. It operates as a true push-down stack or FILO stack. That is, the data first written in will be the data last read out. Within each stack entry, the least significant byte is entered first and retrieved last.

Figure 6 shows a typical sequence for 32 bit operations. 6a represents the stack prior to entry of data. 6b shows the stack following entry of the LS Byte of operand C. 6c illustrates the stack contents following the entry of four bytes of operand C. When operands C, B and A are all fully entered the stack appears as in 6e. If a command is then issued, to add B to A for example, the stack contents look like 6f where R is the result of B + A. When the first (MSB) byte of R is removed the stack appears as in 6g. 6h shows the stack following the complete retrieval or R. An even number of bytes should always be transferred for any data operation.

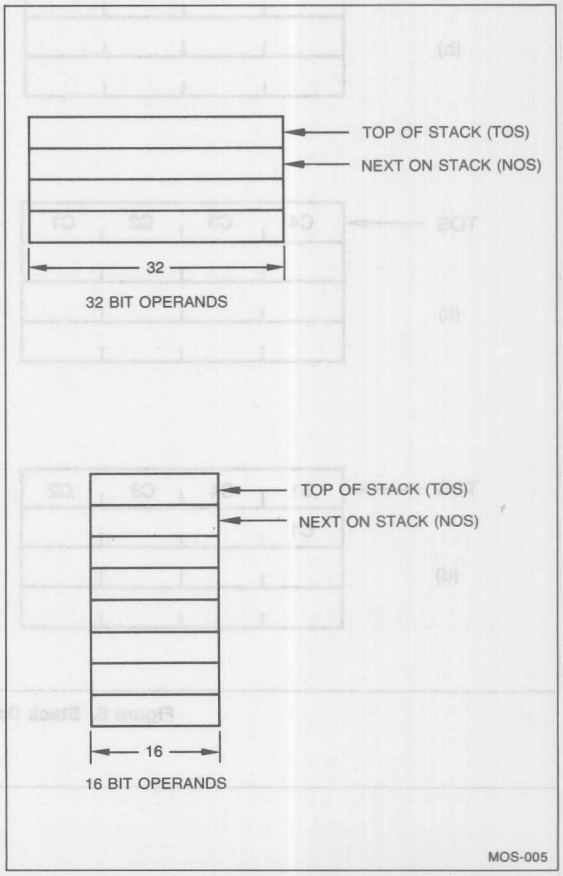



**Figure 5. Stack Configurations.**

### Command Format

Each command executed by the APU is specified by a single byte with the format shown in Figure 7. Bits 0 through 4 indicate the operation to be performed. Bits 5 and 6 specify the data format. Bit 7 is used to control the Service Request interface line. When bit 7 is a one, the SVREQ output will go true when the execution of the command is complete.

9




**Figure 6. Stack Data Sequence Example.**

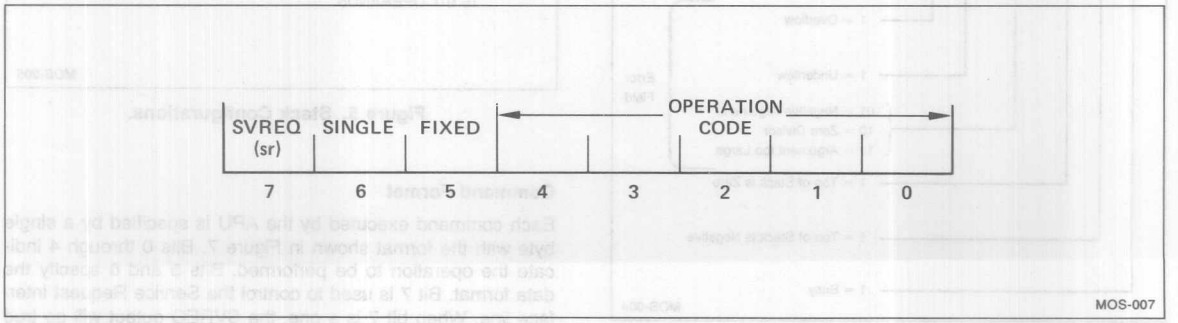



**Figure 7. Command Format.**

| Command Mnemonic | Hex Code (sr = 1) | Hex Code (sr = 0) | Execution Cycles | Summary Description |
|---|---|---|---|---|
| **16-BIT FIXED-POINT OPERATIONS** | | | | |
| SADD | EC | 6C | 16-18 | Add TOS to NOS. Result to NOS. Pop Stack. |
| SSUB | ED | 6D | 30-32 | Subtract TOS from NOS. Result to NOS. Pop Stack. |
| SMUL | EE | 6E | 84-94 | Multiply NOS by TOS. Lower result to NOS. Pop Stack. |
| SMUU | F6 | 76 | 80-98 | Multiply NOS by TOS. Upper result to NOS. Pop Stack. |
| SDIV | EF | 6F | 84-94 | Divide NOS by TOS. Result to NOS. Pop Stack. |
| **32-BIT FIXED-POINT OPERATIONS** | | | | |
| DADD | AC | 2C | 20-22 | Add TOS to NOS. Result to NOS. Pop Stack. |
| DSUB | AD | 2D | 38-40 | Subtract TOS from NOS. Result to NOS. Pop Stack. |
| DMUL | AE | 2E | 194-210 | Multiply NOS by TOS. Lower result to NOS. Pop Stack. |
| DMUU | B6 | 36 | 182-218 | Multiply NOS by TOS. Upper result to NOS. Pop Stack. |
| DDIV | AF | 2F | 196-210 | Divide NOS by TOS. Result to NOS. Pop Stack. |
| **32-BIT FLOATING-POINT PRIMARY OPERATIONS** | | | | |
| FADD | 90 | 10 | 54-368 | Add TOS to NOS. Result to NOS. Pop Stack. |
| FSUB | 91 | 11 | 70-370 | Subtract TOS from NOS. Result to NOS. Pop Stack. |
| FMUL | 92 | 12 | 146-168 | Multiply NOS by TOS. Result to NOS. Pop Stack. |
| FDIV | 93 | 13 | 154-184 | Divide NOS by TOS. Result to NOS. Pop Stack. |
| **32-BIT FLOATING-POINT DERIVED OPERATIONS** | | | | |
| SQRT | 81 | 01 | 782-870 | Square Root of TOS. Result to TOS. |
| SIN | 82 | 02 | 3796-4808 | Sine of TOS. Result to TOS. |
| COS | 83 | 03 | 3840-4878 | Cosine of TOS. Result to TOS. |
| TAN | 84 | 04 | 4894-5886 | Tangent of TOS. Result to TOS. |
| ASIN | 85 | 05 | 6230-7938 | Inverse Sine of TOS. Result to TOS. |
| ACOS | 86 | 06 | 6304-8284 | Inverse Cosine of TOS. Result to TOS. |
| ATAN | 87 | 07 | 4992-6536 | Inverse Tangent of TOS. Result to TOS. |
| LOG | 88 | 08 | 4474-7132 | Common Logarithm of TOS. Result to TOS. |
| LN | 89 | 09 | 4298-6956 | Natural Logarithm of TOS. Result to TOS. |
| EXP | 8A | 0A | 3794-4878 | e raised to power in TOS. Result to TOS. |
| PWR | 8B | 0B | 8290-12032 | NOS raised to power in TOS. Result to NOS. Pop Stack. |
| **DATA AND STACK MANIPULATION OPERATIONS** | | | | |
| NOP | 80 | 00 | 4 | No Operation. Clear or set SVREQ. |
| FIXS | 9F | 1F | 90-214 | Convert TOS from floating point format to fixed point format. |
| FIXD | 9E | 1E | 90-336 | |
| FLTS | 9D | 1D | 62-156 | Convert TOS from fixed point format to floating point format. |
| FLTD | 9C | 1C | 56-342 | |
| CHSS | F4 | 74 | 22-24 | Change sign of fixed point operand on TOS. |
| CHSD | B4 | 34 | 26-28 | |
| CHSF | 95 | 15 | 16-20 | Change sign of floating point operand on TOS. |
| PTOS | F7 | 77 | 16 | Push stack. Duplicate NOS in TOS. |
| PTOD | B7 | 37 | 20 | |
| PTOF | 97 | 17 | 20 | |
| POPS | F8 | 78 | 10 | Pop stack. Old NOS becomes new TOS. Old TOS rotates to bottom. |
| POPD | B8 | 38 | 12 | |
| POPF | 98 | 18 | 12 | |
| XCHS | F9 | 79 | 18 | Exchange TOS and NOS. |
| XCHD | B9 | 39 | 26 | |
| XCHF | 99 | 19 | 26 | |
| PUPI | 9A | 1A | 16 | Push floating point constant $\pi$ onto TOS. Previous TOS becomes NOS. |

**Figure 8.**

often based on some form of polynomial equation, such as:

$$F(X) = A_0 + A_1X + A_2X^2 + A_3X^3 + A_4X^4 \ldots . \quad (1\text{-}1)$$

The primary shortcoming of an approximation in this form is that it typically exhibits very large errors when the magnitude of | X | is large, although the errors are small when | X | is small. With polynomials in this form, the error distribution is markedly uneven over any arbitrary interval.

Fortunately, a set of approximating functions exists that not only minimizes the maximum error but also provides an even distribution of errors within the selected data representation interval. These are known as Chebyshev Polynomials and are based upon cosine functions.[1,2] These functions are defined as follows:

$$T_n(X) = \text{Cos } n\theta; \text{ where } n = 0,1,2 \ldots \quad (1\text{-}2)$$
$$\theta = \text{Cos}^{-1}X$$

The various terms of the Chebyshev series can be computed as shown below:

$$T_0(X) = \text{Cos } (0 \cdot \theta) = \text{Cos } (0) = 1 \quad (1\text{-}4)$$
$$T_1(X) = \text{Cos } (\text{Cos}^{-1}X) = X \quad (1\text{-}5)$$
$$T_2(X) = \text{Cos } 2\theta = 2\text{Cos}^2\,\theta - 1 = 2\text{Cos}^2\,(\text{Cos}^{-1}X) - 1 \quad (1\text{-}6)$$
$$= 2X^2 - 1$$

In general, the next term in the Chebyshev series can be recursively derived from the previous term as follows:

$$T_n(X) = 2X\,[T_n{-}1(X)] - T_n{-}2\,(X);\ n \geq 2 \quad (1\text{-}7)$$

The terms $T_3$, $T_4$, $T_5$ and $T_6$ are given below for reference:

$$T_3 = 4X^3 - 3X \quad (1\text{-}8)$$
$$T_4 = 8X^4 - 8X^2 + 1 \quad (1\text{-}9)$$
$$T_5 = 16X^5 - 20X^3 + 5X \quad (1\text{-}10)$$
$$T_6 = 32X^6 - 48X^4 + 18X^2 - 1 \quad (1\text{-}11)$$

Chebyshev polynomials can be directly substituted for corresponding terms of a power series expansion by simple algebraic manipulation:

$$1 = T_0 \quad (1\text{-}12)$$
$$X = T_1 \quad (1\text{-}13)$$
$$X^2 = 1/2\,(T_0 + T_2) \quad (1\text{-}14)$$
$$X^3 = 1/4\,(3T_1 + T_3) \quad (1\text{-}15)$$
$$X^4 = 1/8\,(3T_0 + 4T_2 + T_4) \quad (1\text{-}16)$$
$$X^5 = 1/16\,(10T_1 + 5T_3 + T_5) \quad (1\text{-}17)$$
$$X^6 = 1/32\,(10T_0 + 15T_2 + 6T_4 + T_6) \quad (1\text{-}18)$$

Each of the derived functions except square root implemented in the Am9511 APU has been reduced to Chebyshev polynomial form. A sufficient number of terms has been used to provide a mean relative error of about one part in $10^7$.

Each of the functions is implemented as a three-step process. The first step involves range reduction. That is, the input argument to the function is transformed to fall within a range of values for which the function can compute a valid result. For example, since functions like sine and cosine are periodic for multiples of $\pi/2$ radians, input arguments for these functions are converted to lie within the range of $-\pi/2$ to $+\pi/2$. Processing of the range-reduced input argument according to the appropriate Chebyshev expansion is done in the second step. The third step includes any necessary post processing of the result, such as sign correction in sine or cosine for a particular quadrant. Range reduction and post processing are unique to each of the functions, while processing the Chebyshev expansion is performed by an algorithm that is common to all functions.

true function, results computed by the Am9511 are not always exact. In order to more comprehensively quantify the error performance of the component, the following graphs have been prepared. Each function has been executed with a statistically significant number of diverse data values, spanning the allowable input data range, and resulting errors have been tabulated. Absolute errors (that is, the number of bits in error) have been converted to relative errors according to the following equation:

$$\text{Relative Error} = \frac{\text{Absolute Error}}{\text{True Result}}$$

This conversion permits the error to be viewed with respect to the magnitude of the true result. This provides a more objective measurement of error performance since it directly translates to a measure of significant digits of algorithm accuracy.

For example, if a given absolute error is 0.001 and the true result is also 0.001, it is clear that the relative error is equal to 1.0 (which implies that even the first significant digit of the result is wrong). However, if the same absolute error is computed for a true result of 10000.0, then the first six significant digits of the result are correct (0.001/10000 = 0.0000001).

Each of the following graphs was prepared to illustrate relative algorithm error as a function of input data range. Natural Logarithm is the only exception; since logarithms are typically additive, absolute error is plotted for this function.

Two graphs have not been included in the following figures: common logarithms and the power function ($X^Y$). Common logarithms are computed by multiplication of the natural logarithm by the conversion factor 0.43429448 and the error function is therefore the same as that for natural logarithm. The power function is realized by combination of natural log and exponential functions according to the equation:

$$X^Y = e^{Y\text{Ln}x}$$

The error for the power function is a combination of that for the logarithm and exponential functions. Specifically, the relative error for PWR is expressed as follows:

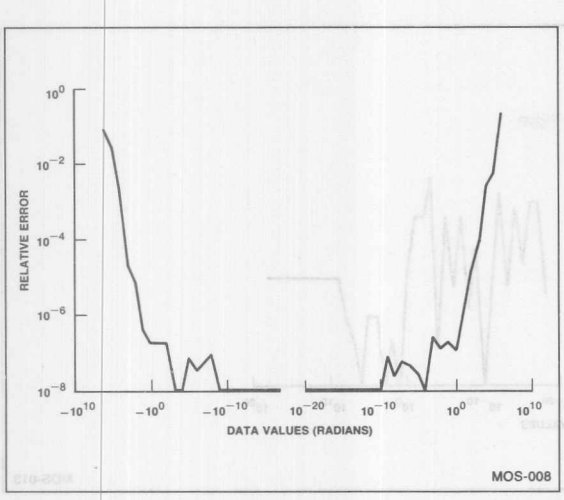
$$|RE_{PWR}| = |RE_{EXP}| + |X\,(AE_{LN})|$$

where:

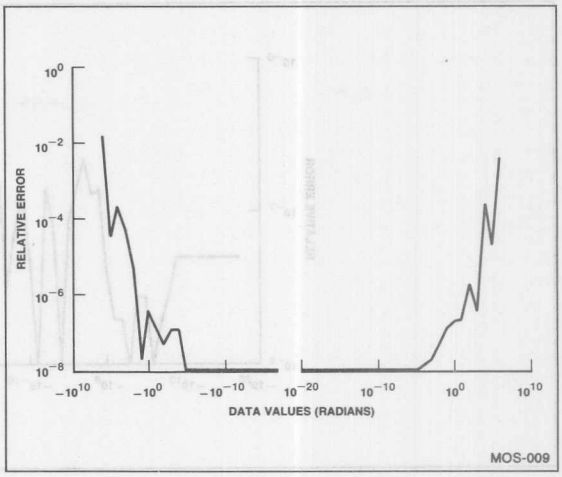
$RE_{PWR}$ = relative error for power function
$RE_{EXP}$ = relative error for exponential function
$AE_{LN}$ = absolute error for natural logarithm
$X$ = value of independent variable in $X^Y$

Notes:

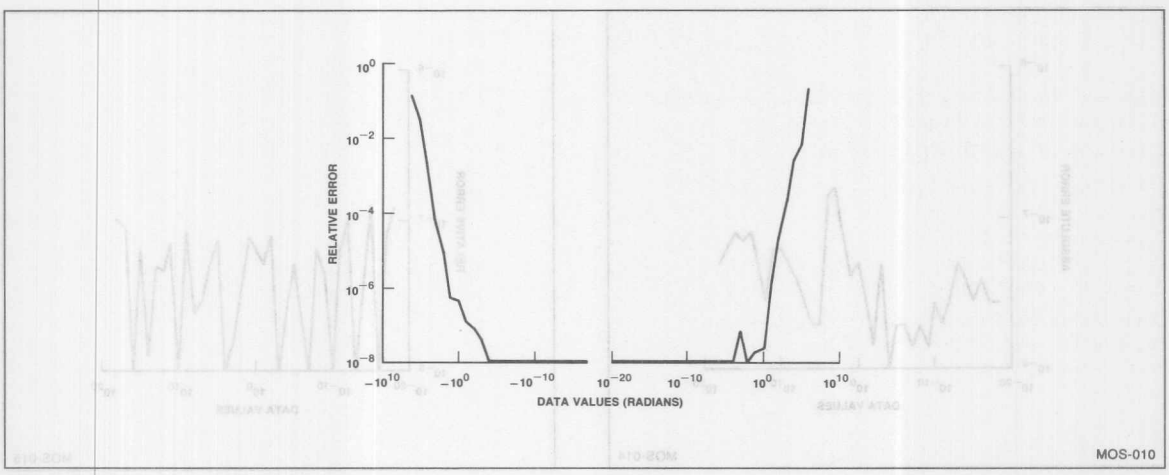
1. Properties of Chebyshev polynomials taken from: Applied Numerical Methods; Carnahan, Luther, Wikes; John Wiley & Sons, Inc.; 1969.
2. Derived function algorithms adapted from: Algorithms for Special Functions (I and II); Numerische Mathematic (1963); Clenshaw, Miller, Woodger.



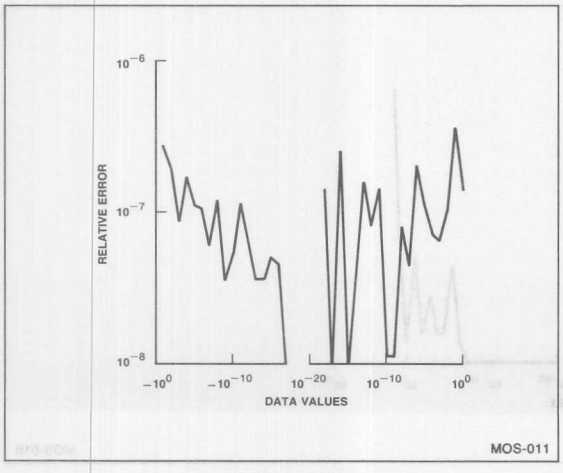

SINE



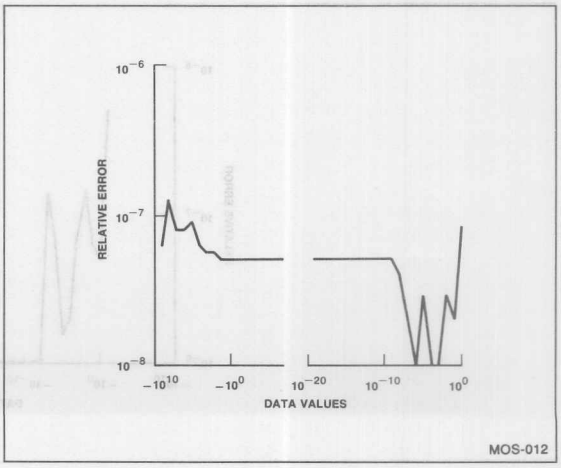

COSINE




TANGENT

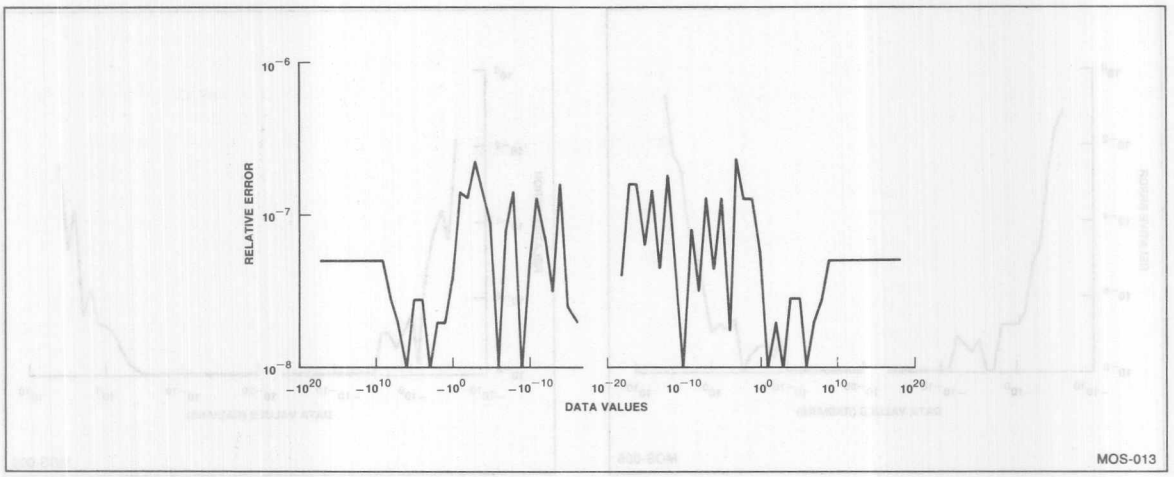



INVERSE SINE

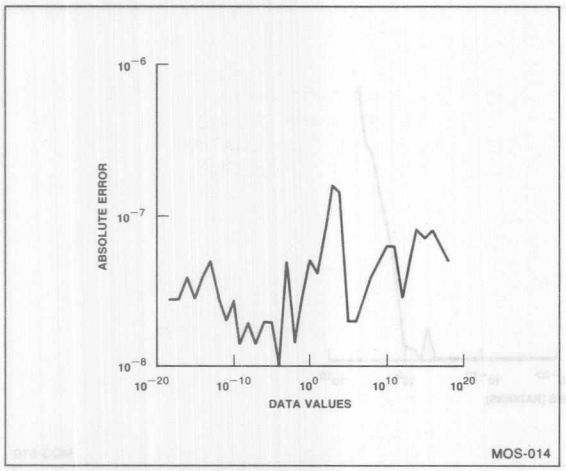



INVERSE COSINE

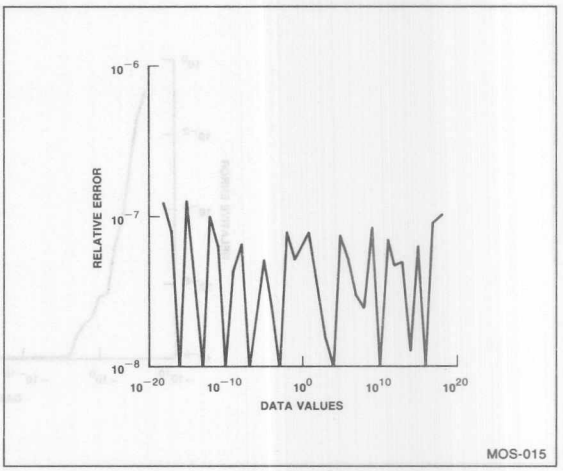
9



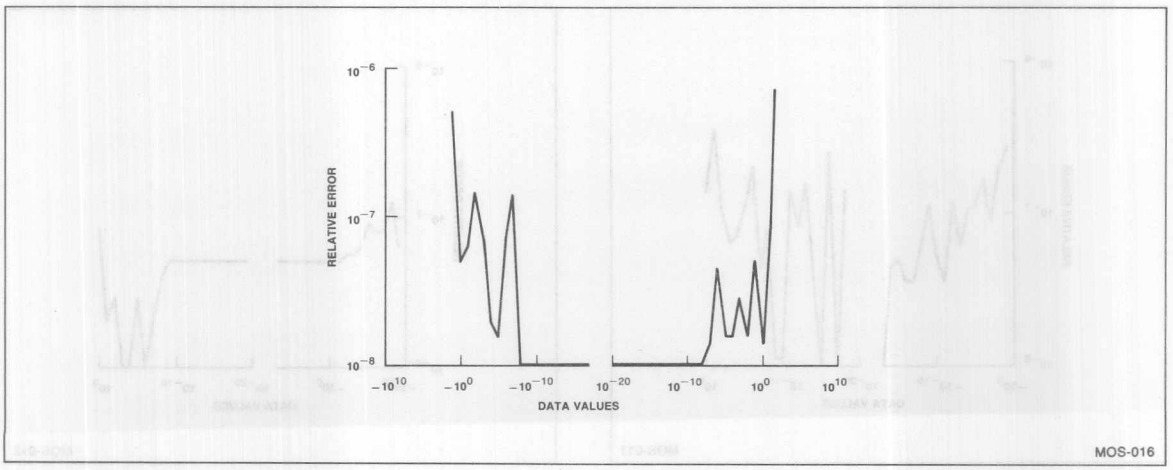

**INVERSE TANGENT**




**NATURAL LOG**




**SQUARE ROOT**




**$e^x$**

## COMMAND DESCRIPTIONS

This section contains detailed descriptions of the APU commands. They are arranged in alphabetical order by command mnemonic. In the descriptions, TOS means Top Of Stack and NOS means Next On Stack.

All derived functions except Square Root use Chebyshev polynomial approximating algorithms. This approach is used to help minimize the internal microprogram, to minimize the maximum error values and to provide a relatively even distribution of errors over the data range. The basic arithmetic operations are used by the derived functions to compute the various Chebyshev terms. The basic operations may produce error codes in the status register as a result.

Execution times are listed in terms of clock cycles and may be converted into time values by multiplying by the clock period used. For example, an execution time of 44 clock cycles when running at a 3MHz rate translates to 14 microseconds (44 x 32$\mu$s = 14$\mu$s). Variations in execution cycles reflect the data dependency of the algorithms.

In some operations exponent overflow or underflow may be possible. When this occurs, the exponent returned in the result will be 128 greater or smaller than its true value.

Many of the functions use portions of the data stack as scratch storage during development of the results. Thus previous values in those stack locations will be lost. Scratch locations destroyed are listed in the command descriptions and shown with the crossed-out locations in the Stack Contents After diagram.

Figure 8 is a summary of all the Am9511 commands. It shows the hex codes for each command, the mnemonic abbreviation, a brief description and the execution time in clock cycles. The commands are grouped by functional classes.

Figure 9 lists the command mnemonics in alphabetical order.

| | | | |
|---|---|---|---|
| ACOS | ARCCOSINE | LOG | COMMON LOGARITHM |
| ASIN | ARCSINE | LN | NATURAL LOGARITHM |
| ATAN | ARCTANGENT | NOP | NO OPERATION |
| CHSD | CHANGE SIGN DOUBLE | POPD | POP STACK DOUBLE |
| CHSF | CHANGE SIGN FLOATING | POPF | POP STACK FLOATING |
| CHSS | CHANGE SIGN SINGLE | POPS | POP STACK SINGLE |
| COS | COSINE | PTOD | PUSH STACK DOUBLE |
| DADD | DOUBLE ADD | PTOF | PUSH STACK FLOATING |
| DDIV | DOUBLE DIVIDE | PTOS | PUSH STACK SINGLE |
| DMUL | DOUBLE MULTIPLY LOWER | PUPI | PUSH $\pi$ |
| DMUU | DOUBLE MULTIPLY UPPER | PWR | POWER ($X^Y$) |
| DSUB | DOUBLE SUBTRACT | SADD | SINGLE ADD |
| EXP | EXPONENTIATION ($e^x$) | SDIV | SINGLE DIVIDE |
| FADD | FLOATING ADD | SIN | SINE |
| FDIV | FLOATING DIVIDE | SMUL | SINGLE MULTIPLY LOWER |
| FIXD | FIX DOUBLE | SMUU | SINGLE MULTIPLY UPPER |
| FIXS | FIX SINGLE | SQRT | SQUARE ROOT |
| FLTD | FLOAT DOUBLE | SSUB | SINGLE SUBTRACT |
| FLTS | FLOAT SINGLE | TAN | TANGENT |
| FMUL | FLOATING MULTIPLY | XCHD | EXCHANGE OPERANDS DOUBLE |
| FSUB | FLOATING SUBTRACT | XCHF | EXCHANGE OPERANDS FLOATING |
| | | XCHS | EXCHANGE OPERANDS SINGLE |

**Figure 9. Command Mnemonics in Alphabetical Order.**

# ACOS

## 32-BIT FLOATING-POINT INVERSE COSINE

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

**Hex Coding:** 86 with sr = 1
06 with sr = 0

**Execution Time:** 6304 to 8284 clock cycles

**Description:**

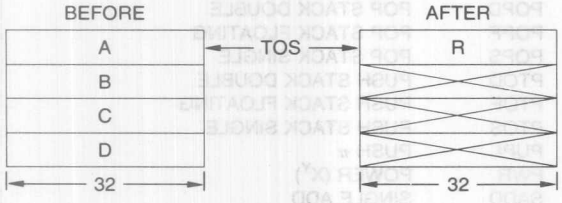
The 32-bit floating-point operand A at the TOS is replaced by the 32-bit floating-point inverse cosine of A. The result R is a value in radians between 0 and $\pi$. Initial operands A, B, C and D are lost.

ACOS will accept all input data values within the range of $-1.0$ to $+1.0$. Values outside this range will return an error code of 1100 in the status register.

**Accuracy:** ACOS exhibits a maximum relative error of $2.0 \times 10^{-7}$ over the valid input data range.

**Status Affected:** Sign, Zero, Error Field

**STACK CONTENTS**




# ATAN

## 32-BIT FLOATING-POINT INVERSE TANGENT

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

**Hex Coding:** 87 with sr = 1
07 with sr = 0

**Execution Time:** 4992 to 6536 clock cycles

**Description:**

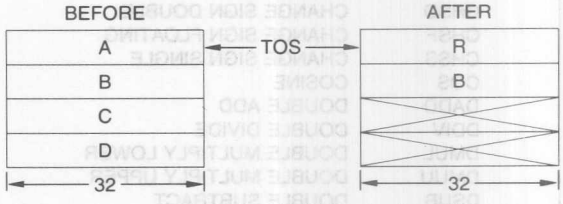
The 32-bit floating-point operand A at the TOS is replaced by the 32-bit floating-point inverse tangent of A. The result R is a value in radians between $-\pi/2$ and $+\pi/2$. Initial operands A, C and D are lost. Operand B is unchanged.

ATAN will accept all input data values that can be represented in the floating point format.

**Accuracy:** ATAN exhibits a maximum relative error of $3.0 \times 10^{-7}$ over the input data range.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




# ASIN

## 32-BIT FLOATING-POINT INVERSE SINE

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

**Hex Coding:** 85 with sr = 1
05 with sr = 0

**Execution Time:** 6230 to 7938 clock cycles

**Description:**

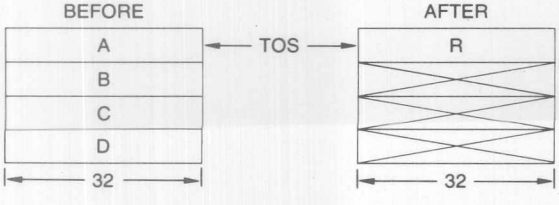
The 32-bit floating-point operand A at the TOS is replaced by the 32-bit floating-point inverse sine of A. The result R is a value in radians between $-\pi/2$ and $+\pi/2$. Initial operands A, B, C and D are lost.

ASIN will accept all input data values within the range of $-1.0$ to $+1.0$. Values outside this range will return an error code of 1100 in the status register.

**Accuracy:** ASIN exhibits a maximum relative error of $4.0 \times 10^{-7}$ over the valid input data range.

**Status Affected:** Sign, Zero, Error Field

**STACK CONTENTS**




# CHSD

## 32-BIT FIXED-POINT SIGN CHANGE

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 1 | 1 | 0 | 1 | 0 | 0 |

**Hex Coding:** B4 with sr = 1
34 with sr = 0

**Execution Time:** 26 to 28 clock cycles

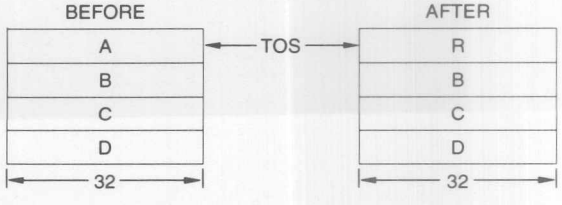
**Description:**

The 32-bit fixed-point two's complement integer operand A at the TOS is subtracted from zero. The result R replaces A at the TOS. Other entries in the stack are not disturbed.

Overflow status will be set and the TOS will be returned unchanged when A is input as the most negative value possible in the format since no positive equivalent exists.

**Status Affected:** Sign, Zero, Error Field (overflow)

**STACK CONTENTS**



# CHSF

## 32-BIT FLOATING-POINT SIGN CHANGE

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 0 | 1 | 0 | 1 |

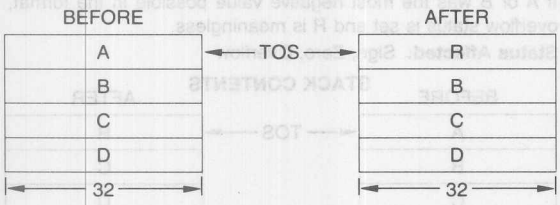
**Hex Coding:** 95 with sr = 1
15 with sr = 0

**Execution Time:** 16 to 20 clock cycles

**Description:**
The sign of the mantissa of the 32-bit floating-point operand A at the TOS is inverted. The result R replaces A at the TOS. Other stack entries are unchanged.
If A is input as zero (mantissa MSB = 0), no change is made.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




# CHSS

## 16-BIT FIXED-POINT SIGN CHANGE

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 1 | 1 | 1 | 0 | 1 | 0 | 0 |

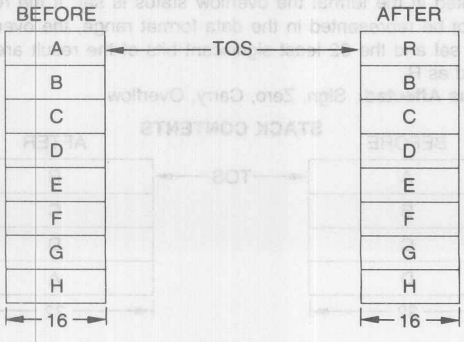
**Hex Coding:** F4 with sr = 1
74 with sr = 0

**Execution Time:** 22 to 24 clock cycles

**Description:**
16-bit fixed-point two's complement integer operand A at the TOS is subtracted from zero. The result R replaces A at the TOS. All other operands are unchanged.
Overflow status will be set and the TOS will be returned unchanged when A is input as the most negative value possible in the format since no positive equivalent exists.

**Status Affected:** Sign, Zero, Overflow

**STACK CONTENTS**




# COS

## 32-BIT FLOATING-POINT COSINE

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

**Hex Coding:** 83 with sr = 1
03 with sr = 0

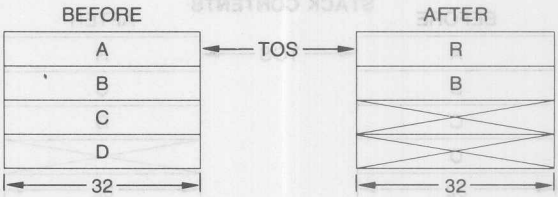
**Execution Time:** 3840 to 4878 clock cycles

**Description:**
The 32-bit floating-point operand A at the TOS is replaced by R, the 32-bit floating-point cosine of A. A is assumed to be in radians. Operands A, C and D are lost. B is unchanged.
The COS function can accept any input data value that can be represented in the data format. All input values are range reduced to fall within an interval of $-\pi/2$ to $+\pi/2$ radians.

**Accuracy:** COS exhibits a maximum relative error of 5.0 x $10^{-7}$ for all input data values in the range of $-2\pi$ to $+2\pi$ radians.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




# DADD

## 32-BIT FIXED-POINT ADD

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 1 | 0 | 1 | 1 | 0 | 0 |

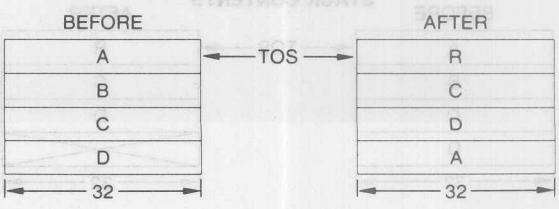
**Hex Coding:** AC with sr = 1
2C with sr = 0

**Execution Time:** 20 to 22 clock cycles

**Description:**
The 32-bit fixed-point two's complement integer operand A at the TOS is added to the 32-bit fixed-point two's complement integer operand B at the NOS. The result R replaces operand B and the Stack is moved up so that R occupies the TOS. Operand B is lost. Operands A, C and D are unchanged. If the addition generates a carry it is reported in the status register.
If the result is too large to be represented by the data format, the least significant 32 bits of the result are returned and overflow status is reported.

**Status Affected:** Sign, Zero, Carry, Error Field

**STACK CONTENTS**




9

# DDIV

## 32-BIT FIXED-POINT DIVIDE

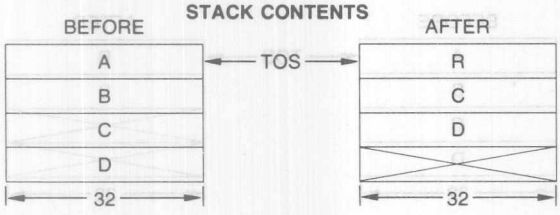
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 1 | 0 | 1 | 1 | 1 | 1 |

**Hex Coding:** AF with sr = 1
2F with sr = 0

**Execution Time:** 196 to 210 clock cycles when A ≠ 0
18 clock cycles when A = 0.

**Description:**
The 32-bit fixed-point two's complement integer operand B at NOS is divided by the 32-bit fixed-point two's complement integer operand A at the TOS. The 32-bit integer quotient R replaces B and the stack is moved up so that R occupies the TOS. No remainder is generated. Operands A and B are lost. Operands C and D are unchanged.
If A is zero, R is set equal to B and the divide-by-zero error status will be reported. If either A or B is the most negative value possible in the format, R will be meaningless and the overflow error status will be reported.

**Status Affected:** Sign, Zero, Error Field




# DMUL

## 32-BIT FIXED-POINT MULTIPLY, LOWER

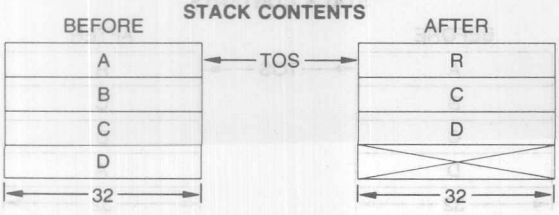
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 1 | 0 | 1 | 1 | 1 | 0 |

**Hex Coding:** AE with sr = 1
2E with sr = 0

**Execution Time:** 194 to 210 clock cycles

**Description:**
The 32-bit fixed-point two's complement integer operand A at the TOS is multiplied by the 32-bit fixed-point two's complement integer operand B at the NOS. The 32-bit least significant half of the product R replaces B and the stack is moved up so that R occupies the TOS. The most significant half of the product is lost. Operands A and B are lost. Operands C and D are unchanged.
The overflow status bit is set if the discarded upper half was non-zero. If either A or B is the most negative value that can be represented in the format, that value is returned as R and the overflow status is set.

**Status Affected:** Sign, Zero, Overflow




# DMUU

## 32-BIT FIXED-POINT MULTIPLY, UPPER

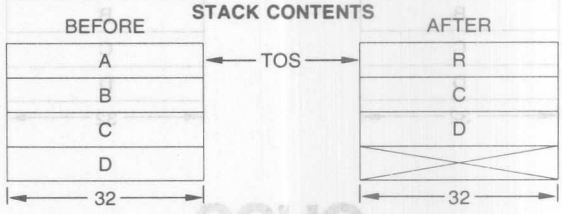
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 1 | 1 | 0 | 1 | 1 | 0 |

**Hex Coding:** B6 with sr = 1
36 with sr = 0

**Execution Time:** 182 to 218 clock cycles

**Description:**
The 32-bit fixed-point two's complement integer operand A at the TOS is multiplied by the 32-bit fixed-point two's complement integer operand B at the NOS. The 32-bit most significant half of the product R replaces B and the stack is moved up so that R occupies the TOS. The least significant half of the product is lost. Operands A and B are lost. Operands C and D are unchanged.
If A or B was the most negative value possible in the format, overflow status is set and R is meaningless.

**Status Affected:** Sign, Zero, Overflow




# DSUB

## 32-BIT FIXED-POINT SUBTRACT

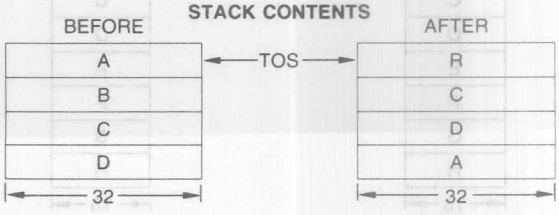
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 1 | 0 | 1 | 1 | 0 | 1 |

**Hex Coding:** AD with sr = 1
2D with sr = 0

**Execution Time:** 38 to 40 clock cycles

**Description:**
The 32-bit fixed-point two's complement operand A at the TOS is subtracted from the 32-bit fixed-point two's complement operand B at the NOS. The difference R replaces operand B and the stack is moved up so that R occupies the TOS. Operand B is lost. Operands A, C and D are unchanged.
If the subtraction generates a borrow it is reported in the carry status bit. If A is the most negative value that can be represented in the format the overflow status is set. If the result cannot be represented in the data format range, the overflow bit is set and the 32 least significant bits of the result are returned as R.

**Status Affected:** Sign, Zero, Carry, Overflow



# EXP

## 32-BIT FLOATING-POINT $e^X$

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

**Hex Coding:** 8A with sr = 1
0A with sr = 0

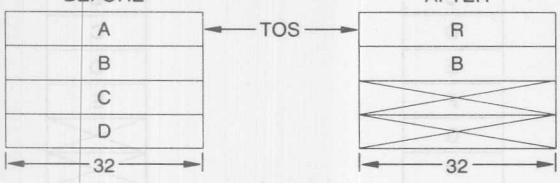
**Execution Time:** 3794 to 4878 clock cycles for $|A| \leq 1.0 \times 2^5$
34 clock cycles for $|A| > 1.0 \times 2^5$

**Description:**
The base of natural logarithms, e, is raised to an exponent value specified by the 32-bit floating-point operand A at the TOS. The result R of $e^A$ replaces A. Operands A, C and D are lost. Operand B is unchanged.
EXP accepts all input data values within the range of $-1.0 \times 2^{+5}$ to $+1.0 \times 2^{+5}$. Input values outside this range will return a code of 1100 in the error field of the status register.

**Accuracy:** EXP exhibits a maximum relative error of $5.0 \times 10^{-7}$ over the valid input data range.

**Status Affected:** Sign, Zero, Error Field

**STACK CONTENTS**




# FADD

## 32-BIT FLOATING-POINT ADD

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

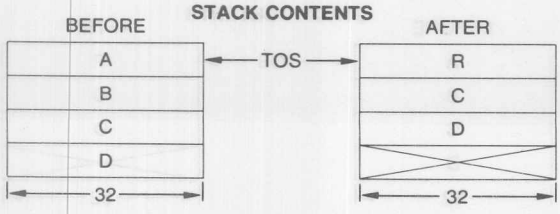
**Hex Coding:** 90 with sr = 1
10 with sr = 0

**Execution Time:** 54 to 368 clock cycles for A ≠ 0
24 clock cycles for A = 0

**Description:**
32-bit floating-point operand A at the TOS is added to 32-bit floating-point operand B at the NOS. The result R replaces B and the stack is moved up so that R occupies the TOS. Operands A and B are lost. Operands C and D are unchanged.
Exponent alignment before the addition and normalization of the result accounts for the variation in execution time. Exponent overflow and underflow are reported in the status register, in which case the mantissa is correct and the exponent is offset by 128.

**Status Affected:** Sign, Zero, Error Field

**STACK CONTENTS**




# FDIV

## 32-BIT FLOATING-POINT DIVIDE

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 0 | 0 | 1 | 1 |

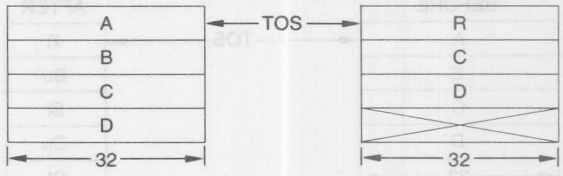
**Hex Coding:** 93 with sr = 1
13 with sr = 0

**Execution Time:** 154 to 184 clock cycles for A ≠ 0
22 clock cycles for A = 0

**Description:**
32-bit floating-point operand B at NOS is divided by 32-bit floating-point operand A at the TOS. The result R replaces B and the stack is moved up so that R occupies the TOS. Operands A and B are lost. Operands C and D are unchanged.
If operand A is zero, R is set equal to B and the divide-by-zero error is reported in the status register. Exponent overflow or underflow is reported in the status register, in which case the mantissa portion of the result is correct and the exponent portion is offset by 128.

**Status Affected:** Sign, Zero, Error Field

**STACK CONTENTS**




# FIXD

## 32-BIT FLOATING-POINT TO 32-BIT FIXED-POINT CONVERSION

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 1 | 1 | 1 | 0 |

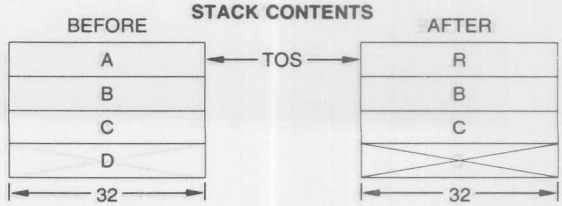
**Hex Coding:** 9E with sr = 1
1E with sr = 0

**Execution Time:** 90 to 336 clock cycles

**Description:**
32-bit floating-point operand A at the TOS is converted to a 32-bit fixed-point two's complement integer. The result R replaces A. Operands A and D are lost. Operands B and C are unchanged.
If the integer portion of A is larger than 31 bits when converted, the overflow status will be set and A will not be changed. Operand D, however, will still be lost.

**Status Affected:** Sign, Zero Overflow

**STACK CONTENTS**




9

# FIXS

## 32-BIT FLOATING-POINT TO 16-BIT FIXED-POINT CONVERSION

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

**Hex Coding:** 9F with sr = 1
1F with sr = 0

**Execution Time:** 90 to 214 clock cycles

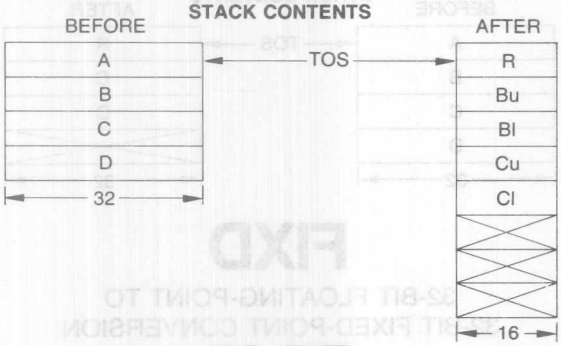
**Description:**

32-bit floating-point operand A at the TOS is converted to a 16-bit fixed-point two's complement integer. The result R replaces the lower half of A and the stack is moved up by two bytes so that R occupies the TOS. Operands A and D are lost. Operands B and C are unchanged, but appear as upper (u) and lower (l) halves on the 16-bit wide stack if they are 32-bit operands.

If the integer portion of A is larger than 15 bits when converted, the overflow status will be set and A will not be changed. Operand D, however, will still be lost.

**Status Affected:** Sign, Zero, Overflow

**STACK CONTENTS**




# FLTD

## 32-BIT FIXED-POINT TO 32-BIT FLOATING-POINT CONVERSION

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 1 | 1 | 0 | 0 |

**Hex Coding:** 9C with sr = 1
1C with sr = 0

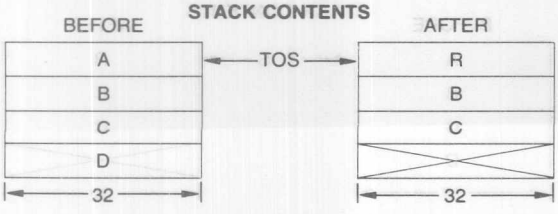
**Execution Time:** 56 to 342 clock cycles

**Description:**

32-bit fixed-point two's complement integer operand A at the TOS is converted to a 32-bit floating-point number. The result R replaces A at the TOS. Operands A and D are lost. Operands B and C are unchanged.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




# FLTS

## 16-BIT FIXED-POINT TO 32-BIT FLOATING-POINT CONVERSION

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 1 | 1 | 0 | 1 |

**Hex Coding:** 9D with sr = 1
1D with sr = 0

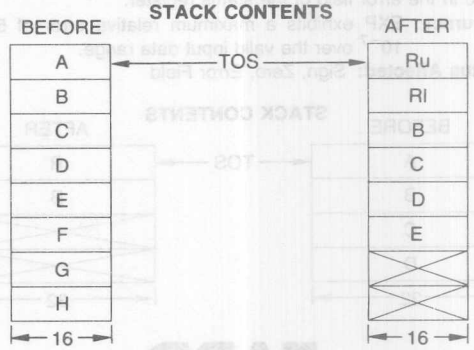
**Execution Time:** 62 to 156 clock cycles

**Description:**

16-bit fixed-point two's complement integer A at the TOS is converted to a 32-bit floating-point number. The lower half of the result R (Rl) replaces A, the upper half (Ru) replaces H and the stack is moved down so that Ru occupies the TOS. Operands A, F, G and H are lost. Operands B, C, D and E are unchanged.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




# FMUL

## 32-BIT FLOATING-POINT MULTIPLY

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 0 | 0 | 1 | 0 |

**Hex Coding:** 92 with sr = 1
12 with sr = 0

**Execution Time:** 146 to 168 clock cycles

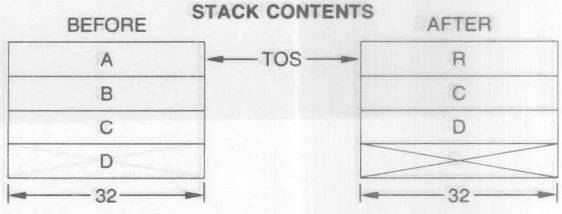
**Description:**

32-bit floating-point operand A at the TOS is multiplied by the 32-bit floating-point operand B at the NOS. The normalized result R replaces B and the stack is moved up so that R occupies the TOS. Operands A and B are lost. Operands C and D are unchanged.

Exponent overflow or underflow is reported in the status register, in which case the mantissa portion of the result is correct and the exponent portion is offset by 128.

**Status Affected:** Sign, Zero, Error Field

**STACK CONTENTS**



# FSUB

## 32-BIT FLOATING-POINT SUBTRACTION

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

**Hex Coding:** 91 with sr = 1
11 with sr = 0

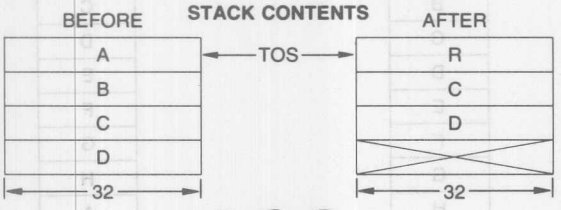
**Execution Time:** 70 to 370 clock cycles for A ≠ 0
26 clock cycles for A = 0

**Description:**
32-bit floating-point operand A at the TOS is subtracted from 32-bit floating-point operand B at the NOS. The normalized difference R replaces B and the stack is moved up so that R occupies the TOS. Operands A and B are lost. Operands C and D are unchanged.

Exponent alignment before the subtraction and normalization of the result account for the variation in execution time.

Exponent overflow or underflow is reported in the status register in which case the mantissa portion of the result is correct and the exponent portion is offset by 128.

**Status Affected:** Sign, Zero, Error Field (overflow)




# LOG

## 32-BIT FLOATING-POINT COMMON LOGARITHM

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

**Hex Coding:** 88 with sr = 1
08 with sr = 0

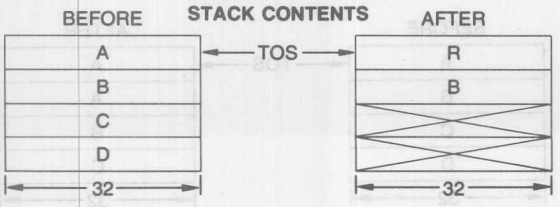
**Execution Time:** 4474 to 7132 clock cycles for A > 0
20 clock cycles for A ≤ 0

**Description:**
The 32-bit floating-point operand A at the TOS is replaced by R, the 32-bit floating-point common logarithm (base 10) of A. Operands A, C and D are lost. Operand B is unchanged.

The LOG function accepts any positive input data value that can be represented by the data format. If LOG of a non-positive value is attempted an error status of 0100 is returned.

**Accuracy:** LOG exhibits a maximum absolute error of $2.0 \times 10^{-7}$ for the input range from 0.1 to 10, and a maximum relative error of $2.0 \times 10^{-7}$ for positive values less than 0.1 or greater than 10.

**Status Affected:** Sign, Zero, Error Field




# LN

## 32-BIT FLOATING-POINT NATURAL LOGARITHM

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 0 | 1 | 0 | 0 | 1 |

**Hex Coding:** 89 with sr = 1
09 with sr = 0

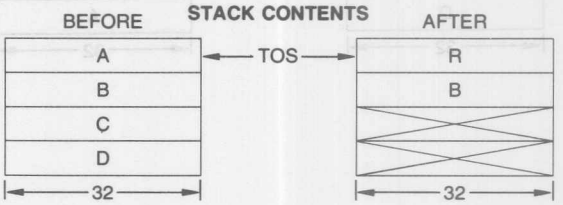
**Execution Time:** 4298 to 6956 clock cycles for A > 0
20 clock cycles for A≤ 0

**Description:**
The 32-bit floating-point operand A at the TOS is replaced by R, the 32-bit floating-point natural logarithm (base e) of A. Operands A, C and D are lost. Operand B is unchanged.

The LN function accepts all positive input data values that can be represented by the data format. If LN of a non-positive number is attempted an error status of 0100 is returned.

**Accuracy:** LN exhibits a maximum absolute error of $2 \times 10^{-7}$ for the input range from $e^{-1}$ to e, and a maximum relative error of $2.0 \times 10^{-7}$ for positive values less than $e^{-1}$ or greater than e.

**Status Affected:** Sign, Zero, Error Field




# NOP

## NO OPERATION

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Hex Coding:** 80 with sr = 1
00 with sr = 0

**Execution Time:** 4 clock cycles

**Description:**
The NOP command performs no internal data manipulations. It may be used to set or clear the service request interface line without changing the contents of the stack.

**Status Affected:** The status byte is cleared to all zeroes.

9

# POPD

## 32-BIT STACK POP

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 1 | 1 | 1 | 0 | 0 | 0 |

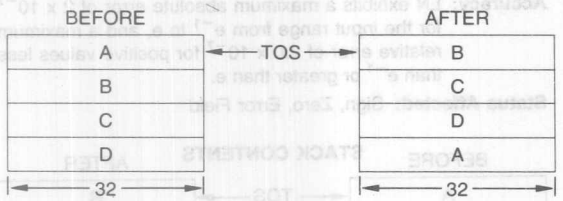
**Hex Coding:** B8 with sr = 1
38 with sr = 0

**Execution Time:** 12 clock cycles

**Description:**
The 32-bit stack is moved up so that the old NOS becomes the new TOS. The previous TOS rotates to the bottom of the stack. All operand values are unchanged. POPD and POPF execute the same operation.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




# POPS

## 16-BIT STACK POP

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 1 | 1 | 1 | 1 | 0 | 0 | 0 |

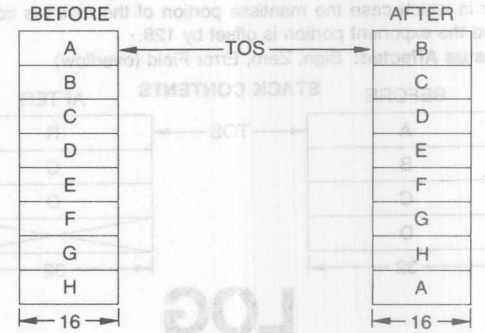
**Hex Coding:** F8 with sr = 1
78 with sr = 0

**Execution Time:** 10 clock cycles

**Description:**
The 16-bit stack is moved up so that the old NOS becomes the new TOS. The previous TOS rotates to the bottom of the stack. All operand values are unchanged.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




# POPF

## 32-BIT STACK POP

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

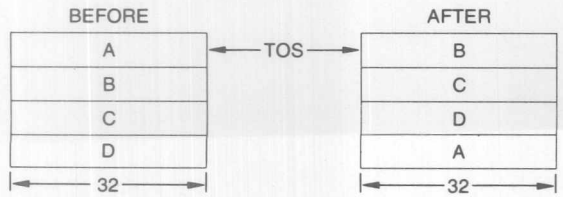
**Hex Coding:** 98 with sr = 1
18 with sr = 0

**Execution Time:** 12 clock cycles

**Description:**
The 32-bit stack is moved up so that the old NOS becomes the new TOS. The old TOS rotates to the bottom of the stack. All operand values are unchanged. POPF and POPD execute the same operation.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




# PTOD

## PUSH 32-BIT TOS ONTO STACK

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 1 | 1 | 0 | 1 | 1 | 1 |

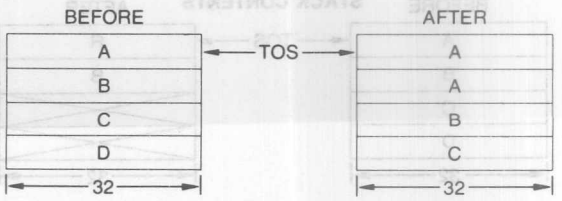
**Hex Coding:** B7 with sr = 1
37 with sr = 0

**Execution Time:** 20 clock cycles

**Description:**
The 32-bit stack is moved down and the previous TOS is copied into the new TOS location. Operand D is lost. All other operand values are unchanged. PTOD and PTOF execute the same operation.

**Status Affected:** Sign, Zero

**STACK CONTENTS**



# PTOF

## PUSH 32-BIT TOS ONTO STACK

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 0 | 1 | 1 | 1 |

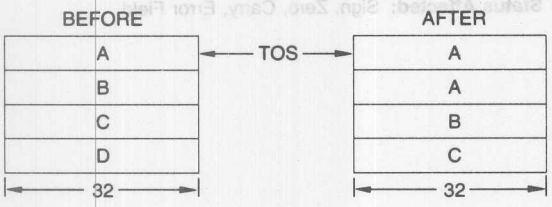
**Hex Coding:** 97 with sr = 1
17 with sr = 0

**Execution Time:** 20 clock cycles

**Description:**
The 32-bit stack is moved down and the previous TOS is copied into the new TOS location. Operand D is lost. All other operand values are unchanged. PTOF and PTOD execute the same operation.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




# PTOS

## PUSH 16-BIT TOS ONTO STACK

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 1 | 1 | 1 | 0 | 1 | 1 | 1 |

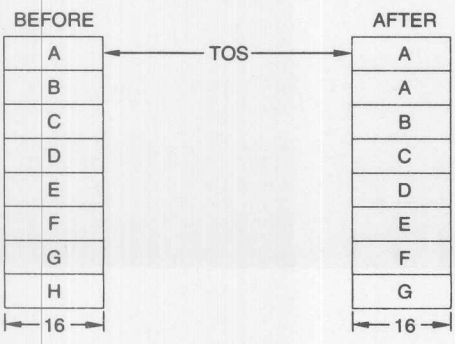
**Hex Coding:** F7 with sr = 1
77 with sr = 0

**Execution Time:** 16 clock cycles

**Description:**
The 16-bit stack is moved down and the previous TOS is copied into the new TOS location. Operand H is lost and all other operand values are unchanged.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




# PUPI

## PUSH 32-BIT FLOATING-POINT $\pi$

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 1 | 0 | 1 | 0 |

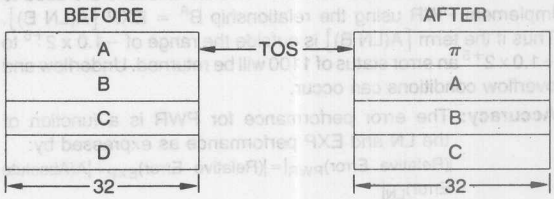
**Hex Coding:** 9A with sr = 1
1A with sr = 0

**Execution Time:** 16 clock cycles

**Description:**
The 32-bit stack is moved down so that the previous TOS occupies the new NOS location. 32-bit floating-point constant $\pi$ is entered into the new TOS location. Operand D is lost. Operands A, B and C are unchanged.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




9

# PWR

## 32-BIT FLOATING-POINT $X^Y$

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 0 | 1 | 0 | 1 | 1 |

**Hex Coding:** 8B with sr = 1
0B with sr = 0

**Execution Time:** 8290 to 12032 clock cycles

**Description:**

32-bit floating-point operand B at the NOS is raised to the power specified by the 32-bit floating-point operand A at the TOS. The result R of $B^A$ replaces B and the stack is moved up so that R occupies the TOS. Operands A, B, and D are lost. Operand C is unchanged.

The PWR function accepts all input data values that can be represented in the data format for operand A and all positive values for operand B. If operand B is non-positive an error status of 0100 will be returned. The EXP and LN functions are used to implement PWR using the relationship $B^A = EXP\,[A(LN\,B)]$. Thus if the term $[A(LN\,B)]$ is outside the range of $-1.0 \times 2^{+5}$ to $+1.0 \times 2^{+5}$ an error status of 1100 will be returned. Underflow and overflow conditions can occur.

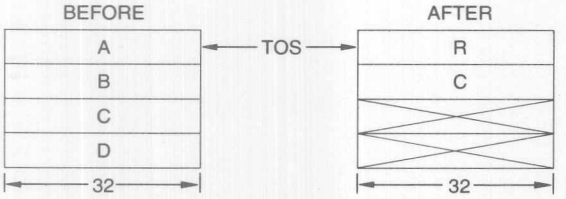
**Accuracy:** The error performance for PWR is a function of the LN and EXP performance as expressed by:

$$|(\text{Relative Error})_{PWR}| = |(\text{Relative Error})_{EXP} + |A(\text{Absolute Error})_{LN}|$$

The maximum relative error for PWR occurs when A is at its maximum value while $[A(LN\,B)]$ is near $1.0 \times 2^5$ and the EXP error is also at its maximum. For most practical applications the relative error for PWR will be less than $7.0 \times 10^{-7}$

**Status Affected:** Sign, Zero, Error Field

**STACK CONTENTS**




# SADD

## 16-BIT FIXED-POINT ADD

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 1 | 1 | 0 | 1 | 1 | 0 | 0 |

**Hex Coding:** EC with sr = 1
6C with sr = 0

**Execution Time:** 16 to 18 clock cycles

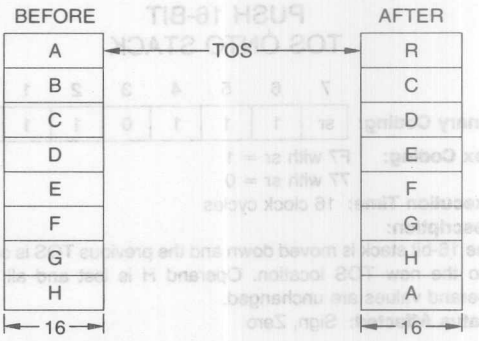
**Description:**

16-bit fixed-point two's complement integer operand A at the TOS is added to 16-bit fixed-point two's complement integer operand B at the NOS. The result R replaces B and the stack is moved up so that R occupies the TOS. Operand B is lost. All other operands are unchanged.

If the addition generates a carry bit it is reported in the status register. If an overflow occurs it is reported in the status register and the 16 least significant bits of the result are returned.

**Status Affected:** Sign, Zero, Carry, Error Field

**STACK CONTENTS**



# SDIV

## 16-BIT FIXED-POINT DIVIDE

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 1 | 1 | 0 | 1 | 1 | 1 | 1 |

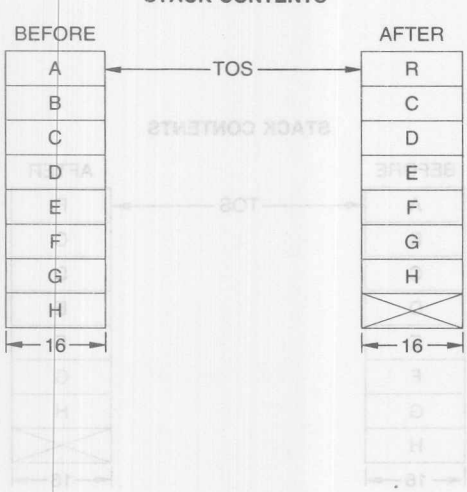
**Hex Coding:** EF with sr = 1
6F with sr = 0

**Execution Time:** 84 to 94 clock cycles for A ≠ 0
14 clock cycles for A = 0

**Description:**
16-bit fixed-point two's complement integer operand B at the NOS is divided by 16-bit fixed-point two's complement integer operand A at the TOS. The 16-bit integer quotient R replaces B and the stack is moved up so that R occupies the TOS. No remainder is generated. Operands A and B are lost. All other operands are unchanged.
If A is zero, R will be set equal to B and the divide-by-zero error status will be reported.

**Status Affected:** Sign, Zero, Error Field

**STACK CONTENTS**




# SIN

## 32-BIT FLOATING-POINT SINE

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

**Hex Coding:** 82 with sr = 1
02 with sr = 0

**Execution Time:** 3796 to 4808 clock cycles for $|A| > 2^{-12}$ radians
30 clock cycles for $|A| \leq 2^{-12}$ radians

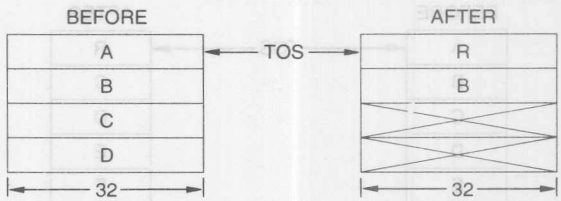
**Description:**
The 32-bit floating-point operand A at the TOS is replaced by R, the 32-bit floating-point sine of A. A is assumed to be in radians. Operands A, C and D are lost. Operand B is unchanged.

The SIN function will accept any input data value that can be represented by the data format. All input values are range reduced to fall within the interval $-\pi/2$ to $+\pi/2$ radians.

**Accuracy:** SIN exhibits a maximum relative error of 5.0 x $10^{-7}$ for input values in the range of $-2\pi$ to $+2\pi$ radians.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




9

# SMUL

## 16-BIT FIXED-POINT MULTIPLY, LOWER

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 1 | 1 | 0 | 1 | 1 | 1 | 0 |

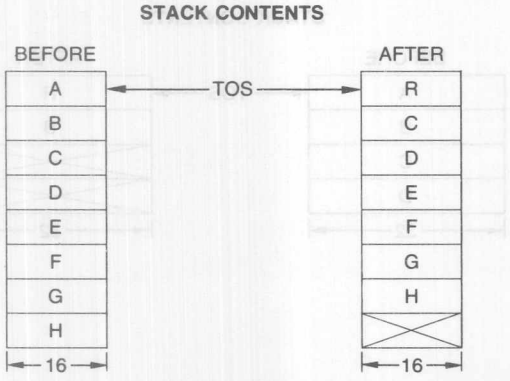
**Hex Coding:** EE with sr = 1
6E with sr = 0

**Execution Time:** 84 to 94 clock cycles

**Description:**

16-bit fixed-point two's complement integer operand A at the TOS is multiplied by the 16-bit fixed-point two's complement integer operand B at the NOS. The 16-bit least significant half of the product R replaces B and the stack is moved up so that R occupies the TOS. The most significant half of the product is lost. Operands A and B are lost. All other operands are unchanged. The overflow status bit is set if the discarded upper half was non-zero. If either A or B is the most negative value that can be represented in the format, that value is returned as R and the overflow status is set.

**Status Affected:** Sign, Zero, Error Field




# SMUU

## 16-BIT FIXED-POINT MULTIPLY, UPPER

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 1 | 1 | 1 | 0 | 1 | 1 | 0 |

**Hex Coding:** F6 with sr = 1
76 with sr. = 0

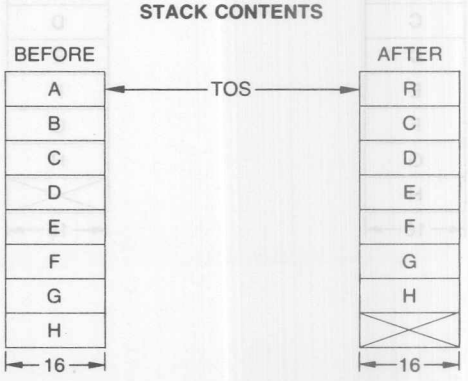
**Execution Time:** 80 to 98 clock cycles

**Description:**

16-bit fixed-point two's complement integer operand A at the TOS is multiplied by the 16-bit fixed-point two's complement integer operand B at the NOS. The 16-bit most significant half of the product R replaces B and the stack is moved up so that R occupies the TOS. The least significant half of the product is lost. Operands A and B are lost. All other operands are unchanged.

If either A or B is the most negative value that can be represented in the format, that value is returned as R and the overflow status is set.

**Status Affected:** Sign, Zero, Error Field



# SQRT

## 32-BIT FLOATING-POINT SQUARE ROOT

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

**Hex Coding:** 81 with sr = 1
01 with sr = 0

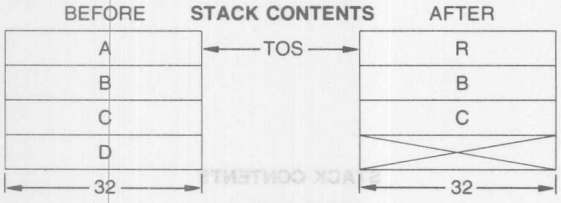
**Execution Time:** 782 to 870 clock cycles

**Description:**

32-bit floating-point operand A at the TOS is replaced by R, the 32-bit floating-point square root of A. Operands A and D are lost. Operands B and C are not changed.

SQRT will accept any non-negative input data value that can be represented by the data format. If A is negative an error code of 0100 will be returned in the status register.

**Status Affected:** Sign, Zero, Error Field




# SSUB

## 16-BIT FIXED-POINT SUBTRACT

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 1 | 1 | 0 | 1 | 1 | 0 | 1 |

**Hex Coding:** ED with sr = 1
6D with sr = 0

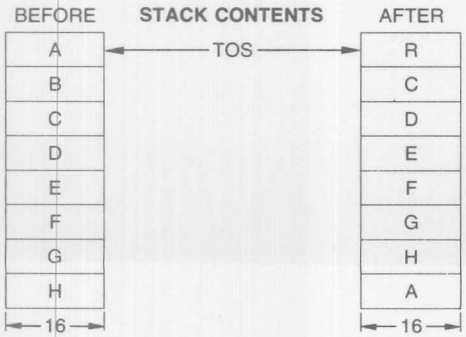
**Execution Time:** 30 to 32 clock cycles

**Description:**

16-bit fixed-point two's complement integer operand A at the TOS is subtracted from 16-bit fixed-point two's complement integer operand B at the NOS. The result R replaces B and the stack is moved up so that R occupies the TOS. Operand B is lost. All other operands are unchanged.

If the subtraction generates a borrow it is reported in the carry status bit. If A is the most negative value that can be represented in the format the overflow status is set. If the result cannot be represented in the format range, the overflow status is set and the 16 least significant bits of the result are returned as R.

**Status Affected:** Sign, Zero, Carry, Error Field




# TAN

## 32-BIT FLOATING-POINT TANGENT

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

**Hex Coding:** 84 with sr = 1
04 with sr = 0

**Execution Time:** 4894 to 5886 clock cycles for $|A| > 2^{-12}$ radians
30 clock cycles for $|A| \leq 2^{-12}$ radians

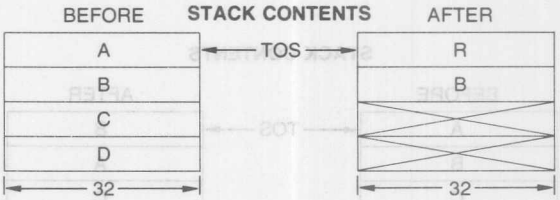
**Description:**

The 32-bit floating-point operand A at the TOS is replaced by the 32-bit floating-point tangent of A. Operand A is assumed to be in radians. A, C and D are lost. B is unchanged.

The TAN function will accept any input data value that can be represented in the data format. All input data values are range-reduced to fall within $-\pi/4$ to $+\pi/4$ radians. TAN is unbounded for input values near odd multiples of $\pi/2$ and in such cases the overflow bit is set in the status register. For angles smaller than $2^{-12}$ radians, TAN returns A as the tangent of A.

**Accuracy:** TAN exhibits a maximum relative error of $5.0 \times 10^{-7}$ for input data values in the range of $-2\pi$ to $+2\pi$ radians except for data values near odd multiples of $\pi/2$.

**Status Affected:** Sign, Zero, Error Field (overflow)




# XCHD

## EXCHANGE 32-BIT STACK OPERANDS

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 1 | 1 | 1 | 0 | 0 | 1 |

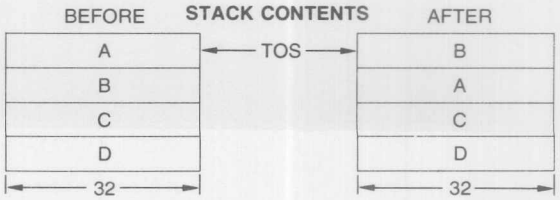
**Hex Coding:** B9 with sr = 1
39 with sr = 0

**Execution Time:** 26 clock cycles

**Description:**

32-bit operand A at the TOS and 32-bit operand B at the NOS are exchanged. After execution, B is at the TOS and A is at the NOS. All operands are unchanged. XCHD and XCHF execute the same operation.

**Status Affected:** Sign, Zero




9

## EXCHANGE 32-BIT STACK OPERANDS

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 0 | 0 | 1 | 1 | 0 | 0 | 1 |

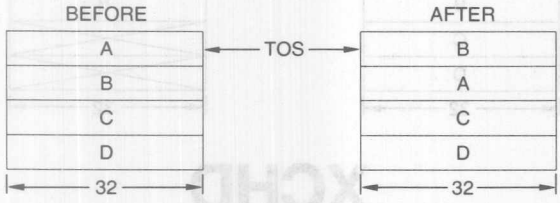
**Hex Coding:** 99 with sr = 1
19 with sr = 0

**Execution Time:** 26 clock cycles

**Description:**
32-bit operand A at the TOS and 32-bit operand B at the NOS are exchanged. After execution, B is at the TOS and A is at the NOS. All operands are unchanged. XCHD and XCHF execute the same operation.

**Status Affected:** Sign, Zero

**STACK CONTENTS**




## EXCHANGE 16-BIT STACK OPERANDS

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Binary Coding:** | sr | 1 | 1 | 1 | 1 | 0 | 0 | 1 |

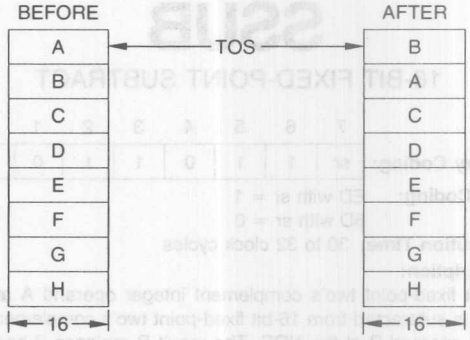
**Hex Coding:** F9 with sr = 1
79 with sr = 0

**Execution Time:** 18 clock cycles

**Description:**
16-bit operand A at the TOS and 16-bit operand B at the NOS are exchanged. After execution, B is at the TOS and A is at the NOS. All operand values are unchanged.

**Status Affected:** Sign, Zero

**STACK CONTENTS**



# Advanced Micro Devices

# Designing Interrupt Systems With the Am9519 Universal Interrupt Controller

By Joseph H. Kroeger

9

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AM-PUB071

## TABLE OF CONTENTS


I INTRODUCTION
- General ..... 9-51
- Features ..... 9-51

II HARDWARE INTERFACE
- Block Diagram ..... 9-52
- Interface Signal Description ..... 9-52
- Interface Considerations ..... 9-53
- IREQ Timing ..... 9-54
- Power Supply ..... 9-55

III OPERATING DESCRIPTION
- Reset ..... 9-56
- Register Description ..... 9-56
- Information Transfers ..... 9-58
- Operating Options ..... 9-58
- Operating Sequence ..... 9-60

IV COMMAND DESCRIPTIONS ..... 9-61

V SYSTEM INTERFACE
- Expansion ..... 9-64
- Initialization and Support ..... 9-65

## INTRODUCTION

### General

Processors exist as tools for the implementation of information system transfer functions. All useful processor systems include at least one peripheral device in order to communicate with the user of the system. The processor not only manipulates information once it is in the system, but also handles the transfer of information to and from the user via the peripherals. Often several devices are integral parts of the overall system. All peripherals must be serviced in one way or another by the system processor. The basic parameters that influence the design of peripheral servicing algorithms are the frequency of service required, the service latency allowed and the service duty cycle of the devices.

There are two general methods used to initiate and coordinate this activity: Program controlled service and Interrupt driven service. In program controlled transfers, the processor schedules all peripheral events; an Interrupt driven system, on the other hand, allows modification of the system activities by external devices.

With no interrupt capability, processors must depend on software polling techniques to service peripheral devices. As the number of such devices grows and/or as the complexity of service increases, the polling program becomes very time consuming and the overhead devoted to polling becomes a significant fraction of the available processing resource. When this limits system performance, the use of interrupts can often provide substantial improvement.

Interrupts are used to enhance processor system throughput and response time by minimizing or eliminating the need for software polling procedures. Interrupts are hardware mechanisms that allow devices external to the processor to asynchronously modify the instruction sequence of the processor program being executed. An elementary single interrupt could be used simply to alert the processor to the fact that some kind of service is desired and thus to initiate a polling routine. More complex systems may have multiple interrupts and vectoring protocols which can be used to further improve performance and eliminate all polling requirements. Vectoring allows direct identification of the interrupting device and its associated service routine.

Figure 1 illustrates the essential functioning of a typical interrupt procedure. As the main program is executing instructions, an external interrupt arrives, in this example during instruction M+2.The processor completes M+2 and then, instead of executing M+3, it performs some kind of interrupt acknowledge procedure, often involving execution of an additional interrupt instruction. The result will usually be that the address of instruction M+3 is saved for future reference, and the location of instruction N is determined. The processor then proceeds to execute the interrupt service routine starting with instruction N. The service routine may save, and later restore, the processor status as well as perform tasks requested by the interrupting device. The last instruction in the routine (N+K) directs the processor to resume the main program at instruction M+3.

Notice that the presence of the hardware interrupt has caused a modification of the sequence of instruction execution; an additional block of instructions has been inserted in the main program. Interrupts provide the system designer with a significant capability that can help optimize his cost/performance tradeoffs.

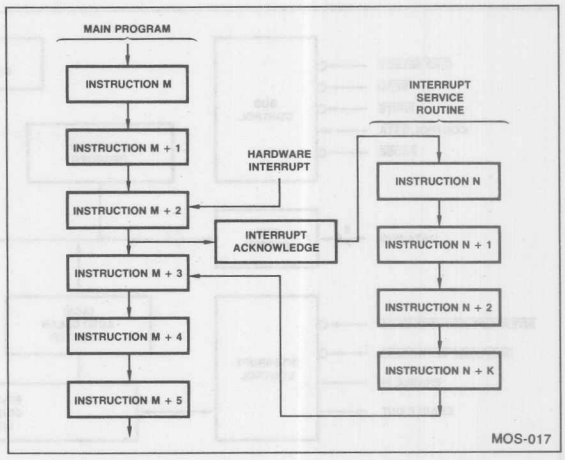



**Figure 1. Basic Interrupt Procedure.**

### Features

The Am9519 Universal Interrupt Controller is a processor support device designed to enhance the interrupt handling capability of a wide variety of processors. A single Am9519 manages the masking, priority resolution and vectoring of up to eight interrupts. It may be easily expanded by the addition of other Am9519 chips to handle a nearly unlimited set of interrupt inputs. It offers many programmable operating options to improve both the efficiency and versatility of its host system operations. The Am9519 is well adapted to a wide range of uses including small, simple, as well as large, sophisticated, interrupt systems.

The Am9519 provides any mix of one, two, three and four byte responses to the host processor during the interrupt acknowledge process. The response bytes are all fully programmable so that any appropriate addressing, vectoring, instruction or other message protocol may be used. Contention among multiple interrupts is managed internally using either fixed or rotating priority resolution circuitry. The direct vectoring capability of the Am9519 may be bypassed using the polled mode option.

An internal mask register permits individual interrupts to be disabled. It may be loaded in parallel by the host processor with any bit pattern, or mask bits may be individually controlled. The interrupt inputs use "pulse-catching" circuitry so that an external register is not needed to capture interrupt pulses. Narrow noise pulses, however, are ignored. The interrupt polarity may be selected as either active-high or active-low.

Another important feature of the Am9519 is its ability to generate software interrupts. The host processor can set interrupt requests under program control, thus permitting hardware to resolve the priority of software tasks. This is often a powerful system asset, especially for sophisticated operating software, as well as an aid for system testing, diagnostic, debugging and maintenance procedures.

The Am9519 is implemented with AMD's LINOX n-channel silicon gate MOS technology. This process features low profile structures, triple ion-implantation, both depletion and enhancement transistors, and small, low capacitance, low power, high speed circuitry. The chip contains 4,400 transistors within a total chip area of 28,765 square mils. It is packaged in a standard 28-pin dual in-line package.

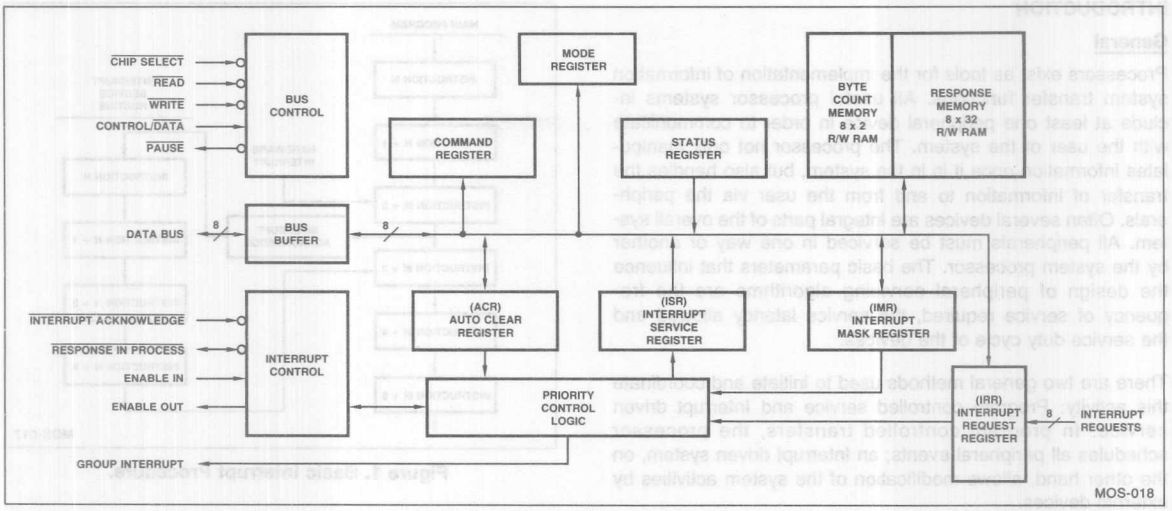



**Figure 2. Am9519 Block Diagram.**

## HARDWARE INTERFACE

### Block Diagram

The block diagram of the Am9519 shown in Figure 2 indicates the interface signals and the basic internal information flow. Interrupt Request inputs are captured and latched in the Interrupt Request register. Any requests not masked by the Interrupt Mask register will cause a Group Interrupt output to the host processor if the unit is enabled. When the processor is ready to handle the interrupt it issues an Interrupt Acknowledge pulse which causes (a) the priority of pending interrupts to be resolved and (b) a byte from the response memory associated with the highest priority interrupt to be transferred to the data bus. The transfer of additional response bytes is controlled by additional Interrupt Acknowledge signals. Other interrupt management functions are controlled by the Auto Clear register, the Interrupt Service register and the Mode register. Control of the Am9519 is exercised by the host processor using the Command register. The Status register reports on the internal condition of the part.

The Am9519 is addressed by the host processor as two distinct ports: a control port and a data port. The control port provides direct access to the Status register and the Command register. The data port is used to communicate with all other internal locations.

### Interface Signal Description

Figure 3 summarizes the interface signals. Figure 4 shows the interface signal pin assignments.

### Data Bus (DB)

The eight three-state bidirectional data bus lines are used to transfer information between the Am9519 and the system data bus. The direction of information flow is controlled by the $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ and $\overline{IACK}$ input signals. Data and command information are written into the device; status, data and response information are output by it.

| Description | Abbreviation | Type | Pins |
|---|---|---|---|
| +5 Volts | VCC | Power | 1 |
| Ground | VSS | Power | 1 |
| Data Bus | DB | I/O | 8 |
| Response In Process | RIP | I/O | 1 |
| Interrupt Request | IREQ | Input | 8 |
| Chip Select | CS | Input | 1 |
| Read | RD | Input | 1 |
| Write | WR | Input | 1 |
| Control/Data | C/D | Input | 1 |
| Interrupt Acknowledge | IACK | Input | 1 |
| Enable In | EI | Input | 1 |
| Enable Out | EO | Output | 1 |
| Group Interrupt | GINT | Output | 1 |
| Pause | PAUSE | Output | 1 |

**Figure 3. Am9519 Interface Signal Summary.**

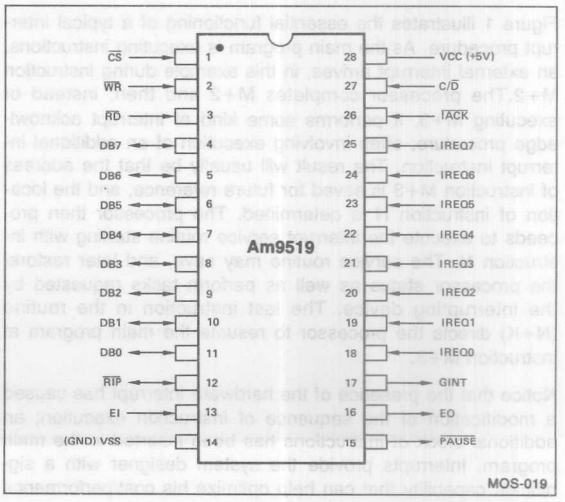



**Figure 4. Connection Diagram.**

**Chip Select ($\overline{CS}$)**

The Chip Select input is an active low signal used to condition the chip for read and write operations on the data bus; Read/Write transfers will not take place unless the $\overline{CS}$ input is low. Chip Select does not condition Interrupt Acknowledge operations. Chip Select is usually derived by decoding an address output by the host processor; the negative-true polarity matches outputs from typical decoder circuits.

**Read ($\overline{RD}$)**

The Read input is an active low signal conditioned by Chip Select that indicates information is to be transferred from the Am9519 to the data bus. Read is usually a timed pulse issued by the host processor.

**Write ($\overline{WR}$)**

The Write input is an active low signal conditioned by Chip Select that indicates information is to be transferred from the data bus to the Am9519. Write is usually a timed pulse issued by the host processor.

**Control/Data (C/$\overline{D}$)**

The Control/Data input acts as the port address line and is used to select source and destination locations for read and write transfers. Data transfers (C/$\overline{D}$=0) are made to or from preselected internal memory or register locations. Control transfers (C/$\overline{D}$=1) write into the command register or read from the status register.

**Interrupt Request (IREQ)**

The eight Interrupt Request inputs are used by external devices to indicate that service is desired. The Interrupt Request Register associated with the inputs uses asynchronous pulse-catching circuitry to latch any active requests that occur. The input polarity may be programmed to capture either positive-going or negative-going transitions. Reset selects the active low option.

**Response In Process ($\overline{RIP}$)**

The Response In Process signal is a bidirectional line designed to be used when two or more Am9519 circuits are connected together. $\overline{RIP}$ is used to prevent new higher priority interrupts from interferring with an Interrupt Acknowledge process that is underway. An Am9519 that is responding to a selected interrupt will treat $\overline{RIP}$ as an output and will hold the signal low until the acknowledge response is complete. An Am9519 without a selected interrupt will treat $\overline{RIP}$ as an input and will ignore $\overline{IACK}$ pulses as long as $\overline{RIP}$ is low. The $\overline{RIP}$ lines from multiple Am9519 circuits may be wired directly together. $\overline{RIP}$ is an open drain signal, and requires an external pullup resistor to VCC in order to establish the logic high level.

**Group Interrupt (GINT)**

When active, the Group Interrupt output indicates that at least one bit is set in the Interrupt Request Register (IRR) which is not masked by the Interrupt Mask Register or the Interrupt Service Register. GINT is used to notify the host processor that service is desired. It may be programmed for either active high or active low polarity in order to simplify the interface with the host circuitry. Reset selects active low. When active high is selected the output is a standard two-state buffer configuration. When active low is selected the output is open drain and requires an external pullup resistor to VCC in order to establish the logic high level. The open drain configuration is useful for wired-or connections in systems with more than one Am9519.

**Interrupt Acknowledge ($\overline{IACK}$)**

The Interrupt Acknowledge input is an active low signal generated by the host processor and used to request interrupt response information. One response byte will be transferred by the Am9519 for each $\overline{IACK}$ pulse received and up to four bytes may be transferred during each interrupt acknowledge sequence. The first $\overline{IACK}$ pulse following a GINT output also initiates the internal selection of the highest priority unmasked interrupt.

Many processors provide interrupt acknowledge signals directly, including the 8085, the 8080A and the 2650. For others, such as the Z80 and the 6800, it can be generated quite easily with simple gating.

**Pause**

The Pause output is an active low signal used during $\overline{IACK}$ cycles to indicate that the Am9519 has not completed the data bus transfer operation presently underway. The $\overline{IACK}$ pulse should be extended by the host processor at least until the $\overline{PAUSE}$ output goes high. The width of active $\overline{PAUSE}$ pulses is a function of several variables; it will be quite short in some systems and longer in others. $\overline{PAUSE}$ is an open drain output and requires an external pullup resistor to establish the high logic level. $\overline{PAUSE}$ signals should be wired together in multiple chip interrupt systems.

**Enable In (EI)**

The Enable In input is an active high signal used to implement a "daisy-chain" expansion capability with other Am9519 chips. EI may also be used as a hardware disable/enable input for the interrupt system. When EI is low, $\overline{IACK}$ inputs to the chip are ignored. Internally, a relatively high impedance resistor is connected between EI and VCC so that an unused EI requires no external pullup resistor.

**Enable Out (EO)**

The Enable Out output is an active high signal used to implement a "daisy-chain" expansion capability with other Am9519 chips. When the $\overline{IACK}$ input goes low, EO goes low until EI goes high and the chip determines that no unmasked request is pending. EO is a two-state output with relatively modest drive capability.

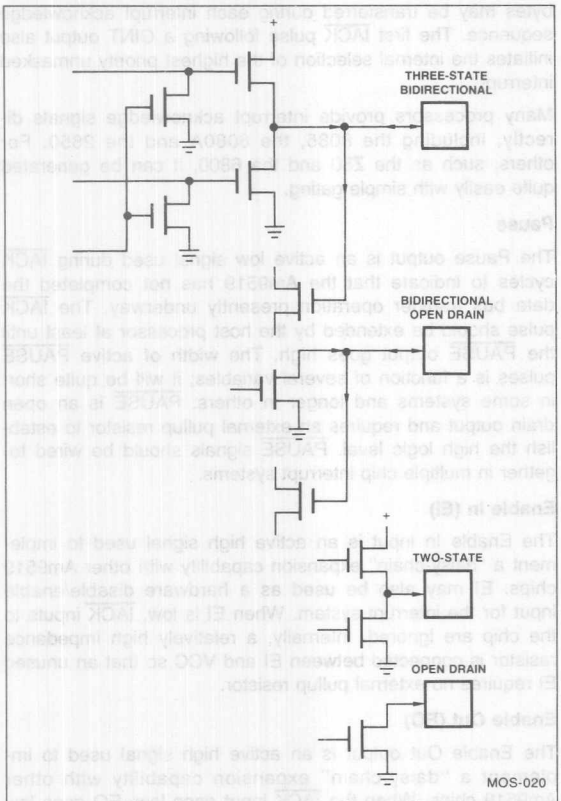
**Interface Considerations**

All of the input and output signals for the Am9519 are specified with logic levels identical to those of standard TTL circuits. The worst-case input logic levels are 2.0V high and 0.8V low. Except for the open drain signals, the worst-case output logic levels are 2.4V high and 0.4V low. Thus, for TTL interfacing, the normal worst-case noise immunity of at least 400mV is maintained. The logic level specifications take into account all combinations of the three variables that affect the logic level threshold: ambient temperature, supply voltage and processing parameters. A change in any of these toward nominal values will improve the actual operating margins.

The $\overline{PAUSE}$ and $\overline{RIP}$ outputs are open drain with no active pullup transistors; their output high levels are established by the external circuitry. The GINT output, when programmed for active low polarity ($\overline{GINT}$), is also an open drain output that does not control its output high level.

All of the output buffers except EO and the open drain outputs can source at least 200$\mu$A worst-case and can sink at least 3.2mA worst-case while maintaining TTL output logic levels. EO normally only drives EI of another Am9519 chip and is specified with less drive capability in order to improve the

priority resolution speed in multi-chip interrupt systems. The open drain outputs all sink at least 3.2mA as the other outputs do. Current sourcing for the open drain outputs is determined by the external circuitry. Figure 5 summarizes the types of outputs on the Am9519.




| Signal | Output Description |
|---|---|
| Data Bus (DB0-DB7) | Bidirectional, Three-State |
| Response In Process (RIP) | Bidirectional, Open-drain |
| Pause | Open-drain |
| Group Interrupt (GINT) | Two-State when active high<br>Open-Drain when active low |
| Enable Out (EO) | Two-state, low drive |

**Figure 5. Am9519 Output Buffer Summary and Circuitry.**

Unprotected open gate inputs of high quality MOS transistors exhibit very high resistances on the order of $10^{14}$ ohms. It is easy in many circumstances for charge to enter the gate node of such an input faster than it can be discharged and consequently for the gate voltage to rise high enough to break down the oxides and destroy the transistor. All inputs to the Am9519 include protection networks to help prevent damaging accumulations of static charge. The protection circuitry is designed to slow the transitions of incoming current surges and to provide low impedance discharge paths for voltages beyond the normal operating levels. Please note, however, that input energy levels can nonetheless be too high to be successfully absorbed. Conventional design, storage, and handling precautions should be observed so that the protection networks themselves are not overstressed.

Within the limits of normal operation, the input protection circuitry is inactive and may be modeled as a lumped series RC as shown in Figure 6. The functionally active input connection during normal operation is the gate of an MOS transistor. Except for EI, no active sources or drains are connected to the inputs so that neither transient nor steady-state currents are impressed on the driving signals by the Am9519 other than the charging or discharging of the input capacitance and the accumulated leakage associated with the protection network and the input circuit. Lumped input capacitances are usually around 6pF and leakage currents are usually less than 1$\mu$A.

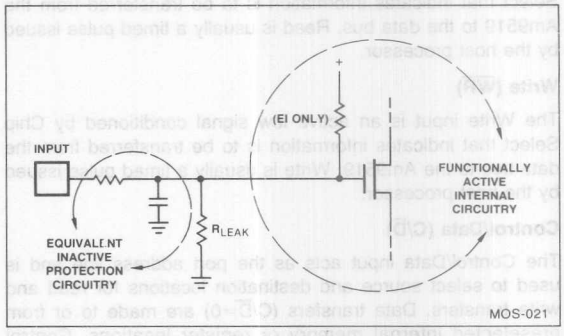



**Figure 6. Input Circuitry.**

Fanout from the driving circuitry into the Am9519 inputs will generally be limited by transition time considerations rather than DC current limitations when the loading is dominated by MOS circuits like the Am9519. In an operating environment, all inputs should be terminated so they do not float and accumulate stray static charges. Unused inputs should be tied directly to Ground or to VCC, as appropriate. An input in use will have some type of logic output driving it and termination during operation will not be a problem. Where inputs are driven from logic external to the card containing this chip, however, on-board termination should be provided to protect the chip when the board is unplugged and the input would otherwise float. A pull-up resistor or a simple inverter or gate will suffice.

### IREQ Timing

The circuitry at the IREQ inputs is quite straightforward and is illustrated in Figure 7. Inverters 1 and 2 buffer the input and shift the logic voltages to the somewhat wider swing used internally. The exclusive-or gate is used to select the sense of the active transition edge that will set the IRR. Mode register bit M4 is used directly for control of the exclusive-or gate. The selected interface edge will always produce a negative going transition at output 3. Inverters 4, 5, 6, 7 and 8 form a delay chain. Nor gate 9 has three inputs and the IRR bit will be set when all three inputs to 9 are low. As shown in the timing diagram of Figure 8, the input to gate 9 from inverter 8 is normally low when there is no active IREQ signal at the interface. When a transition occurs, the output of gate 3 will go low and only the signal from inverter 5 prevents the immediate setting of the IRR bit. As shown in the left portion of the timing diagram, if the output from 3 has returned high before the output from 5 goes low, the IREQ transition will be ignored and the IRR bit will not be set. On the other hand, the right side of the timing diagram shows that if the active IREQ input is present long enough, then the output from both 3 and 5 will become low at the same time, and output 9 will go high. Output 8 is used to turn off Nor gate 9 after the IRR bit is set.

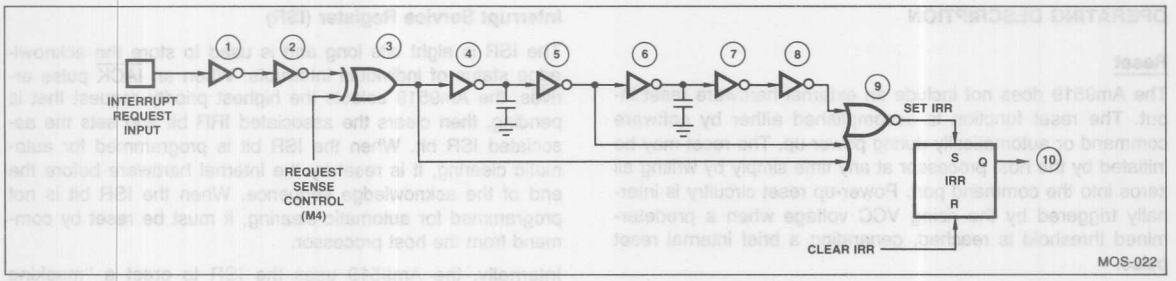



**Figure 7. Interrupt Request Logic.**

In summary, the input circuitry for the IREQ signals provides these characteristics:

1. Polarity for IREQ inputs is controlled;
2. Narrow IREQ pulses are ignored;
3. Wide IREQ pulses are captured;
4. Transitions to active levels are captured just once;
5. New transitions are required to generate new interrupts.

The IRR thus acts in a "pulse-catching" mode with respect to the IREQ inputs. Figure 9 shows the types of IREQ waveforms that will be recognized and latched by the IRR. Note that a transition to a level may be used although only a pulse is required; it is not necessary to maintain an IREQ input active level. Further, a continuously active level on IREQ will not cause a new interrupt each time IRR is cleared. There must be a new active transition on IREQ after IRR is cleared in order to generate a new interrupt. An active level must go inactive for a specific interval before its new active edge will be recognized.

To minimize noise sensitivity, all active IREQ pulses narrower than a specific value will be ignored by the IRR. To maintain the pulse-catching characteristics, all active IREQ pulses wider than the specified data sheet minimum will be captured by the IRR. The results for intermediate pulse widths will depend on characteristics of the particular part being used and its operating conditions, especially temperature.

## Power Supply

The Am9519 requires only a single +5V power supply. The commercial temperature range parts have a voltage tolerance of ±5%; the military temperature range tolerance is ±10%. Maximum supply currents are specified in the data sheet at the high end of the voltage tolerance and the low end of the temperature range. In addition, the current specifications take into account the worst-case distribution of processing parameters that may be encountered during the manufacturing life of the product. Typical supply current values, on the other hand, are specified for a nominal supply of +5.0 volts, nominal ambient temperature of 25°C, and nominal processing parameters. Supply current always decreases with increasing ambient temperature; thermal run-away is not a problem.

Although supply current will vary from part to part, a given unit at a given operating temperature will exhibit a nearly constant power drain. There is no functional operating region that will cause more than a few percent change in the supply current. Decoupling of VCC, then, is straightforward and will generally be used simply to isolate the Am9519 from external VCC noise.

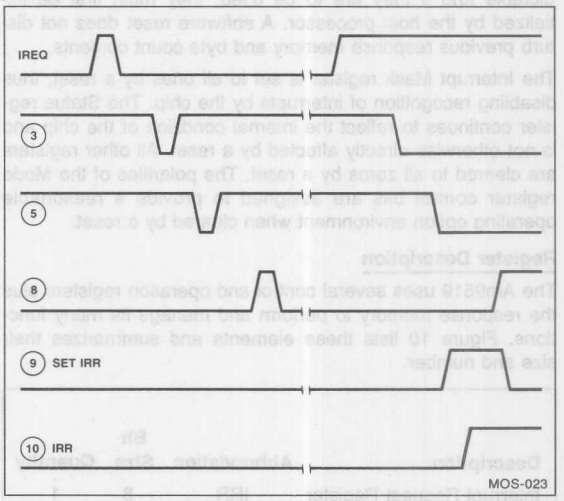



**Figure 8. IREQ Internal Timing.**

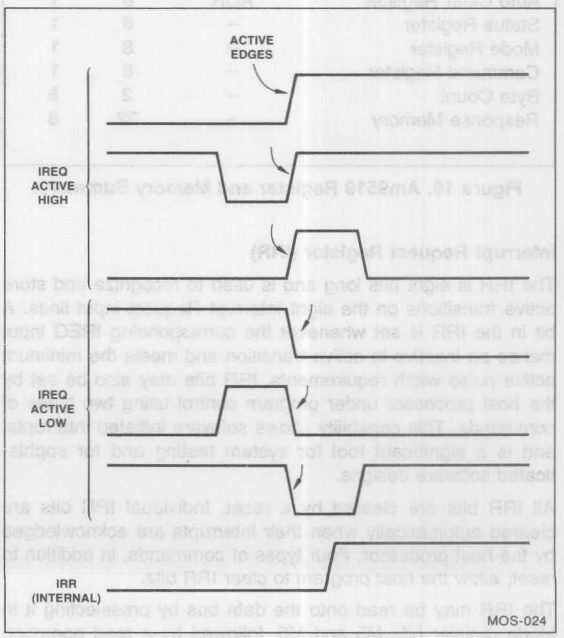



**Figure 9. IREQ Waveforms.**

9

## OPERATING DESCRIPTION

### Reset

The Am9519 does not include an external hardware reset input. The reset function is accomplished either by software command or automatically during power-up. The reset may be initiated by the host processor at any time simply by writing all zeros into the command port. Power-up reset circuitry is internally triggered by the rising VCC voltage when a predetermined threshold is reached, generating a brief internal reset pulse.

The response memory and byte count registers are not affected by resets. Their content after power-up are unpredictable and if they are to be used, they must first be initialized by the host processor. A software reset does not disturb previous response memory and byte count contents.

The Interrupt Mask register is set to all ones by a reset, thus disabling recognition of interrupts by the chip. The Status register continues to reflect the internal condition of the chip and is not otherwise directly affected by a reset. All other registers are cleared to all zeros by a reset. The polarities of the Mode register control bits are assigned to provide a reasonable operating option environment when cleared by a reset.

### Register Description

The Am9519 uses several control and operation registers plus the response memory to perform and manage its many functions. Figure 10 lists these elements and summarizes their size and number.

| Description | Abbreviation | Bit Size | Quantity |
|---|---|---|---|
| Interrupt Request Register | IRR | 8 | 1 |
| Interrupt Service Register | ISR | 8 | 1 |
| Interrupt Mask Register | IMR | 8 | 1 |
| Auto Clear Register | ACR | 8 | 1 |
| Status Register | – | 8 | 1 |
| Mode Register | – | 8 | 1 |
| Command Register | – | 8 | 1 |
| Byte Count | – | 2 | 8 |
| Response Memory | – | 32 | 8 |

**Figure 10. Am9519 Register and Memory Summary.**

#### Interrupt Request Register (IRR)

The IRR is eight bits long and is used to recognize and store active transitions on the eight Interrupt Request input lines. A bit in the IRR is set whenever the corresponding IREQ input makes an inactive-to-active transition and meets the minimum active pulse width requirements. IRR bits may also be set by the host processor under program control using two types of commands. This capability allows software initiated interrupts, and is a significant tool for system testing and for sophisticated software designs.

All IRR bits are cleared by a reset. Individual IRR bits are cleared automatically when their interrupts are acknowledged by the host processor. Four types of commands, in addition to reset, allow the host program to clear IRR bits.

The IRR may be read onto the data bus by preselecting it in Mode register bits M5 and M6, followed by a read operation at the data port.

#### Interrupt Service Register (ISR)

The ISR is eight bits long and is used to store the acknowledge status of individual interrupts. When an $\overline{IACK}$ pulse arrives, the Am9519 selects the highest priority request that is pending, then clears the associated IRR bit and sets the associated ISR bit. When the ISR bit is programmed for automatic clearing, it is reset by the internal hardware before the end of the acknowledge sequence. When the ISR bit is not programmed for automatic clearing, it must be reset by command from the host processor.

Internally, the Am9519 uses the ISR to erect a "masking fence". When an ISR bit is set and fixed priority mode is selected, only requests of higher priority will cause a new GINT output. Thus, requests from lower priority interrupts (and from new requests associated with the set ISR bit) will be fenced out and ignored until the ISR bit is cleared. In the rotating priority mode, all requests are fenced by an ISR bit that is set, and no new GINT outputs will be generated until the ISR is cleared. When auto clear is specified, no fence is erected since the ISR bit is cleared.

If an unmasked interrupt arrives from a device of higher priority than the current ISR, GINT will go true and the host processor will be interrupted if its interrupt input is enabled. When the new interrupt is acknowledged, the associated higher priority ISR bit is set and the fence moves up to the new level. When the new ISR bit is cleared, the fence will then fall back to the previous ISR level.

The ISR may be read onto the data bus by preselecting it in Mode register bits M5 and M6, followed by a read operation at the data port.

#### Interrupt Mask Register (IMR)

The IMR is eight bits long and is used to enable/disable the processing of individual interrupts. Only unmasked IRR bits can cause a Group Interrupt to be generated. The IMR does not otherwise affect the operation of the IRR. An IRR bit that is set while masked will cause a GINT when its IMR bit is cleared.

All eight IMR bits may be set, cleared, read or loaded in parallel by the host processor. In addition, individual IMR bits may be set or cleared by command. This allows a control routine to directly enable and disable an individual interrupt without disturbing the other mask bits and without knowledge of their state or the system context.

The IMR polarity is active high for masking; a zero enables the interrupt and a one disables it. The power-on reset and the software reset cause all IMR bits to be set, thus disabling all requests.

#### Auto Clear Register (ACR)

The ACR is eight bits long and specifies the automatic clearing option for each of the ISR bits. When an auto clear bit is set, the corresponding ISR bit that has been set in an $\overline{IACK}$ cycle is cleared by the internal hardware before the end of the $\overline{IACK}$ sequence. When an auto clear bit is not set, the corresponding ISR bit that has been set in an $\overline{IACK}$ cycle is cleared by command from the host processor.

The auto clear option, when selected, provides two concomitant functional effects. First, it eliminates the need for the associated interrupt service routine to issue a command to clear the ISR bit. Secondly, it eliminates the masking fence that would otherwise have been erected, allowing lower priority interrupts to cause a new GINT output.

The ACR is loaded in parallel from the data bus by issuing the ACR load preselect command followed by a write into the data port. The ACR may be read onto the data bus by preselecting it in Mode register bits M5 and M6, followed by a read operation at the data port.

### Status Register

The Status Register is eight bits long and contains information describing the internal state of the Am9519 chip. The Status register is read directly by executing a read operation at the control port. Figure 11 shows the Status bit assignments.

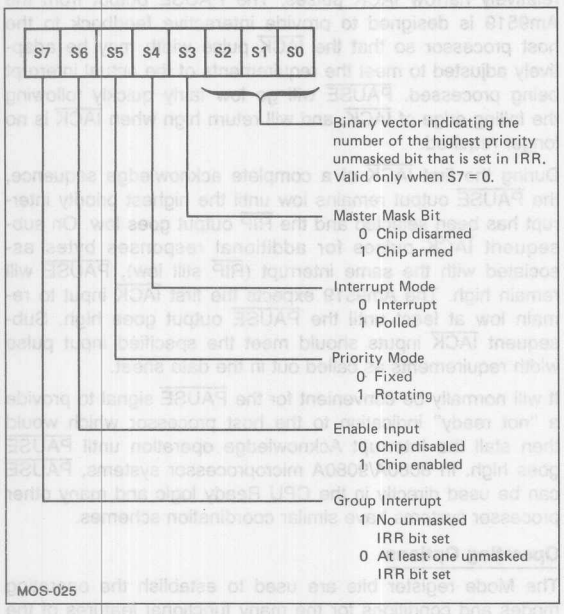



**Figure 11. Status Register Bit Assignments.**

The high order status bit, S7, reflects the information state of the Group Interrupt signal. Note that the polarity definition of S7 is independent of the defined polarity of GINT (Mode bit M3). Bit S7 remains valid when GINT is disabled by the polled mode option, thus permitting the host processor to check for "interrupts" by reading the Status register.

Status bit S6 reflects the state of the Enable In input signal and is used to indicate, in a multiple chip interrupt structure, which chips in the chain are disabled. When S6 is high, the chip can generate a GINT output and operation of its EO signal proceeds. When S6 is low, no GINT will be generated and EO will be forced low.

Status bit S5 reflects the state of the Priority Mode option, as specified by bit M0 of the Mode register. When S5 is high, rotating priority has been selected. When S5 is low, fixed priority has been selected.

Status bit S4 reflects the state of the Interrupt Mode option, as specified by bit M2 of the Mode register. When S4 is high, the polled mode has been selected and GINT disabled. When S4 is low, the interrupt mode has been selected.

Status bit S3 reflects the state of the Master Mask bit as specified by bit M7 of the Mode register. When S3 is low, the chip has been disarmed and IRR bits that are set will not generate GINT outputs. When S3 is high, the chip has been armed and interrupts can occur.

Status bits S2, S1 and S0 form a three bit field indicating the encoded binary number of the highest priority unmasked bit that is set in the IRR. This field should be considered invalid except when bit S7 of the Status register is low, indicating that at least one unmasked interrupt request is present. The binary coding of the field corresponds to the zero through seven numbering of the IREQ inputs. When more than one unmasked IRR bit is set, the S2, S1, S0 field will indicate the one unfenced request that is the highest priority as determined by the priority mode being used. Thus, the number of the dominant interrupt after all masking, fencing and priority resolution, is encoded into the Status register. This field is quite useful in the polled mode since it can act as a psuedo-vector for the host processor software.

### Command Register

The Command Register is eight bits long and is used to store the most recently entered command. It is loaded directly from the data bus by executing a write operation at the control port. Depending on the specific command opcode that is entered, an immediate internal activity may be initiated or the part may be preconditioned for subsequent data bus transfers. The "Command Description" section of this note explains each command operation. The commands are summarized in Figure 17.

### Mode Register

The Mode register is eight bits long and controls the operating modes and options of the Am9519. Figure 12 shows the bit assignments for the Mode register. No single command or interface operation will load all bits of the Mode register in parallel. The five low order bits (M0 through M4) are loaded in parallel directly from the command register. Mode bits M5, M6, and M7 are controlled by separate commands. The Mode register cannot be read out on the data bus. The data in Mode bits M0, M2, and M7 are available as part of the Status register. The Mode register is cleared by a software reset or a power-up reset. The "Operating Options" section of this note describes the detailed functions associated with each Mode bit.

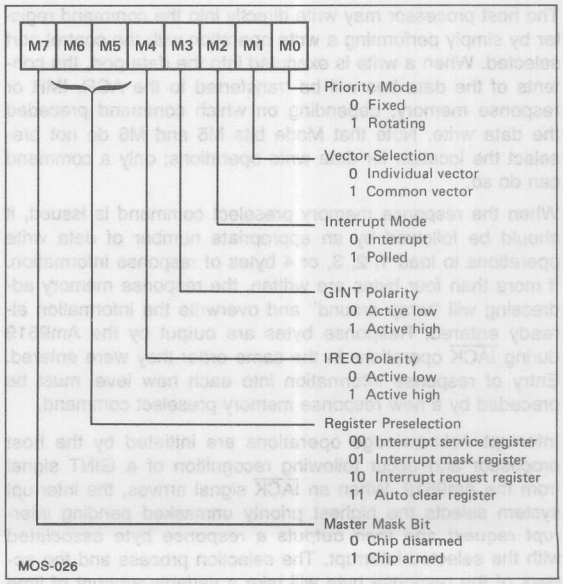



**Figure 12. Mode Register Bit Assignments.**

9

## Information Transfers

Figure 13 summarizes the control signal configurations for all information transfers on the Am9519 data bus. The interface control logic assumes the following conventions:

1. $\overline{RD}$ and $\overline{WR}$ are never active at the same time.
2. $\overline{RD}$, $\overline{WR}$ and C/$\overline{D}$ are ignored unless $\overline{CS}$ is low.

| Control Input | | | | | Data Bus Operation |
|---|---|---|---|---|---|
| $\overline{CS}$ | C/$\overline{D}$ | $\overline{RD}$ | $\overline{WR}$ | $\overline{IACK}$ | |
| 0 | 0 | 0 | 1 | 1 | Transfer contents of data register specified by Mode bits M5, M6 to data bus. |
| 0 | 0 | 1 | 0 | 1 | Transfer contents of data bus to data register specified by Command register. |
| 0 | 1 | 0 | 1 | 1 | Transfer contents of Status register to data bus. |
| 0 | 1 | 1 | 0 | 1 | Transfer contents of data bus to Command register. |
| 1 | X | X | X | 0 | Transfer contents of selected response memory location to data bus. |
| 1 | X | X | X | 1 | No information transferred; data bus outputs off. |

**Figure 13. Summary of Data Bus Transfers.**

When $\overline{IACK}$ is low, internal logic disables the $\overline{CS}$ input. This prevents signals on the address bus from inadvertently selecting the chip.

The host processor may read the Status register directly by simply performing a read operation with the control port selected. When a read is executed at the data port, the information transferred will be the contents of the ISR, IMR, IRR or ACR, depending on the state of Mode register bits M5 and M6.

The host processor may write directly into the command register by simply performing a write operation with the control port selected. When a write is executed into the data port, the contents of the data bus will be transferred to the ACR, IMR or response memory, depending on which command preceded the data write. Note that Mode bits M5 and M6 do not preselect the location for data write operations; only a command can do so.

When the response memory preselect command is issued, it should be followed by an appropriate number of data write operations to load 1, 2, 3, or 4 bytes of response information. If more than four bytes are written, the response memory addressing will "wrap around" and overwrite the information already entered. Response bytes are output by the Am9519 during $\overline{IACK}$ operations in the same order they were entered. Entry of response information into each new level must be preceded by a new response memory preselect command.

Interrupt Acknowledge operations are initiated by the host processor and occur following recognition of a GINT signal from the Am9519. When an $\overline{IACK}$ signal arrives, the interrupt system selects the highest priority unmasked pending interrupt request and then outputs a response byte associated with the selected interrupt. The selection process and the access of the response byte will take a variable amount of time that depends on several parameters, including:

1. the operating temperature,
2. the actual internal logic delays,
3. the number of Am9519 chips cascaded together,
4. the priority level of the interrupt being acknowledged,
5. the Mode register operating options,
6. the byte position within the response sequence.

The worst-case $\overline{IACK}$ pulse widths must be long enough to accomodate the accumulated delays that can occur in large interrupt systems operating in worst-case situations. Yet small systems operating under typical conditions will require only relatively narrow $\overline{IACK}$ pulses. The $\overline{PAUSE}$ output from the Am9519 is designed to provide interactive feedback to the host processor so that the $\overline{IACK}$ pulse width may be adaptively adjusted to meet the requirements of the actual interrupt being processed. $\overline{PAUSE}$ will go low fairly quickly following the falling edge of $\overline{IACK}$, and will return high when $\overline{IACK}$ is no longer required.

During the first $\overline{IACK}$ of a complete acknowledge sequence, the $\overline{PAUSE}$ output remains low until the highest priority interrupt has been selected and the $\overline{RIP}$ output goes low. On subsequent $\overline{IACK}$ pulses for additional responses bytes associated with the same interrupt ($\overline{RIP}$ still low), $\overline{PAUSE}$ will remain high. The Am9519 expects the first $\overline{IACK}$ input to remain low at least until the $\overline{PAUSE}$ output goes high. Subsequent $\overline{IACK}$ inputs should meet the specified input pulse width requirements as called out in the data sheet.

It will normally be convenient for the $\overline{PAUSE}$ signal to provide a "not ready" indication to the host processor which would then stall the Interrupt Acknowledge operation until $\overline{PAUSE}$ goes high. In 8080A/9080A microprocessor systems, $\overline{PAUSE}$ can be used directly in the CPU Ready logic and many other processor systems have similar coordination schemes.

## Operating Options

The Mode register bits are used to establish the operating modes and conditions for the many functional features of the Am9519. The Mode register allows the host processor to personalize the interrupt system for the application at hand.

### Priority Selection

Bit M0 in the Mode register specifies the priority operating mode for the Am9519. When M0=0, fixed priority is selected and the eight IREQ inputs are assigned a priority based on their physical location at the chip interface. IREQ0 has the highest priority and IREQ7 has the lowest. See Figure 14.

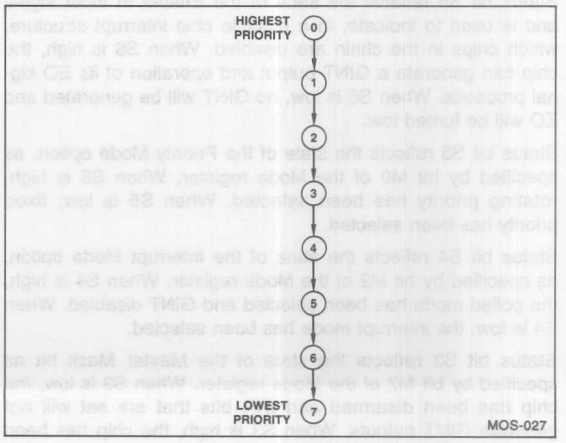



**Figure 14. Fixed Priority Mode.**

Priority is not resolved until the host processor initiates the interrupt acknowledge sequence. Thus, for example, an IREQ5 input may cause a GINT output to the host, but if an input on IREQ2 arrives before the falling edge of $\overline{IACK}$, then it is IREQ2 that will be selected and serviced. Notice that inherent in the fixed priority structure is the possibility that IREQ5 might never be selected and serviced as long as there are higher priority interrupts pending. IREQ2 could end up being serviced many times before IREQ5 is acknowledged. In many systems this is an appropriate method for handling the interrupting devices. Where circumstances permit, the masking capability of the Am9519 can be used by the host processor to modify the effective priority structure, perhaps by masking out recently serviced high priority devices, thus allowing lower priority inputs to be recognized.

Alternatively, where the eight interrupts have similar priority and service bandwidth requirements, the rotating priority mode may be selected (Mode register bit M0=1). As shown in Figure 15 the relative priorities remain the same as in the fixed mode; that is, IREQ2 is higher than IREQ3 which is higher than IREQ4, etc. However, in rotating priority mode, the lowest priority position in the circular chain is assigned by the hardware to the most recently serviced interrupt.

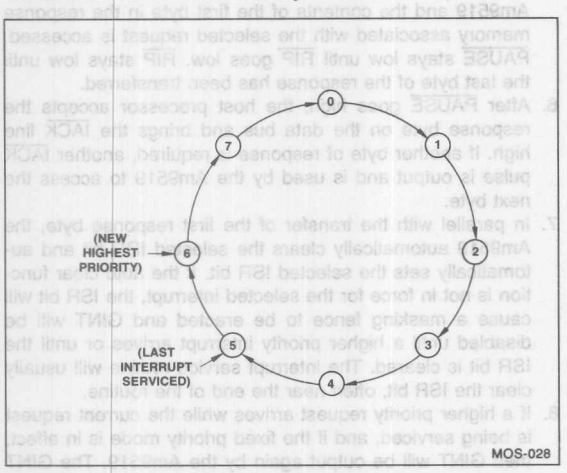



**Figure 15. Rotating Priority Mode.**

The example illustrated in Figure 15 assumes that IREQ5 has just finished being serviced and has therefore been assigned the lowest priority. Thus, IREQ6 occupies the new highest priority position, IREQ7 next-to-highest, etc. If two new interrupts then arrive at level 1 and level 4, IREQ1 will be selected and serviced, and will become the lowest priority. IREQ4 will then be acknowledged unless an active input on IREQ2 or IREQ3 has arrived in the meantime.

This rotating priority scheme prevents any request from dominating the system. It assures that an input will not have to wait for more than seven other service cycles before being acknowledged. Rotation occurs when the ISR bit of the presently selected interrupt is cleared.

In the rotating priority mode, inputs other than the one currently being serviced are fenced out and will not cause interrupts until the ISR bit is cleared. Thus, only one bit at a time will be set in the ISR. Care should be used when selecting the rotating mode to keep from doing so at a time when more than one ISR is set.

### Vectoring

Bit M1 of the Mode register specifies the vectoring option. When M1=0 the individual vector mode is selected and each interrupt is associated with its own unique four-byte location in the response memory. When M1=1, on the other hand, the common vector mode is selected and all response information is supplied from the location associated with IREQ0, no matter which request is being acknowledged. This operating option will be useful in situations where several similar devices share a common service routine and direct individual device identification is not important. This may be true simply because of the nature of the peripheral/system interaction, or it may be a transient system condition that only uses the common vector option temporarily, perhaps to save the overhead involved in filling the response memory twice.

### Polled Mode

Bit 2 of the Mode register allows the system to disable the GINT output. When M2=0 the interrupt mode is selected with the GINT output enabled. This might be considered the "normal" interrupt mode and makes full use of the interrupt control and management capabilities of the Am9519. When M2=1 the polled mode is selected which prevents the GINT output from going true by forcing it to its inactive state. In this condition, since no interrupts are supplied to the host processor, there will usually not be any $\overline{IACK}$ pulses returned to the Am9519. Consequently, ISR bits are not set, fences are not erected and IRR bits will not be automatically cleared. In the polled mode the host processor may read the Status register to determine if a request is pending and which request has the highest priority. IRR bits may be cleared by the host software. When the polled option is selected, the EI input is connected directly to the EO output thus functionally removing the polled chip from the external priority hierarchy.

Effectively, the polled mode of operation bypasses the hardware interrupt, inter-chip priority resolution, vectoring and fencing functions of the Am9519. What remains is the request latching, masking and intra-chip priority resolution.

### GINT Polarity

Bit 3 of the Mode register specifies the sense of the GINT output. When M3=0, Group Interrupt is selected as active low ($\overline{GINT}$) and becomes an open drain output. This allows simple wired-or connections to other similar Am9519 outputs as well as to other sources of interrupts, and matches the polarity required by many processors. When M3=1, Group Interrupt is selected as active high (GINT) and becomes a two-state push-pull output, simplifying the interface to processors with active high interrupt inputs.

### IREQ Polarity

Bit 4 of the Mode register specifies the sense of the IREQ inputs. When M4=0 the Interrupt Request signals are selected as active low ($\overline{IREQ}$) and a negative-going transition is required to set the IRR. When M4=1 the Interrupt Request signals are selected as active high (IREQ) and a positive-going transition is required to set the IRR. This sense option helps simplify the interface to interrupting devices.

### Register Preselection

Bits 5 and 6 of the Mode register specify the internal data register that will be output by the Am9519 on any read operation at the data port ($\overline{CS}$=0, $\overline{RD}$=0, C/$\overline{D}$=0). These bits do not affect destinations for write operations. The four

registers available for reading are the IRR, ISR, IMR and ACR. Preselect coding for each register is shown in Figure 12. The preselection remains in effect for all data read transfers until the contents of M5 and M6 are changed.

The ability to examine these important operating registers, combined with the information available in the Status register, provides significant insight into the internal conditions of the Am9519. This allows the host processor not only enhanced dynamic operating flexibility, but also access to important diagnostic/testing/debugging information.

### Master Mask

Bit 7 of the Mode register specifies the armed status of the Am9519 by way of the Master Mask control bit. When M7=0 the chip is disarmed just as if all eight bits in the IMR had been set. That is, IREQ inputs will be accepted and latched but will not cause GINT outputs to the host. In addition, the EO output is brought low, disabling any lower priority chips that may be attached. When M7=1, the chip is armed and any active unmasked interrupt inputs will be able to cause GINT outputs to the host processor.

The Master Mask capability permits the host system to disarm a chip and prevent processing of the interrupts without disturbing the contents of the IMR. Thus when the chip is re-armed, the old IMR conditions remain in effect and need not be reloaded. Note that a single command to the Master Mask bit of the highest priority interrupt chip is able to shut down the complete interrupt system, no matter how large.

### Mode Reset

When a power-up or software reset occurs, the Mode register is cleared to all zeros. This means that after reset the following Mode register operating options will be in effect:

Fixed priority
Individual vectoring
Interrupt (non-polled) operation
GINT active low sense
IREQ active low sense
ISR preselected for reading
Chip disarmed by Master Mask

## Operating Sequence

The management of interrupts by the Am9519 is illustrated below with a description of a fairly typical sequence of events. The Am9519 has already been initialized and enabled and is ready to run. The host processor has enabled its internal interrupt structure.

1. One (or more) of the IREQ inputs becomes active indicating that service is desired.
2. The requests are captured and latched in the IRR asynchronously. The latching action of the IRR cannot be disabled and active requests will always be stored unless a previous request at the same IRR bit has not been cleared.
3. If the active IRR bit is masked by the corresponding bit in the IMR, no further action takes place. When the IRR bit is not masked, an active Group Interrupt output will be generated if the Am9519 is not in its polled mode.
4. The GINT output from the Am9519 is used by the host processor as an interrupt input. When GINT is recognized by the host, it normally will complete the execution of its current instruction and will then execute some form of interrupt acknowledge sequence instead of the next program instruction. As part of the acknowledge cycle, the processor usually automatically disables its interrupt input. The Am9519 expects to receive one or more $\overline{IACK}$ signals from the processor during the acknowledge sequence.
5. When $\overline{IACK}$ is received, the Am9519 brings its $\overline{PAUSE}$ output low and begins selection of the highest priority unmasked active IRR bit. All interrupts that have become active before the falling edge of $\overline{IACK}$ are considered. When selection is complete, the $\overline{RIP}$ output is pulled low by the Am9519 and the contents of the first byte in the response memory associated with the selected request is accessed. $\overline{PAUSE}$ stays low until $\overline{RIP}$ goes low. $\overline{RIP}$ stays low until the last byte of the response has been transferred.
6. After $\overline{PAUSE}$ goes high, the host processor accepts the response byte on the data bus and brings the $\overline{IACK}$ line high. If another byte of response is required, another $\overline{IACK}$ pulse is output and is used by the Am9519 to access the next byte.
7. In parallel with the transfer of the first response byte, the Am9519 automatically clears the selected IRR bit and automatically sets the selected ISR bit. If the auto clear function is not in force for the selected interrupt, the ISR bit will cause a masking fence to be erected and GINT will be disabled until a higher priority interrupt arrives or until the ISR bit is cleared. The interrupt service routine will usually clear the ISR bit, often near the end of the routine.
8. If a higher priority request arrives while the current request is being serviced, and if the fixed priority mode is in effect, then GINT will be output again by the Am9519. The GINT signal will be recognized by the host processor only if the host has enabled its interrupt input. If this new request is acknowledged, the Am9519 will clear the corresponding IRR bit and set the corresponding ISR bit.
9. When the host processor has completed all interrupt service activity to satisfy the interrupting devices, it will normally clear the remaining ISR bit, if any, enable its internal interrupt system, if it has not already done so, and then return to the main program.

## COMMAND DESCRIPTIONS

The Am9519 command set allows the host processor to customize and alter the interrupt operating modes and features for particular applications, to initialize and update the response locations, and to manipulate the internal controlling bit sets during interrupt servicing. Commands are entered from the data bus directly into the Command register by writing into the Am9519 control port ($\overline{CS}$=0, $\overline{WR}$=0, C/$\overline{D}$=1). All the available commands are described below and are summarized in Figure 17. In the binary coding of the commands, "X" indicates a do-not-care bit position.

### RESET

Coding:

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Description: The Reset command allows the host processor to establish a known internal condition. The response memory and byte count registers are not affected by the software reset. The IMR is set to all ones. The ISR, IRR, ACR and Mode registers are cleared to all zeros.

### CLEAR IRR AND IMR

Coding:

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | X | X | X |

Description: All bits in the IMR and all bits in the IRR are cleared at the same time. Thus all interrupts are enabled and the previous history of all IREQ transitions is forgotten. If GINT was active when the command was entered, it will go inactive.

### CLEAR SINGLE IMR AND IRR BIT

Coding:

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | B2 | B1 | B0 |

Description: The same single bit position is cleared in both the IMR and the IRR. Other bits are not changed. If the specified IRR bit was generating an active interrupt output, GINT may go inactive upon entry of the command. The bit position cleared is specified by the B2, B1, B0 field as shown in Figure 16.

### CLEAR IMR

Coding:

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | X | X | X |

Description: All bits in the IMR are cleared to zeros. All IRR bits will therefore be unmasked and any IRR bits that had been set will be able to cause an active GINT output after the command is entered.

### CLEAR SINGLE IMR BIT

Coding:

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | B2 | B1 | B0 |

Description: A single bit in the IMR is cleared. Other bits are not changed. If the corresponding bit in the IRR was set, it will be unmasked and will be able to cause an active GINT after entry of the command. The IMR bit cleared is specified by the B2, B1, B0 field as shown in Figure 16.

### SET IMR

Coding:

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | X | X | X |

Description: All bits in the IMR are set to ones. All IRR bits will therefore be masked and unable to generate an active GINT. If GINT had been active, it will go inactive after the command is entered.

### SET SINGLE IMR BIT

Coding:

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 1 | B2 | B1 | B0 |

Description: A single bit in the IMR is set. Other bits are not changed. If the corresponding bit in the IRR was active and generating a GINT output, GINT will become inactive after the command is entered. The IMR bit set is specified by the B2, B1, B0 field as shown in Figure 16.

### CLEAR IRR

Coding:

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | X | X | X |

Description: All bits in the IRR are cleared to zeros. GINT will become inactive. New transitions on the IREQ inputs will be necessary to cause an interrupt.

### CLEAR SINGLE IRR BIT

Coding:

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 | B2 | B1 | B0 |

Description: A single bit in the IRR is cleared to zero. It will not cause an active GINT until it is set. The IRR bit cleared is specified by the B2, B1, B0 field as shown in Figure 16.

### SET IRR

Coding:

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | X | X | X |

Description: All bits in the IRR are set to ones. Any that are unmasked will be able to cause an active GINT output. This command allows the host CPU to initiate eight interrupts in parallel.

### SET SINGLE IRR BIT

Coding:

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 1 | B2 | B1 | B0 |

Description: A single bit in the IRR is set to a one. If it is unmasked it will be able to generate an active GINT. This command allows the host processor to simulate with software the arrival of a hardware interrupt request. It also gives the software access to the hardware priority resolution, masking and control features of the Am9519. The bit set is specified by the B2, B1, B0 field as shown in Figure 16.

### CLEAR HIGHEST PRIORITY ISR BIT

Coding:

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 0 | X | X | X | X |

Description: A single bit in the ISR is cleared to zero. If only one bit was set, that is the one cleared. If more than one bit was set, this command clears the one with the highest priority. This command is useful in software contexts where the service routine does not know which device is being serviced. It should be used with caution since the highest priority ISR bit may not really be the bit intended. When using the auto clear option on some interrupts and/or when a subroutine nesting hierarchy is not priority driven, the highest priority ISR bit may not correspond to the one being serviced.

### CLEAR ISR

Coding:

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 0 | X | X | X |

Description: All bits in the ISR are cleared to zeros. Mask fencing is eliminated.

### CLEAR SINGLE ISR BIT

Coding:

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 | B2 | B1 | B0 |

Description: A single bit in the ISR is cleared to zero. If the bit was already cleared, no effective operation takes place. The bit cleared is specified by the B2, B1, B0 field as shown in Figure 16. This will be the most useful command for service routines to use in managing the ISR without the help of the auto-clear option.

### LOAD MODE BITS M0 THROUGH M4

Coding:

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | M4 | M3 | M2 | M1 | M0 |

Description: The five low order bits of the Command register are transferred into the five low order bits of the Mode register. This command controls all of the Mode options except the master mask and the register preselection.

### CONTROL MODE BITS M5, M6, M7

Coding:

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | M6 | M5 | N1 | N0 |

Description: The M6, M5 field in the command is loaded into the M6, M5 locations in the Mode register. This field controls the register preselection bits in the Mode register. The N1, N0 field in the command controls Mode bit M7 (Master Mask) and is decoded as follows:

| N1 | N0 | |
|---|---|---|
| 0 | 0 | No change to M7 |
| 0 | 1 | Set M7 |
| 1 | 0 | Clear M7 |
| 1 | 1 | (Illegal) |

Thus, this command may be considered as three distinct commands, depending on the coding of N1 and N0:

1. Load M5, M6 only
2. Load M5, M6 and set M7
3. Load M5, M6 and clear M7

The Command Summary in Figure 17 lists all three versions.

### PRESELECT IMR FOR WRITING

Coding:

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 1 | X | X | X | X |

Description: The IMR is targeted to be loaded from the data bus when the next write operation occurs at the data port. All subsequent data write operations will also load the IMR until a different command is entered. Read operations may be successfully inserted between the entry of this command and the subsequent writing of data into the IMR. The Mode register is not affected by this command.

### PRESELECT ACR FOR WRITING

Coding:

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | X | X | X | X |

Description: The ACR is targeted to be loaded from the data bus when the next write operation occurs at the data port. All subsequent data write operations will also load the ACR until a different command is entered. Read operations may be successfully inserted between the entry of this command and the subsequent writing of data into the ACR. The Mode register is not affected by this command.

### PRESELECT RESPONSE MEMORY FOR WRITING

Coding:

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | BY1 | BY0 | L2 | L1 | L0 |

Description: One level in the response memory is targeted for loading from the data bus by subsequent data write operations. The byte count register for that level is loaded from the BY1, BY0 field in the command. The L2, L1, L0 field specifies which of the eight response levels is being selected. This command should be followed by one to four data write operations to load response bytes. Field coding:

| BY1 | BY0 | Count |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 3 |
| 1 | 1 | 4 |

| L2 | L1 | L0 | Level |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | 6 |
| 1 | 1 | 1 | 7 |

The byte count value does not control the number of bytes entered into the response memory. It does control the number of bytes read from the memory by $\overline{IACK}$ pulses. Response bytes are output by the Am9519 in the same order they were entered.

| B2 | B1 | B0 | Bit Specified |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | 6 |
| 1 | 1 | 1 | 7 |

**Figure 16. Coding of B2, B1, B0 Field of Commands.**

| COMMAND CODE | | | | | | | | COMMAND DESCRIPTION |
|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |
| 0 | 0 | 0 | 1 | 0 | X | X | X | Clear all IRR and all IMR bits |
| 0 | 0 | 0 | 1 | 1 | B2 | B1 | B0 | Clear IRR and IMR bit specified by B2, B1, B0 |
| 0 | 0 | 1 | 0 | 0 | X | X | X | Clear all IMR bits |
| 0 | 0 | 1 | 0 | 1 | B2 | B1 | B0 | Clear IMR bit specified by B2, B1, B0 |
| 0 | 0 | 1 | 1 | 0 | X | X | X | Set all IMR bits |
| 0 | 0 | 1 | 1 | 1 | B2 | B1 | B0 | Set IMR bit specified by B2, B1, B0 |
| 0 | 1 | 0 | 0 | 0 | X | X | X | Clear all IRR bits |
| 0 | 1 | 0 | 0 | 1 | B2 | B1 | B0 | Clear IRR bit specified by B2, B1, B0 |
| 0 | 1 | 0 | 1 | 0 | X | X | X | Set all IRR bits |
| 0 | 1 | 0 | 1 | 1 | B2 | B1 | B0 | Set IRR bit specified by B2, B1, B0 |
| 0 | 1 | 1 | 0 | X | X | X | X | Clear highest priority ISR bit |
| 0 | 1 | 1 | 1 | 0 | X | X | X | Clear all ISR bits |
| 0 | 1 | 1 | 1 | 1 | B2 | B1 | B0 | Clear ISR bit specified by B2, B1, B0 |
| 1 | 0 | 0 | M4 | M3 | M2 | M1 | M0 | Load Mode register bits 0–4 with specified pattern |
| 1 | 0 | 1 | 0 | M6 | M5 | 0 | 0 | Load Mode register bits 5, 6 with specified pattern |
| 1 | 0 | 1 | 0 | M6 | M5 | 0 | 1 | Load Mode register bits 5, 6 and set Mode bit 7 |
| 1 | 0 | 1 | 0 | M6 | M5 | 1 | 0 | Load Mode register bits 5, 6 and clear Mode bit 7 |
| 1 | 0 | 1 | 1 | X | X | X | X | Preselect IMR for subsequent loading from data bus |
| 1 | 1 | 0 | 0 | X | X | X | X | Preselect ACR for subsequent loading from data bus |
| 1 | 1 | 1 | BY1 | BY0 | L2 | L1 | L0 | Load BY1, BY0 into byte count register and preselect response memory level specified by L2, L1, L0 for subsequent loading from data bus |

**Figure 17. Am9519 Command Summary.**

9

## SYSTEM INTERFACE

### Expansion

Several Am9519 chips may be cascaded to expand the number of interrupts than can be handled by the system. A two-chip configuration is shown connected to an 8080A/9080A microprocessor in Figure 18. In general, expansion past a single Am9519 will require simply an added Chip Select signal for each extra chip, and perhaps an inverter for the GINT signal if the processor interrupt input is active-high. The $\overline{\text{GINT}}$, $\overline{\text{PAUSE}}$, and $\overline{\text{RIP}}$ signals are all designed to be wire-OR'ed in expanded systems.

Priority management in expanded systems is controlled by the Enable In, Enable Out and Response In Process signals. Figure 19 shows the basic interconnections for an example interrupt system that can accept up to 40 interrupts, using five Am9519 chips. Notice that $\overline{\text{IACK}}$ is wired in parallel to all five circuits, and that the $\overline{\text{GINT}}$, $\overline{\text{RIP}}$, and $\overline{\text{PAUSE}}$ lines are respectively tied together. The three pullup resistors are used to establish the high logic levels for the open-drain outputs. Enable In of the first chip (A) is allowed to float, or may be tied high. Each Enable Out signal is connected to the next lower level Enable In input. Each chip accepts eight IREQ inputs; for purposes of this example it is assumed that an active interrupt arrives at chip D in the chain.

Figure 20 shows the timing relationships for the configuration of Figure 19. When the IREQ arrives, a $\overline{\text{GINT}}$ output is generated by chip D and is used to interrupt the host processor. When the host returns an $\overline{\text{IACK}}$ pulse, all the EO lines are brought low in parallel. $\overline{\text{PAUSE}}$ also goes low, and is used to extend the $\overline{\text{IACK}}$ pulse.

After the fall of $\overline{\text{IACK}}$, all chips wait until a brief internal delay elapses and then examine EI. If EI is low, internal activity is suspended until EI goes high. If EI is high, then the internal circuitry is checked to see if an unmasked request is pending. If so, $\overline{\text{RIP}}$ is brought low, $\overline{\text{PAUSE}}$ is brought high, EO is kept low, and the first response byte is output on the data bus. In this example, there is no request in chip A and therefore the EO(A) line is brought high. This then allows chip B to see if it has an unmasked request waiting for service. If not, EO(B) goes high also and, with no interrupts at C, EO(C) goes high, driving EI(D) high. Since chip D finds a waiting request, it does not bring EO(D) high but it does bring $\overline{\text{RIP}}$ low. When $\overline{\text{RIP}}$ goes low it allows all the $\overline{\text{PAUSE}}$ outputs to switch high which permits the termination of the $\overline{\text{IACK}}$ pulse.

It can be seen, then, that the $\overline{\text{PAUSE}}$ output will automatically adjust the position of its rising edge to accommodate the exact functional and operational conditions that occur for each particular $\overline{\text{IACK}}$ cycle. For larger systems, like that in Figure 19, operating at high temperatures with slow versions of the Am9519 and servicing low priority interrupts, the processor delay caused by $\overline{\text{PAUSE}}$ may be quite long and a few processor wait cycles may be required to extend the $\overline{\text{IACK}}$ pulse. On the other hand, when a system like Figure 18 is running at typical room temperatures with typical parts and the interrupt is a high priority one, the $\overline{\text{PAUSE}}$ output width will be quite narrow and no wait cycles will be necessary.

The $\overline{\text{RIP}}$ output serves two basic functions within the interrupt system. First, its falling edge informs the other connected chips that an interrupt request has been selected and $\overline{\text{PAUSE}}$ may, therefore, be released. Secondly, as long as $\overline{\text{RIP}}$ is low, only the single chip that is pulling $\overline{\text{RIP}}$ down is allowed to respond to $\overline{\text{IACK}}$ inputs. $\overline{\text{RIP}}$ stays low until all response bytes for the selected interrupt have been transferred.

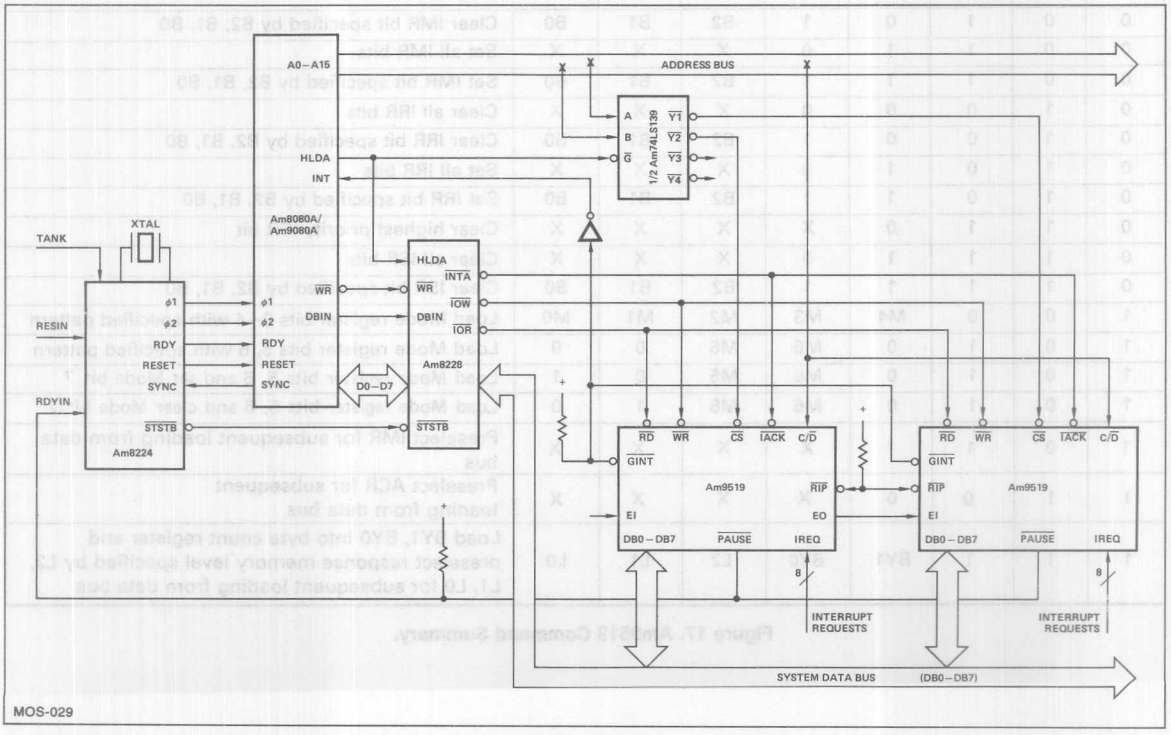



**Figure 18. 16 Interrupt Configuration with 8080A/9080A.**

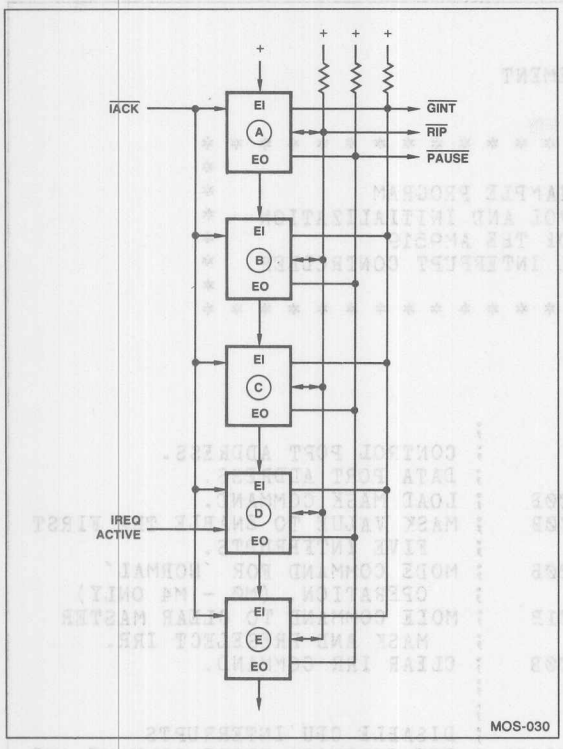



Figure 19. Five-Chip Expansion Example.

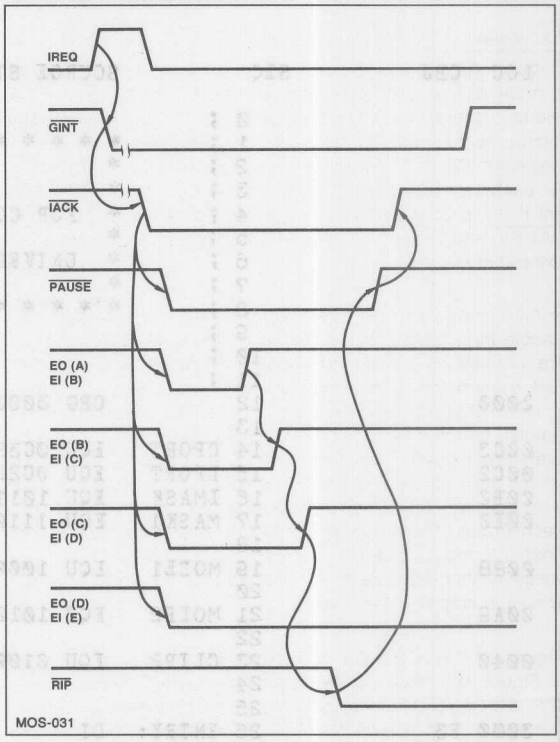



Figure 20. Inter-Chip Priority Resolution.

Assume that a new interrupt arrives at chip B in Figure 19 during the time that the first byte of a multibyte response for the interrupt at chip D is being transferred. Without the $\overline{RIP}$ signal there would be confusion when the second $\overline{IACK}$ pulse arrives. Both chips might try to send out response bytes since the interrupt at chip B is a higher priority, yet chip D is in the midst of a response sequence. With $\overline{RIP}$ present, however, no problem arises. Chip D pulls $\overline{RIP}$ low when it is selected and keeps $\overline{RIP}$ low until its response is complete. Chip B treats $\overline{RIP}$ as an input and will not respond to $\overline{IACK}$ until $\overline{RIP}$ goes high.

### Initialization and Support

Before the Am9519 can perform useful work, it must be initialized to customize it for a particular application and to load it with appropriate data values. During active operation, control options may be changed and response data may be modified. Because of the many ways it might be used, the Am9519 can be programmed using many different approaches. The following sequence description shows only one of several possible methods for constructing a basic service routine:

1. Disable processor interrupts.
2. Execute software reset at Am9519.
3. Transfer commands and response data from a control table into the Am9519.
4. Transfer operating options into the Mode register.
5. Transfer the operating Mask conditions into the IMR.
6. Clear the IRR.
7. Clear Master Mask.
8. Enable processor interrupts.
9. Return.

Figure 21 shows an example listing for such a routine using 8080A/9080A coding. Several assumptions are made about the hardware and software environment in which the routine will function:

1. When the routine is entered, register pair H, L contains the address of the first location of a control table, and register B contains a count that indicates how many entries the table contains.
2. One Am9519 is in the system. Its data port is decoded by the hardware as hex I/O address C2. Its control port is hex I/O address C3.
3. Only the first five interrupts will be in use by the main program. The others will be used later to support other processes.
4. Main program options: Fixed priority, Individual vectoring, Interrupt mode, GINT active high, IREQ active low, IRR selected for reading, Auto clear not used.

The control table is an important part of the routine and contains command information as well as the response data itself. The table consists of up to eight entries, each up to five bytes long, with all entries the same length. The first byte of each entry contains the response memory preselect command code with fields for the BY1, BY0 byte count and the L2, L1, L0 level pointer. The next one to four bytes of each entry contain the data loaded into the response memory. In this example the table has entries of four bytes each and is illustrated in Figure 22.

This type of table organization may contain extra bytes, but it compensates for this by allowing a brief, simple program to handle it. The table is fairly general and allows any length response to be programmed independently for each interrupt. It

9

```
LOC  OBJ        SEQ        SOURCE STATEMENT

                  0 ;
                  1 ;       * * * * * * * * * * * * * * * * * * * *
                  2 ;       *                                       *
                  3 ;       *          EXAMPLE PROGRAM              *
                  4 ;       *  FOR CONTROL AND INITIALIZATION       *
                  5 ;       *            OF THE AM9519              *
                  6 ;       *  UNIVERSAL INTERRUPT CONTROLLER       *
                  7 ;       *                                       *
                  8 ;       * * * * * * * * * * * * * * * * * * * *
                  9 ;
                 10 ;
                 11 ;
3000             12            ORG 3000H
                 13                                  ;
00C3             14 CPORT      EQU 0C3H              ; CONTROL PORT ADDRESS.
00C2             15 DPORT      EQU 0C2H              ; DATA PORT ADDRESS.
00B0             16 LMASK      EQU 10110000B         ; LOAD MASK COMMAND.
00E0             17 MASK1      EQU 11100000B         ; MASK VALUE TO ENABLE THE FIRST
                 18                                  ;   FIVE INTERRUPTS.
0088             19 MODE1      EQU 10001000B         ; MODE COMMAND FOR 'NORMAL'
                 20                                  ;   OPERATION. (M0 - M4 ONLY)
00A9             21 MODE2      EQU 10101001B         ; MODE COMMAND TO CLEAR MASTER
                 22                                  ;   MASK AND PRESELECT IRR.
0040             23 CLIRR      EQU 01000000B         ; CLEAR IRR COMMAND.
                 24                                  ;
                 25                                  ;
3000 F3          26 ENTRY:     DI                    ; DISABLE CPU INTERRUPTS
3001 3E00        27            MVI A,00000000B       ; GET SOFTWARE RESET COMMAND AND
3003 D3C3        28            OUT CPORT             ; SEND TO CONTROL PORT.
                 29                                  ;
3005 7E          30 AAA:       MOV A,M               ; GET CONTROL BYTE FROM TABLE &
3006 D3C3        31            OUT CPORT             ; SEND TO CONTROL PORT.
3008 23          32            INX H                 ; INCREMENT TABLE POINTER.
3009 0E03        33            MVI C,3               ; INITIALIZE VECTOR BYTE COUNT.
300B 7E          34 BBB:       MOV A,M               ; GET VECTOR BYTE AND
300C D3C2        35            OUT DPORT             ; SEND TO DATA PORT.
300E 23          36            INX H                 ; POINT TO NEXT TABLE BYTE.
300F 0D          37            DCR C                 ; DECREMENT BYTE COUNT.
3010 C20B30      38            JNZ BBB               ; ENTRY DONE?  NO:BACK TO BBB.
3013 05          39            DCR B                 ; YES:DECREMENT ENTRY COUNTER.
3014 C20530      40            JNZ AAA               ; TABLE DONE? NO:BACK TO AAA.
                 41                                  ;
3017 3E88        42            MVI A,MODE1           ; YES: PROCEED WITH MODE BYTE.
3019 D3C3        43            OUT CPORT             ; SEND MODE TO CONTROL PORT.
301B 3EB0        44            MVI A,LMASK           ; GET MASK LOAD COMMAND AND
301D D3C3        45            OUT CPORT             ; SEND TO CONTROL PORT.
301F 3EE0        46            MVI A,MASK1           ; GET OPERATING MASK AND
3021 D3C2        47            OUT DPORT             ; SEND TO DATA PORT.
3023 3E40        48            MVI A,CLIRR           ; GET CLEAR IRR COMMAND AND
3025 D3C3        49            OUT CPORT             ; SEND TO CONTROL PORT.
3027 3EA9        50            MVI A,MODE2           ; GET CLEAR MASTER MASK COMMAND
3029 D3C3        51            OUT CPORT             ; AND SEND TO CONTROL PORT.
302B FB          52            EI                    ; ENABLE CPU INTERRUPTS.
302C C9          53            RET                   ; RETURN TO CALLING PROGRAM.
                 54                                  ;
                 55            END
```

**Figure 21. Example Routine.**

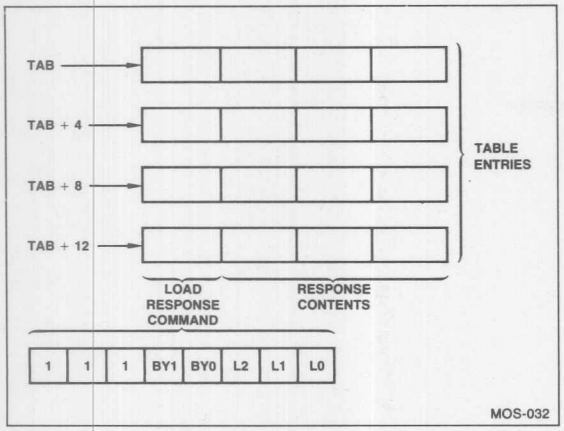



**Figure 22. Example Control Table.**

also allows any number of response locations to be updated in any order. The program driving the table simply assumes that every response level receives the same number of bytes as the level with the longest response.

Other table organizations are also possible. A more general table could contain the IMR value to be used, the ACR value, the table byte length, the operating mode values, etc. As more of the variable control information is added to the table, the software routine becomes more general and can be used not only for initialization, but for operational changes as well. Then there might be several tables in memory with an address supplied to the routine that points to the controlling table to be used. Note that the calling program can use just portions of an existing table if desired, simply by controlling the contents of the machine registers when the routine is entered.

Another approach is to omit the byte count/level command code from the table and compute its value in the driving routine. This may be especially appropriate when all the response entries are the same length and contiguous levels are being filled. The BY1, BY0 field need not change then, and a simple increment instruction will generate the proper command coding by changing the L2, L1, L0 field. To minimize the table length, which might become an important consideration for larger systems with many more interrupts, it is also possible to use the byte count to control the number of bytes transferred into each memory level.

The Am9519 offers new levels of versatility and sophistication for interrupt systems. It represents interesting opportunities for both hardware and software engineers to enhance new designs and to take advantage of the features now available.

TABLE ENTRIES
RESPONSE CONTENTS
LOCO RESPONSE COMMAND
LO
L1
L2
BY0
BY1
L
L
L

# Appendices

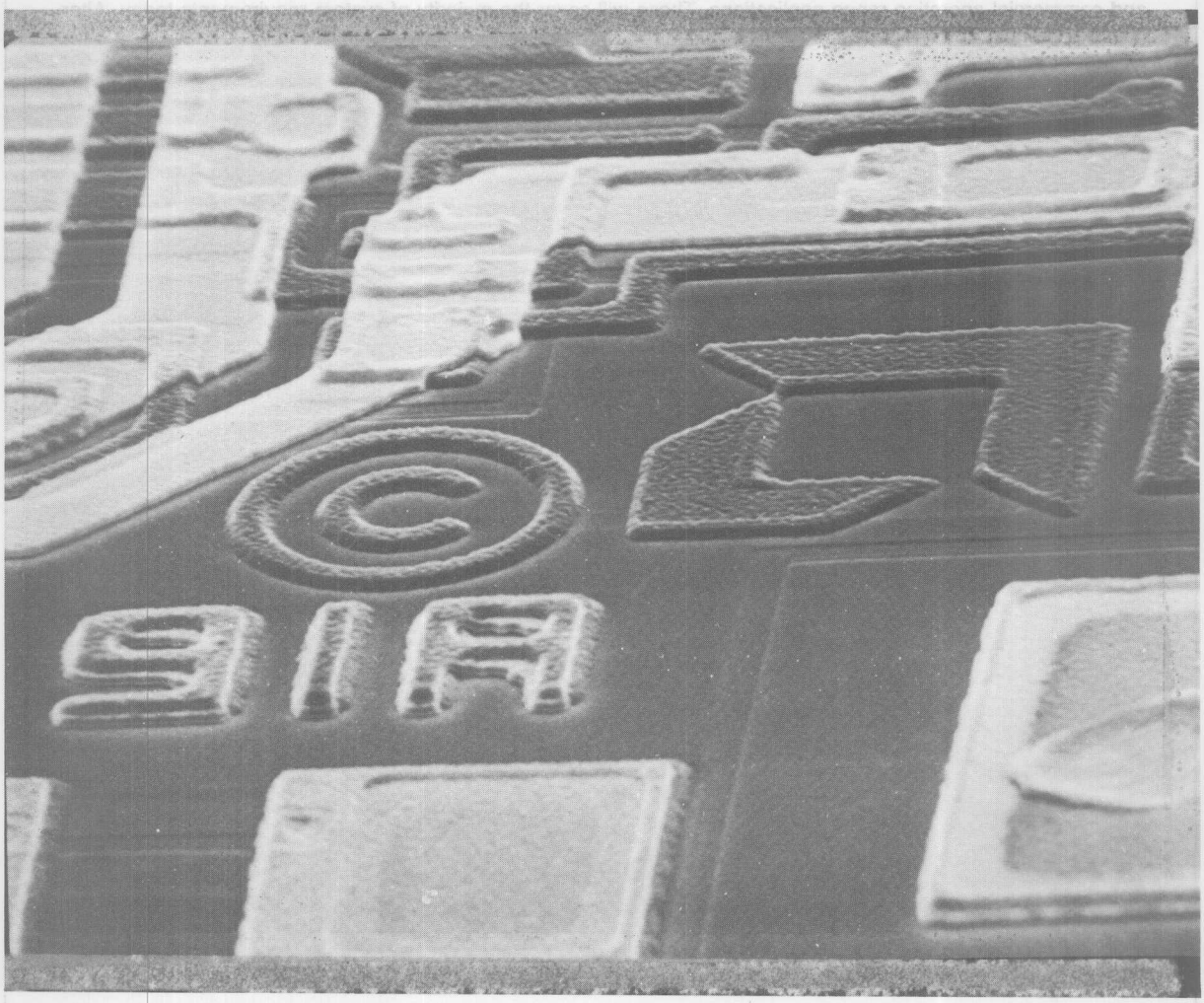
A

# Appendices

A

# Advanced Micro Devices Commitment to Excellence

## Product Assurance Programs for Military and Commercial Integrated Circuits



A

## Commitment to Excellence

Advanced Micro Devices was conceived on the premise that there was a place in the semiconductor community for a manufacturer dedicated to excellence.

In product assurance procedures, Advanced Micro Devices is unique. Only Advanced Micro Devices processes all integrated circuits, commercial as well as military, to the demanding requirements of MIL-STD-883. The Rome Air Development Center (RADC), which is the Air Force's principal authority on component reliability, has issued MIL-HDBK-217B which indicates that parts processed to Military Standard 883, Level C (Advanced Micro Devices' standard processing) yield a product nearly ten times better in failure rates than the industry commercial average.

Our Sunnyvale facility has been certified by the Defense Electronics Supply Center (DESC) to produce parts to JAN Class B and C under Military Specification MIL-M-38510. The National Aeronautics and Space Administration (NASA) has certified this production line for the manufacture of Class A products for programs requiring the highest levels of reliability. Advanced Micro Devices is the only integrated circuit company formed within the last ten years to achieve such line certification.

This brochure outlines Advanced Micro Devices' standard programs for Class B, C and A devices for military and commercial operating range applications. These will cover the majority of system requirements today. Alternative screening flows for specific user needs can be performed on request. Check with your local sales office for further information.

# ADVANCED MICRO DEVICES' STANDARD PRODUCTS ARE MANUFACTURED TO MIL-STD-883 REQUIREMENTS

Advanced Micro Devices' product assurance programs are based on two key documents.

MIL-M-38510 – General Specification for Microcircuits

MIL-STD-883 – Test Methods and Procedures for Microelectronics

The screening charts in this brochure show that every integrated circuit shipped by Advanced Micro Devices receives the critical screening procedures defined in MIL-STD-883, Method 5004 for Class C product. This includes molded plastic devices.

In addition, documentation, design, processing and assembly workmanship guidelines are patterned after MIL-M-38510 specifications.

Commercial and industrial users receive the quality and reliability benefits of this aerospace-type screening and documentation at no additional cost.

## STANDARD PRODUCT TESTING CATEGORIES

Advanced Micro Devices offers integrated circuits to four standard testing categories.

1. Commercial operating range product (typically 0°C to 70°C)
2. Commercial product with 100% temperature testing
3. Military operating range product (typically −55°C to +125°C)
4. JAN qualified product

Categories 1, 2 and 3 are available on most Advanced Micro Devices circuits. Category 4 is offered on a more limited line. Check with your local sales office for details.

## STANDARD PRODUCT ASSURANCE CATEGORIES

Devices produced to the above testing categories are available to the three standard classes of product assurance defined by MIL-STD-883. As a minimum, every device shipped by Advanced Micro Devices meets the screening requirements of Class C.

**Class C – For commercial and ground-based military systems where replacement can be accomplished without difficulty.**

According to MIL-HDBK-217B, this assures relative failure rates 9.4 times better than that of regular industry commercial product.

**Class B – For flight applications and commercial systems where maintenance is difficult or expensive and where reliablity is vital.**

Devices are upgraded from Class C to Class B by burn-in screening and additional testing.

According to MIL-HDBK-217B, Class B failure rate is improved 30 times over regular industry commercial product. Advanced Micro Devices Class B processing conforms to MIL-STD-883 requirements. MIL-HDBK-217B indicates that this may provide failure rates as much as two times better than some other manufacturers' "equivalent" or "pseudo" Class B programs.

**Class S – For space applications where replacement is extremely difficult or impossible and reliability is imperative.**

Class S screening includes x-ray and other special inspections tailored to the specific requirements of the user.

The 100% screening and quality conformance testing performed within these Advanced Micro Devices programs is shown in TABLES I, II and III. A full description of the process flow is provided in Product Assurance Document 15-010, available on request.

# CLASS C SCREENING FLOW FOR COMMERCIAL SYSTEMS AND GROUND BASED MILITARY SYSTEMS

## TABLE I
## CLASS C
## INTEGRATED CIRCUITS

| Screening Procedure per MIL-STD-883 Method 5004, Class C | | COMMERCIAL OPERATING RANGE | MILITARY OPERATING RANGE | |
|---|---|---|---|---|
| | | HERMETIC AND MOLDED PACKAGES | HERMETIC PACKAGE ONLY | |
| | | Flow C1 | Flow C3 | Flow C4 |
| Screen | Test Method | Commercial Product | Military Product | Jan Qualified Product |
| VISUAL AND MECHANICAL | | | | |
| Internal visual | 2010, Condition B | 100% | 100% | 100% |
| High temperature storage | 1008, Condition C, 24 hours | 100% | 100% | 100% |
| Temperature cycle | 1010, Condition C | 100% | 100% | 100% |
| Constant acceleration | 2001 | 100% (1) | 100% | 100% |
| Hermeticity, Fine and Gross | 1014 | 100% (1) | 100% | 100% |
| FINAL ELECTRICAL TESTS | | AMD Data Sheet | AMD Data Sheet | 38510 Slash Sheet |
| Static (dc) | a) At 25°C, and power supply extremes | 100% | 100% | 100% |
| | b) At temperature and power supply extremes | (2) | – | – |
| Functional | a) At 25°C, and power supply extremes | 100% | 100% | 100% |
| | b) At temperature and power supply extremes | (2) | – | – |
| Switching (ac) or Dynamic | At 25°C, nominal power supply | (2) | – | – |
| QUALITY CONFORMANCE | 5005, Group A (See Table II) | Sample | Sample | Sample |
| Sample Tests | Group B | – | – | Sample |
| | Group C | – | – | Sample |
| | Group D | – | – | Sample |
| EXTERNAL VISUAL | 2009 (Note 5) | 100% | 100% | 100% |

## TABLE II
## GROUP A QUALITY CONFORMANCE LEVELS

Advanced Micro Devices employs the military-recommended LTPD sampling system to assure quality. MIL-STD-883, Method 5005, TABLE I, Group A, subgroups 1 through 9 as appropriate to the device family are performed on every lot. Quality levels defined for Class B product are applied by Advanced Micro Devices to both Class B and Class C orders.

| | LTPD | INITIAL SAMPLE SIZE |
|---|---|---|
| Subgroup 1 – Static tests at 25°C | 5 | 45 |
| Subgroup 2 – Static tests at maximum rated operating temperature | 7 | 32 |
| Subgroup 3 – Static tests at minimum rated operating temperature | 7 | 32 |
| Subgroup 4 – Dynamic tests at 25°C – LINEAR devices | 5 | 45 |
| Subgroup 5 – Dynamic tests at maximum rated operating temperature – LINEAR devices | 7 | 32 |
| Subgroup 6 – Dynamic tests at minimum rated operating temperature – LINEAR devices | 7 | 32 |
| Subgroup 7 – Functional tests at 25°C | 5 | 45 |
| Subgroup 8 – Functional tests at maximum and minimum rated operating temperatures | 10 | 22 |
| Subgroup 9 – Switching tests at 25°C – DIGITAL devices | 7 | 32 |
| Subgroup 10 – Switching tests at maximum rated operating temperatures – DIGITAL devices | * | |
| Subgroup 11 – Switching tests at minimum rated operating temperatures – DIGITAL devices | * | |

*These subgroups, where applicable, are usually performed during initial characterization only for all except JAN Qualified product.

# CLASS B SCREENING FLOW FOR HIGH RELIABILITY COMMERCIAL AND MILITARY SYSTEMS

**TABLE III**
**CLASS B**
**INTEGRATED CIRCUITS**
**(Class C plus burn in screening and additional testing.)**

| Screening Procedure per MIL-STD-883 Method 5004, Class B | | COMMERCIAL OPERATING RANGE | MILITARY OPERATING RANGE | |
|---|---|---|---|---|
| | | HERMETIC AND MOLDED PACKAGES | HERMETIC PACKAGE ONLY | |
| | | Flow B1 | Flow B3 | Flow B4 |
| Screen | Test Method | Commercial Product | Military Product | Jan Qualified Product |
| VISUAL AND MECHANICAL | | | | |
| Internal visual | 2010, Condition B | 100% | 100% | 100% |
| High temperature storage | 1008, Condition C, 24 hours | 100% | 100% | 100% |
| Temperature cycle | 1010, Condition C | 100% | 100% | 100% |
| Constant acceleration | 2001 | 100% (1) | 100% | 100% |
| Hermeticity, Fine and Gross | 1014 | 100% (1) | 100% | 100% |
| BURN IN | | | | |
| Interim (pre burn in) electricals | Per applicable device specification | 100% | 100% | 100% |
| Burn in | 1015, 160 hours at 125°C or equivalent.* | 100% (3) | 100% | 100% |
| FINAL ELECTRICAL TESTS | | AMD Data Sheet | AMD Data Sheet | 38510 Slash Sheet |
| Static (dc) | a) At 25°C, and power supply extremes | 100% | 100% | 100% |
| | b) At temperature and power supply extremes | (2) (3) | 100% | 100% |
| Functional | a) At 25°C, and power supply extremes | 100% | 100% | 100% |
| | b) At temperature and power supply extremes | (2) (3) | 100% | 100% |
| Switching (ac) or Dynamic | At 25°C, nominal power supply | (2) | 100% | 100% |
| QUALITY CONFORMANCE | 5005, Group A (See Table II) | Sample | Sample | Sample |
| Sample Tests | Group B | – | (4) | Sample |
| | Group C | – | (4) | Sample |
| | Group D | – | (4) | Sample |
| EXTERNAL VISUAL | 2009 (Note 5) | 100% | 100% | 100% |

Notes: 1. Not applicable to molded packages.
2. All MOS RAMs and many other MOS devices receive a.c. testing and 100% d.c. screening at high temperature and power supply extremes as standard. Other products sampled at Group A (Table II).
3. Am2900 LSI products receive a 96 hour burn-in, plus 100% d.c. screening at high temperature and power supply extremes.
4. Available to special order.
5. Without optical aid for commercial devices.

*(Unless device data sheet specifies otherwise).

# CLASS S
# FOR AEROSPACE SYSTEMS. (FORMERLY CLASS A)

Advanced Micro Devices offers Class S programs based on screening defined in MIL-STD-883, Method 5004. Contact your local Advanced Micro Devices' sales office for more information.

A

# STANDARD PRODUCT
# SCREENING SUMMARY AND ORDERING INFORMATION

## 1. COMMERCIAL PRODUCT

- Screened per MIL-STD-883, Method 5004.
- Electrically tested per AMD Data Sheet.
- Supplied in hermetic and molded packages.
- Quality conformance testing, Method 5005, Group A, performed to levels specified for Class B on both Class C and Class B options.

### Class C (Flow C1)

- Order standard AMD part number.
- Marked same as order number.

  Example: Am2901ADC

### Class B (Flow B1)

- Burn in performed in AMD circuit condition.
- Order standard AMD part number, add suffix B (or /883B for 1, 2 and 300 Series Linear devices).
- Marked same as order number.

  Example: Am2901ADC-B

## 2. COMMERCIAL PRODUCT WITH 100% TEMPERATURE TESTING

- Identical to standard commercial operating range product with the addition of 100% dc and functional testing at 100°C and power supply extremes.

### Class C (Flow C2)

- Order standard AMD part number, add suffix T.
- Marked same as order number.

  Example: Am2901ADC-T

### Class B (Flow B2)

- Burn in performed in AMD circuit condition.
- Order standard AMD part number, add suffix TB.
- Marked same as order number.

  Example: Am2901ADC-TB

## 3. MILITARY PRODUCT

- Screened per MIL-STD-883, Method 5004.
- Electrically tested per AMD Data Sheet.
- Supplied in hermetic package only.
- Quality conformance testing, Method 5005, Group A, performed to levels specified for Class B on both Class B and Class C options.

### Class C (Flow C3)

- Order standard AMD part number.
- Marked same as order number.

  Example: Am2901ADM

### Class B (Flow B3)

- Burn in performed in AMD circuit condition.
- AC at 25°C, dc and functional testing at 25°C as well as temperature and power supply extremes performed on 100% of every lot.
- Quality conformance testing, Method 5005, Groups B, C and D available to special order.
- Order standard AMD part number, add suffix B.
- Marked same as order number.

  Example: Am2901ADM-B

## 4. JAN QUALIFIED PRODUCT

- Screened per MIL-STD-883, Method 5004.
- Electrically tested to JAN detail specification (slash sheet).
- Manufactured in Defense Logistics Agency certified facility.
- Quality conformance testing, Method 5005, Groups A, B, C and D performed as standard and must be completed prior to shipment.
- It is a product for which AMD has gained QPL listing.*

### Class C (Flow C4)

- Order per military document.
- Marked per military document.

  Example: JM38510/44001CQB

### Class B (Flow B4)

- Burn in performed in circuit condition approved for JAN devices.
- Order per military document.
- Marked per military document.

  Example: JM38510/44001BRC

*In certain cases where JAN Qualified product is specified but is not available, Advanced Micro Devices can provide devices to the electrical limits and burn-in criteria of the slash sheet. This class of product has been called JAN Equivalent and marked M38510/ by some manufacturers. This identification is no longer permitted by DESC. Check with your local sales office for availability of specific device types.

# PRODUCT ASSURANCE

All products manufactured by Advanced Micro Devices, including Bipolar Logic and Interface, Memory and Microprocessors, Linear and MOS/LSI meet the quality requirements of MIL-M-38510. In addition all products, both commercial and military temperature range, receive the 100% screening procedures defined in the current revision of MIL-STD-883, Method 5004, Class C.

## 1. AMD STANDARD PRODUCT – CLASS C PROCESSING

a) **Internal visual inspection:** Method 2010, Condition B.
b) **High temperature storage:** Method 1008, Condition C; 150°C, 24 hours.
c) **Temperature cycling:** Method 1010, Condition C; −65°C, 150°C, 10 cycles.
d) **Constant acceleration:** Method 2001, Condition E; 30,000 g., $Y_1$ plane. (Hermetic packages only.)
e) **Fine leak:** Method 1014, Condition A; $5 \times 10^{-8}$ atm cc per second. (Hermetic packages only.)
f) **Gross leak:** Method 1014, Condition C. (Hermetic packages only.)
g) **Final electrical test:** 100% D.C. and functional testing at 25°C and Group A sample per Method 5005.

To order this product, use the order number shown for the product desired. Example: AM2501DM for full military temperature range part in dual-in-line package, AM2501DC for commercial temperature range in dual-in-line package.

As noted, all material is processed to Class C and no additional price adders are imposed to deliver this level of reliability.

## 2. CLASS B PROCESSING

### Military Temperature Range

Standard product is upgraded to Class B with a 160-hour burn-in at 125°C followed by 100% electrical testing of D.C. parameters at 25°C, 125°C, −55°C and A.C. parameters at 25°C. Maximum PDA of 10% is based on the 25°C D.C. test subgroup. Burn-in conditions are steady state power (MIL-STD-883, Method 1015, Condition B) for linear circuits, and steady state power and reverse bias (Condition C) for all others. Standard burn-in circuit specifications for any device are available upon request. Condition D burn-in is available to special order. Consult your local AMD sales office for price and delivery.

To order this product, use the order number shown for the product desired and add the suffix "B". Example: AM2501DMB for military temperature product in dual-in-line package with burn-in as described, SN54LS174WB for military temperature range product in flat pack with burn-in. This processing meets all of the requirements of MIL-STD-883, Class B product.

### Commercial Temperature Range

Standard AMD Class C commercial temperature range product is burned in for use in non-military systems to a modified Class B program. A 160 hour burn-in, to a method meeting the requirements of Method 1015, Conditions A and B, is followed by the standard Class C electrical test procedures.

To order this level of screening, use the order number shown for the commercial device and add the suffix "B". Examples: AM25LS175DCB and SN74LS153NB.

## 3. CLASS S PROCESSING

Class S processing is recommended only for applications where replacement is extremely difficult and reliability is imperative. This material is only produced to special order. Consult AMD for further details.

## 4. QUALIFICATION AND QUALITY CONFORMANCE INSPECTION

Qualification and Quality Conformance Inspections are the electrical, mechanical, die-related and package-related tests defined by MIL-STD-883, Method 5005.

a) **Group A Electrical Tests:** Subgroups 1-9 (as appropriate for the device type) are always sampled. Subgroups 10-11 are sampled to special order or when applicable by device specification. Attributes data are available upon request and must be specifically noted on the purchase order.

The following inspections are performed to special order and must be called out separately from the order for components. Date code time period must be specified (e.g., same date code, date code within 6 weeks, etc.). Price will include devices used in the test, services performed and the data. Generic data covering Groups B, C and D from tests previously performed by AMD are usually available on the more popular items and families for a nominal charge.

b) **Group B Mechanical Tests:** Subgroups for the appropriate reliability class are tested in accordance with the procedures of MIL-STD-883, Method 5005. Attributes data are supplied as part of the order.

c) **Group C Die-Related Tests:** Subgroups for the appropriate reliability class are tested in accordance with the procedures of MIL-STD-883, Method 5005. Attributes data are supplied as part of the order.

d) **Group D Package-Related Tests:** Subgroups 1-5 are tested in accordance with the procedures of MIL-STD-883, Method 5005. Attributes data are supplied as part of the order.

## 5. NON-STANDARD PROCESSING AND ADDITIONAL INSPECTION SERVICES

Non-standard processing options such as customer marking, special electrical test tapes, U.S. builds, etc. must be quoted on an individual order basis. Detailed drawings and general specifications must first be reviewed by the factory before a firm quotation can be furnished.

Additional inspection services including radiographic (X-Ray) inspection, variables data (read and record) and scanning electron microscope (SEM) lot inspection are available.

Consult your local AMD sales office for further information on price and delivery of any of the above special requirements.

The product assurance program at Advanced Micro Devices defines manufacturing flow, establishes standards and controls, and confirms the product quality at critical points. Standardization under this program assures that all products meet military and government agency specifications for reliable ground applications. Further screening for users desiring flight hardware and other higher reliability classes is simplified because starting product meets all initial requirements for high-reliability parts.

The quality standards and screening methods of this program are equally valuable for commercial parts where equipment must perform reliably with minimum field service.

Two military documents provide the foundation for this program. They are:

**MIL-M-38510** – General Specification for Microcircuits
**MIL-STD-883** – Test Methods and Procedures for Microelectronics

**MIL-M-38510** describes design, processing and assembly workmanship guidelines for military and space-grade integrated circuits. All circuits manufactured by Advanced Micro Devices for full temperature range (−55°C to +125°C) operation meet these quality requirements of MIL-M-38510.

**MIL-STD-883** defines detail testing and inspection methods for integrated circuits. Three of the methods are quality and processing standards directly related to product assurance:

**Test Method 2010** defines the visual inspection of integrated circuits before sealing. By confirming fabrication and assembly quality, inspection to this standard assures the user of reliable circuits in long-term field applications. Standard inspection at Advanced Micro Devices includes all the requirements of the latest revision of Method 2010, condition B.

**Test Method 5004** defines three reliability classes of parts. All must receive certain basic inspection, preconditioning and screening stresses. The classes are:

**Class C** – Used where replacement can be readily accomplished. Screening steps are given in the AMD processing flow chart.

**Class B** – Used where maintenance is difficult or expensive and where reliability is vital. Devices are upgraded from Class C to Class B by 160-hour burn-in at 125°C followed by more extensive electrical measurements. All other screening requirements are the same.

**Class S** – Used where replacement is extremely difficult and reliability is imperative. Class S screening selects extra reliability parts by expanded visual and X-ray inspection, further burn-in, and tighter sampling inspection.

All hermetically sealed integrated circuits (military and commercial) manufactured by Advanced Micro Devices are screened to MIL-STD-883, Class C. Molded integrated circuits receive Class C screening except that centrifuge and hermeticity steps are omitted.

Optional extended processing to MIL-STD-883, Class B is available for all AMD integrated circuits. Parts procured to this screening are marked with a "−B" following the standard part number, except that linear 100, 200 or 300 series are suffixed "/883B".

**Test Method 5005** defines qualification and quality conformance procedures. Subgroups, tests and quality levels are given for Group A (electrical), Group B (mechanical quality related to the user's assembly environment), Group C (die related tests) and Group D (package related tests). Group A tests are always performed; Group B, C and D may be specified by the user.

## MANUFACTURING, SCREENING AND INSPECTION FOR INTEGRATED CIRCUITS

All integrated circuits are screened to MIL-STD-883, Method 5004, Class C; quality conformance inspection where required is performed to Class B quality levels on either Class B or Class C product.

All full-temperature-range (−55°C to +125°C) circuits are manufactured to the workmanship requirements of MIL-M-38510.

The flow chart identifies processing steps as they relate to MIL-STD-883 and MIL-M-38510.

### STANDARD PROCESSING CLASS C Steps 1 Through 25

HERMETIC PACKAGE PROCESS

MOLDED PACKAGE PROCESS

1 **INSPECTION**

Purchased or fabricated starting materials are inspected for conformance to specified requirements. Inspection follows written procedures, and records are analyzed for supplier quality negotiations.

2 **WAFER FABRICATION**

Repeated masking, etching and diffusion processes produce finished dice in wafer form.

3 **IN-PROCESS INSPECTION**

Each wafer is inspected prior to irreversible process steps.

4 **FINISHED WAFER INSPECTION**

Sample wafers from each finished diffusion lot are inspected to confirm lot quality before release for test and assembly.

5 **WAFER ELECTRICAL TEST**

Electrical probe test of every die. A computer-controlled system measures static and dynamic parameters and identifies dice that do not meet electrical requirements.

6 **DIE SEPARATION**

Wafers are separated into individual dice and electrical rejects are removed.

7 **VISUAL INSPECTION**

Separated dice are inspected and selected at high magnification.

8 **QUALITY INSPECTION**

Decisions at the 100% inspection are reviewed through periodic random sampling, confirming product quality and revealing any need for operator retraining.

9 **DIE ATTACH**

10 **QUALITY INSPECTION**

Strength of die attachment, position of die and visual quality of eutectic wetting are confirmed periodically by inspecting random samples and push-testing the attached dice.

11 **WIRE BOND**

Hermetic: Aluminum wires, ultrasonic bonding.

Molded: Gold wires, thermocompression bonding.

12 **QUALITY INSPECTION**

Weld strength, bond size and position, wire dress and general workmanship are confirmed periodically by comparing random samples with assembly instructions and quality standards. Bond strength is plotted on statistical control charts, providing early warning of process drifts.

13 **INTERNAL VISUAL INSPECTION**

Assembled but unsealed units are individually inspected at low and high power.

**QUALITY STANDARDS:**

All devices – MIL-STD-883, Method 2010, Condition B (latest revision). Full temperature devices – MIL-M-38510, Para. 3.7 for workmanship (re-bonding limits).

14 **QUALITY INSPECTION**

Decisions at the 100% inspection are reviewed through periodic random sampling, providing confirmation of product quality and revealing any need for operator retraining.

15a **FINAL SEAL**

(Hermetic devices)

15b **ENCAPSULATE**

(Molded Devices)

16 **HIGH TEMPERATURE STORAGE**

MIL-STD-883, Method 1008, Cond. C: 150°C, 24 hr

17 **TEMPERATURE CYCLE**

MIL-STD-883, Method 1010, Cond. C: −65°C, +150°C, 10 cycles

18 **CENTRIFUGE**

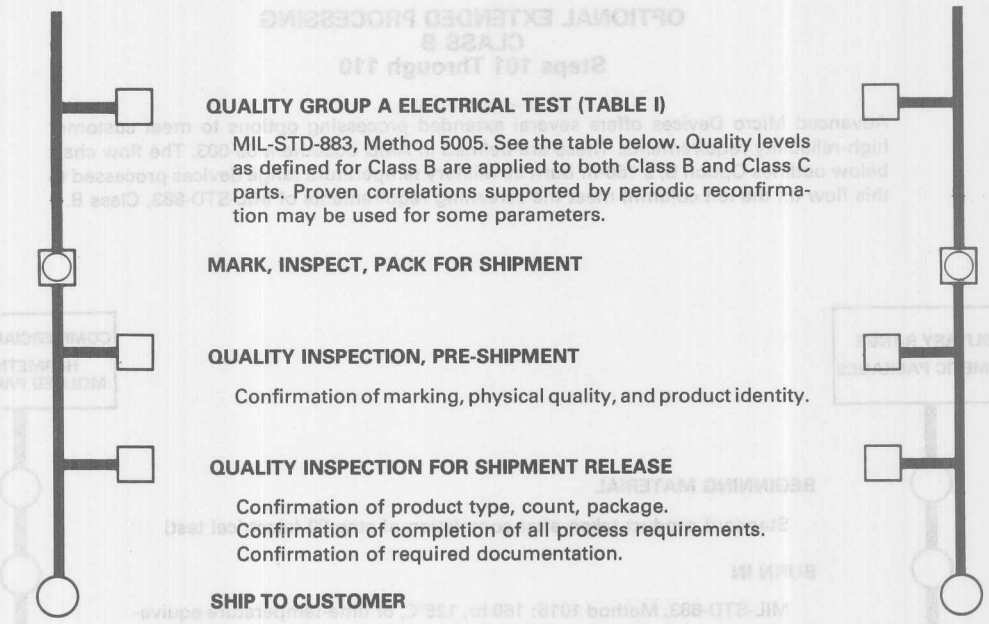
MIL-STD-883, Method 2001, Cond. E: 30,000 G

19 **SEAL (HERMETICITY) TEST**

MIL-STD-883, Method 1014, Cond. A or B: Fine Leak
MIL-STD-883, Method 1014, Cond. C2: Gross Leak

20 **ELECTRICAL TEST**

MIL-STD-883, Method 5004, Para. 3.1.12: Static, dynamic, functional tests at 25°C or in certain products at the most critical extreme temperature to assure accuracy of device selection.



21 **QUALITY GROUP A ELECTRICAL TEST (TABLE I)**

MIL-STD-883, Method 5005. See the table below. Quality levels as defined for Class B are applied to both Class B and Class C parts. Proven correlations supported by periodic reconfirmation may be used for some parameters.

22 **MARK, INSPECT, PACK FOR SHIPMENT**

23 **QUALITY INSPECTION, PRE-SHIPMENT**

Confirmation of marking, physical quality, and product identity.

24 **QUALITY INSPECTION FOR SHIPMENT RELEASE**

Confirmation of product type, count, package.
Confirmation of completion of all process requirements.
Confirmation of required documentation.

25 **SHIP TO CUSTOMER**

This AMD standard product meets screening requirements of MIL-STD-883, Class C.

**GROUP A ELECTRICAL TESTS**
**From MIL-STD-883, Method 5005, Table I**

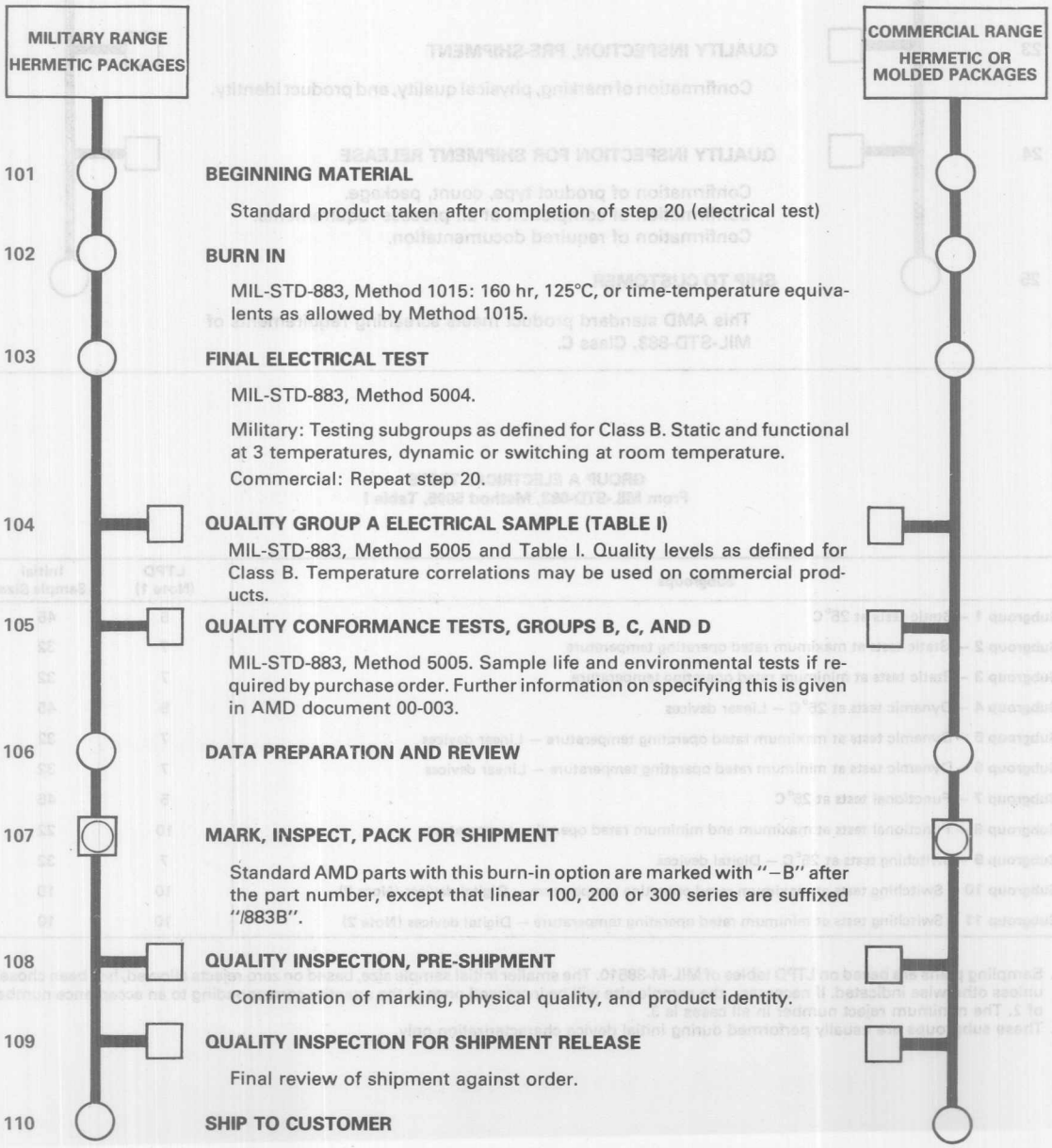
| Subgroups | LTPD (Note 1) | Initial Sample Size |
|---|---|---|
| **Subgroup 1** — Static tests at 25°C | 5 | 45 |
| **Subgroup 2** — Static tests at maximum rated operating temperature | 7 | 32 |
| **Subgroup 3** — Static tests at minimum rated operating temperature | 7 | 32 |
| **Subgroup 4** — Dynamic tests at 25°C — Linear devices | 5 | 45 |
| **Subgroup 5** — Dynamic tests at maximum rated operating temperature — Linear devices | 7 | 32 |
| **Subgroup 6** — Dynamic tests at minimum rated operating temperature — Linear devices | 7 | 32 |
| **Subgroup 7** — Functional tests at 25°C | 5 | 45 |
| **Subgroup 8** — Functional tests at maximum and minimum rated operating temperatures | 10 | 22 |
| **Subgroup 9** — Switching tests at 25°C — Digital devices | 7 | 32 |
| **Subgroup 10** — Switching tests at maximum rated operating temperature — Digital devices (Note 2) | 10 | 10 |
| **Subgroup 11** — Switching tests at minimum rated operating temperature — Digital devices (Note 2) | 10 | 10 |

1. Sampling plans are based on LTPD tables of MIL-M-38510. The smaller initial sample size, based on zero rejects allowed, has been chosen unless otherwise indicated. If necessary, the sample size will be increased once to the quantity corresponding to an acceptance number of 2. The minimum reject number in all cases is 3.
2. These subgroups are usually performed during initial device characterization only.

B

## OPTIONAL EXTENDED PROCESSING
## CLASS B
## Steps 101 Through 110

Advanced Micro Devices offers several extended processing options to meet customer high-reliability requirements. These are defined in AMD document 00-003. The flow chart below outlines Option B, a 160-hr burn in. Military temperature range devices processed to this flow (in the left column) meet the screening requirements of MIL-STD-883, Class B.




101 **BEGINNING MATERIAL**

Standard product taken after completion of step 20 (electrical test)

102 **BURN IN**

MIL-STD-883, Method 1015: 160 hr, 125°C, or time-temperature equivalents as allowed by Method 1015.

103 **FINAL ELECTRICAL TEST**

MIL-STD-883, Method 5004.

Military: Testing subgroups as defined for Class B. Static and functional at 3 temperatures, dynamic or switching at room temperature.

Commercial: Repeat step 20.

104 **QUALITY GROUP A ELECTRICAL SAMPLE (TABLE I)**

MIL-STD-883, Method 5005 and Table I. Quality levels as defined for Class B. Temperature correlations may be used on commercial products.

105 **QUALITY CONFORMANCE TESTS, GROUPS B, C, AND D**

MIL-STD-883, Method 5005. Sample life and environmental tests if required by purchase order. Further information on specifying this is given in AMD document 00-003.

106 **DATA PREPARATION AND REVIEW**

107 **MARK, INSPECT, PACK FOR SHIPMENT**

Standard AMD parts with this burn-in option are marked with "–B" after the part number, except that linear 100, 200 or 300 series are suffixed "/883B".

108 **QUALITY INSPECTION, PRE-SHIPMENT**

Confirmation of marking, physical quality, and product identity.

109 **QUALITY INSPECTION FOR SHIPMENT RELEASE**

Final review of shipment against order.

110 **SHIP TO CUSTOMER**

Military temperature range parts meet screening requirements of MIL-STD-883, Class B.

## OTHER OPTIONS

Document 00-003, "Extended Processing Options", further defines Option B as well as other screening or sampling options available or special order. Available options are listed here for reference.

| Option | Description | Effect |
|---|---|---|
| A | Modified Class A screen (Similar to Class S screening) | Provides space-grade product, following most Class S requirements of MIL-STD-883, Method 5004. |
| B | 160-hr operating burn in | Upgrades a part from Class C to Class B. |
| X | Radiographic inspection (X-ray) | Related to Option A. Provides limited internal inspection of sealed parts. |
| S | Scanning Electron Microscope (SEM) metal inspection | Sample inspection of metal coverage of die. |
| V | Preseal visual inspection to MIL-STD-883, Method 2010, Cond. A | More stringent visual inspection of assemblies and die surfaces prior to seal. |
| P | Particle impact noise (PIN) screen with ultrasonic detection. | Detects loose particles of approximately 0.5 mil size or larger, which could affect reliability in zero-G or high vibration applications. |
| Q | Quality conformance inspection (Group B, C and D life and environmental tests) | Samples from the lot are stressed and tested per Method 5005. The customer's order must state which groups are required. Group B destroys 16 devices; Group C, 92 devices; Group D, 60 devices. |

## PACKAGE PER DEVICE TYPE

| Device | Package-Temperature Code | | | | | | |
|---|---|---|---|---|---|---|---|
| | PC | DC | DM/DL | FM | CC | HC | HM |
| Am14/1506 | – | – | – | – | – | H-8-1 | H-8-1 |
| Am14/1507 | – | – | – | – | – | H-8-1 | H-8-1 |
| Am1702A | – | D-24-4* | D-24-4* | – | – | – | – |
| Am2401 | P-16-1 | D-16-2 | D-16-2 | – | – | – | – |
| Am2708 | – | D-24-4* | D-24-4* | – | – | – | – |
| Am2716 | – | D-24-4* | D-24-4* | – | – | – | – |
| Am2802 | P-16-1 | D-16-1 | D-16-1 | – | – | – | – |
| Am2803 | P-8-1 | – | – | – | – | H-8-1 | H-8-1 |
| Am2804 | P-8-1 | – | – | – | – | H-8-1 | H-8-1 |
| Am2805 | – | – | – | – | – | H-10-1 | H-10-1 |
| Am2806 | – | – | – | – | – | H-10-1 | H-10-1 |
| Am2807 | P-8-1 | – | – | – | – | – | – |
| Am2808 | P-8-1 | – | – | – | – | – | – |
| Am2809 | P-8-1 | – | – | – | – | H-8-1 | H-8-1 |
| Am2810 | P-16-1 | D-16-1 | D-16-1 | – | – | – | – |
| Am2812 | – | D-28-2 | D-28-2 | – | – | – | – |
| Am2813 | – | D-28-2 | D-28-2 | – | – | – | – |
| Am2814 | P-16-1 | D-16-2 | D-16-2 | – | – | – | – |
| Am2825 | P-10-1 | D-16-2 | D-16-2 | – | – | – | – |
| Am2826 | P-16-1 | D-16-2 | D-16-2 | – | – | – | – |
| Am2827 | P-8-1 | D-8-2 | D-8-2 | – | – | – | – |
| Am2833 | P-8-1 | D-8-2 | D-8-2 | – | – | – | – |
| Am2841 | P-16-1 | D-16-1 | D-16-1 | – | – | – | – |
| Am2847 | P-16-1 | D-16-1 | D-16-1 | – | – | – | – |
| Am2855 | P-16-1 | D-16-1 | D-16-1 | – | – | – | – |
| Am2856 | P-10-1 | – | – | – | – | H-10-1 | H-10-1 |
| Am2857 | P-8-1 | D-8-2 | D-8-2 | – | – | – | – |
| Am2896 | P-16-1 | D-16-1 | D-16-1 | – | – | – | – |
| Am4025/5025 | P-10-1 | D-16-1 | D-16-1 | – | – | – | – |
| Am4026/5026 | P-16-1 | D-16-1 | D-16-1 | – | – | – | – |
| Am4027/5027 | P-8-1 | D-8-2 | D-8-2 | – | – | – | – |
| Am4055/5055 | P-16-1 | D-16-1 | D-16-1 | – | – | – | – |
| Am4056/5056 | – | – | – | – | – | H-10-1 | H-10-1 |
| Am4057/5057 | P-8-1 | D-8-2 | D-8-2 | – | – | – | – |
| Am8035 | P-40-1 | – | – | – | D-40-1 | – | – |
| Am8041 | P-40-1 | – | – | – | D-40-1 | – | – |
| Am8048 | P-40-1 | – | – | – | D-40-1 | – | – |
| Am8085A | P-40-1 | D-40-1 | D-40-1 | – | D-40-1 | – | – |
| Am8155 | P-40-1 | – | – | – | D-40-1 | – | – |
| Am8156 | P-40-1 | – | – | – | D-40-1 | – | – |
| Am8253 | P-24-1 | – | – | – | D-24-1 | – | – |
| Am8255A | P-40-1 | – | D-40-1 | – | D-40-1 | – | – |
| Am8279 | P-40-1 | – | – | – | D-40-1 | – | – |
| Am9016 | P-16-1 | D-16-1 | D-16-1 | – | – | – | – |
| Am9044 | P-18-1 | D-18-1 | D-18-1 | – | – | – | – |
| Am90L44 | P-18-1 | D-18-1 | D-18-1 | – | – | – | – |
| Am9080 | P-40-1 | D-40-1 | D-40-1 | – | D-40-1 | – | – |
| Am9101 | P-22-1 | D-22-1 | D-22-1 | – | – | – | – |
| Am91L01 | P-22-1 | D-22-1 | D-22-1 | – | – | – | – |
| Am9111 | P-18-1 | D-18-1 | D-18-1 | – | – | – | – |
| Am91L11 | P-18-1 | D-18-1 | D-18-1 | – | – | – | – |
| Am9112 | P-16-1 | D-16-1 | D-16-1 | – | – | – | – |
| Am91L12 | P-16-1 | D-16-1 | D-16-1 | – | – | – | – |
| Am9114 | P-18-1 | D-18-1 | D-18-1 | – | – | – | – |
| Am91L14 | P-18-1 | D-18-1 | D-18-1 | – | – | – | |

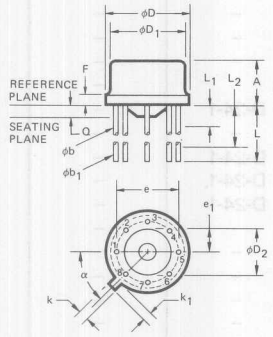
## PACKAGE PER DEVICE TYPE (Cont.)

| Device | Package-Temperature Code | | | | | | |
|---|---|---|---|---|---|---|---|
| | PC | DC | DM/DL | FM | CC | HC | HM |
| Am9124 | P-18-1 | D-18-1 | D-18-1 | F-18-2 | – | – | – |
| Am91L24 | P-18-1 | D-18-1 | D-18-1 | F-18-2 | – | – | – |
| Am9130 | P-22-1 | D-22-1 | D-22-1 | – | – | – | – |
| Am91L30 | P-22-1 | D-22-1 | D-22-1 | – | – | – | – |
| Am9131 | P-22-1 | D-22-1 | D-22-1 | – | – | – | – |
| Am91L31 | P-22-1 | D-22-1 | D-22-1 | – | – | – | – |
| Am9140 | P-22-1 | D-22-1 | D-22-1 | F-22-1 | – | – | – |
| Am91L40 | P-22-1 | D-22-1 | D-22-1 | F-22-1 | – | – | – |
| Am9141 | P-22-1 | D-22-1 | D-22-1 | F-22-1 | – | – | – |
| Am91L41 | P-22-1 | D-22-1 | D-22-1 | F-22-1 | – | – | – |
| Am9147 | – | D-18-1 | D-18-1 | F-18-2 | – | – | – |
| Am9208 | P-24-1 | D-24-2 | D-24-2 | – | – | – | – |
| Am9214/3514 | – | D-24-2 | D-24-2 | – | D-24-1 | – | – |
| Am9216 | P-24-1 | D-24-2 | D-24-2 | – | – | – | – |
| Am9217/8316A | P-24-1 | D-24-2 | D-24-2 | – | D-24-1 | – | – |
| Am9218/8316E | P-24-1 | D-24-2 | D-24-2 | – | D-24-1 | – | – |
| Am9232/9233 | P-24-1 | D-24-2 | D-24-2 | – | D-24-1 | – | – |
| Am9244 | P-18-1 | D-18-1 | D-18-1 | F-18-2 | – | – | – |
| Am92L44 | P-18-1 | D-18-1 | D-18-1 | F-18-2 | – | – | – |
| Am9511A | – | D-24-2 | D-24-2 | – | – | – | – |
| Am9512 | – | D-24-2 | D-24-2 | – | – | – | – |
| Am9513 | – | D-40-1 | D-40-1 | – | – | – | – |
| Am9517A | P-40-1 | D-40-1 | D-40-1 | – | – | – | – |
| Am9519 | P-28-1 | D-28-1 | D-28-1 | – | – | – | – |
| Am9551 | P-28-1 | D-28-1 | D-28-1 | – | D-28-1 | – | – |
| Am9555 | P-40-1 | D-40-1 | D-40-1 | – | D-40-1 | – | – |
| Am9557 | P-40-1 | D-40-1 | D-40-1 | – | – | – | – |

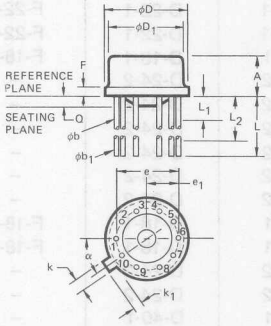
C

## METAL CAN PACKAGES

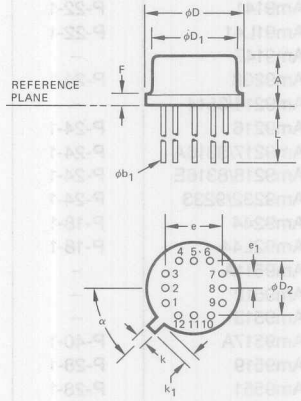
H-8-1




H-10-1




G-12-1



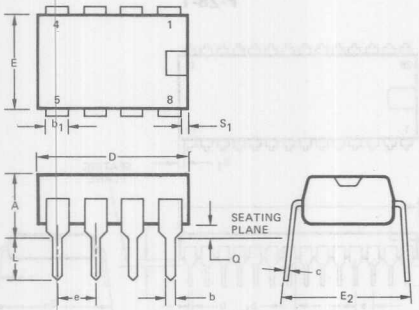

| AMD Pkg. | H-8-1 | | H-10-1 | | G-12-1 | |
|---|---|---|---|---|---|---|
| Common Name | TO-99 Metal Can | | TO-100 Metal Can | | TO-8 Metal Can | |
| 38510 Appendix C | A-1 | | A-2 | | – | |
| Parameters | Min. | Max. | Min. | Max. | Min. | Max. |
| A | .165 | .185 | .165 | .185 | .155 | .180 |
| e | .185 | .215 | .215 | .245 | .390 | .410 |
| $e_1$ | .090 | .110 | .105 | .125 | .090 | .110 |
| F | .013 | .033 | .013 | .033 | .020 | .030 |
| k | .027 | .034 | .027 | .034 | .024 | .034 |
| $k_1$ | .027 | .045 | .027 | .045 | .024 | .038 |
| L | .500 | .570 | .500 | .610 | .500 | .600 |
| $L_1$ | | .050 | | .050 | | |
| $L_2$ | .250 | | .250 | | | |
| α | 45° BSC | | 36° BSC | | 45° | |
| ϕb | .016 | .019 | .016 | .019 | | |
| $\phi b_1$ | .016 | .021 | .016 | .021 | .016 | .021 |
| ϕD | .350 | .370 | .350 | .370 | .590 | .610 |
| $\phi D_1$ | .305 | .335 | .305 | .335 | .540 | .560 |
| $\phi D_2$ | .120 | .160 | .120 | .160 | .390 | .410 |
| Q | .015 | .045 | .015 | .045 | | |

Notes: 1. Standard lead finish is bright acid tin plate or gold plate.
2. ϕb applies between $L_1$ and $L_2$. $\phi b_1$ applies between $L_1$ and 0.500" beyond reference plane.

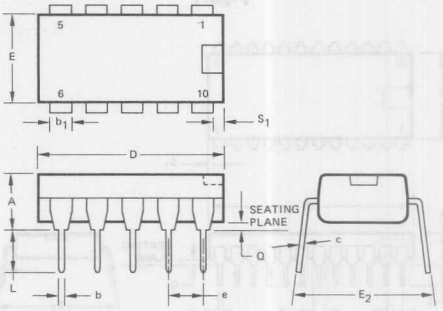
## PACKAGE OUTLINES (Cont.)

### MOLDED DUAL IN-LINE PACKAGES

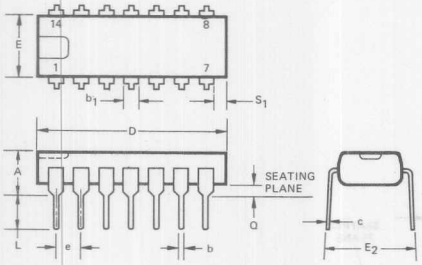
P-8-1



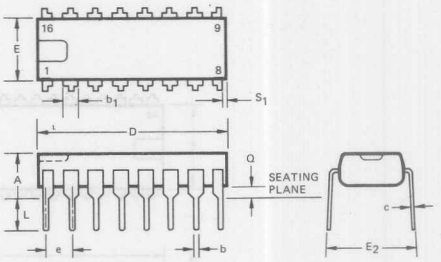

P-10-1



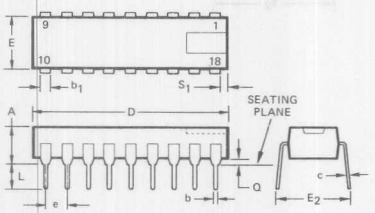

P-14-1



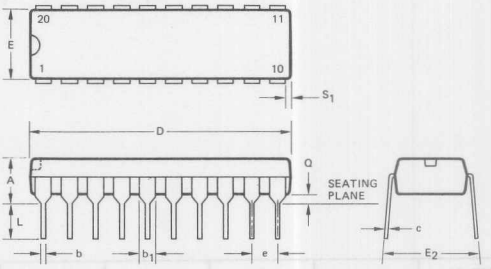

P-16-1



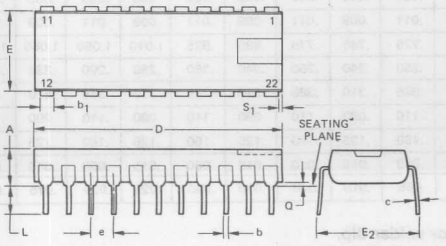

P-18-1




P-20-1




P-22-1

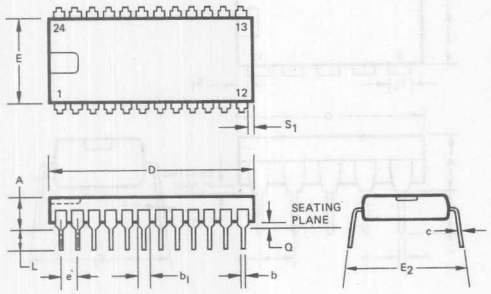



C

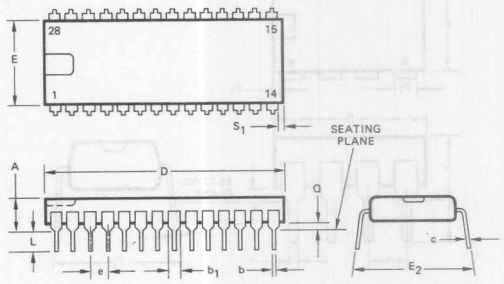
## PACKAGE OUTLINES (Cont.)

### MOLDED DUAL IN-LINE PACKAGES (Cont.)

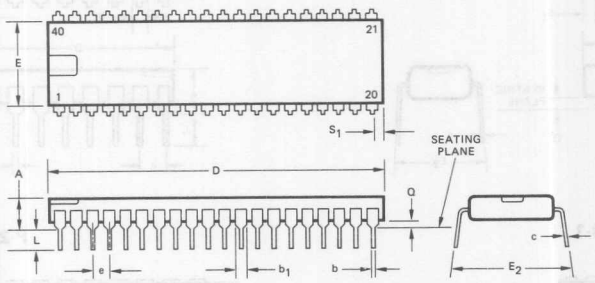
P-24-1




P-28-1




P-40-1



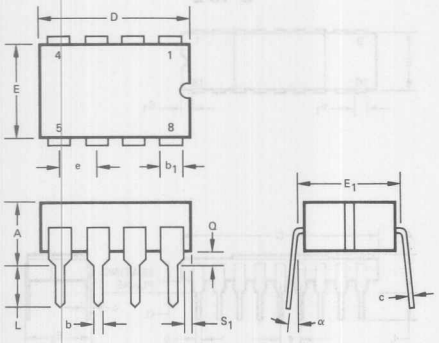

| AMD Pkg. | P-8-1 | | P-10-1 | | P-14-1 | | P-16-1 | | P-18-1 | | P-20-1 | | P-22-1 | | P-24-1 | | P-28-1 | | P-40-1 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Parameters | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. |
| A | .150 | .200 | .150 | .200 | .150 | .200 | .150 | .200 | .150 | .200 | .150 | .200 | .150 | .200 | .170 | .215 | .150 | .200 | .150 | .200 |
| b | .015 | .022 | .015 | .020 | .015 | .020 | .015 | .020 | .015 | .020 | .015 | .020 | .015 | .020 | .015 | .020 | .015 | .020 | .015 | .020 |
| $b_1$ | .055 | .065 | .055 | .065 | .055 | .065 | .055 | .065 | .055 | .065 | .055 | .065 | .055 | .065 | .055 | .065 | .055 | .065 | .055 | .065 |
| c | .009 | .011 | .009 | .011 | .009 | .011 | .009 | .011 | .009 | .011 | .009 | .011 | .009 | .011 | .009 | .011 | .009 | .011 | .009 | .011 |
| D | .375 | .395 | .505 | .550 | .745 | .775 | .745 | .775 | .895 | .925 | 1.010 | 1.050 | 1.080 | 1.120 | 1.240 | 1.270 | 1.450 | 1.480 | 2.050 | 2.080 |
| E | .240 | .260 | .240 | .260 | .240 | .260 | .240 | .260 | .240 | .260 | .250 | .290 | .330 | .370 | .515 | .540 | .530 | .550 | .530 | .550 |
| $E_2$ | .310 | .385 | .310 | .385 | .310 | .385 | .310 | .385 | .310 | .385 | .310 | .385 | .410 | .480 | .585 | .700 | .585 | .700 | .585 | .700 |
| e | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 |
| L | .125 | .150 | .125 | .150 | .125 | .150 | .125 | .150 | .125 | .150 | .125 | .150 | .125 | .160 | .125 | .160 | .125 | .160 | .125 | .160 |
| Q | .015 | .060 | .015 | .060 | .015 | .060 | .015 | .060 | .015 | .060 | .015 | .060 | .015 | .060 | .015 | .060 | .015 | .060 | .015 | .060 |
| $S_1$ | .010 | .030 | .040 | .070 | .040 | .065 | .010 | .040 | .030 | .040 | .025 | .055 | .015 | .045 | .035 | .065 | .040 | .070 | .040 | .070 |

Notes: 1. Standard lead finish is tin plate or solder dip.
2. Dimension $E_2$ is an outside measurement.

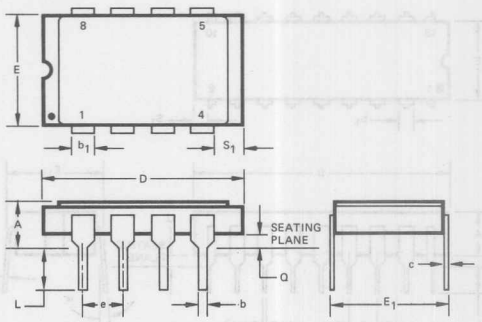
## PACKAGE OUTLINES (Cont.)

### HERMETIC DUAL IN-LINE PACKAGES

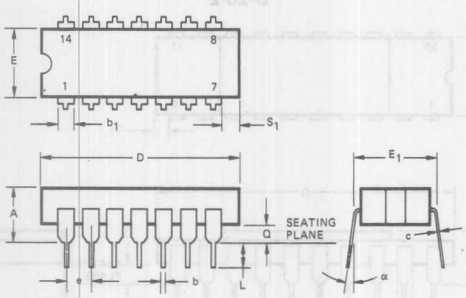
D-8-1



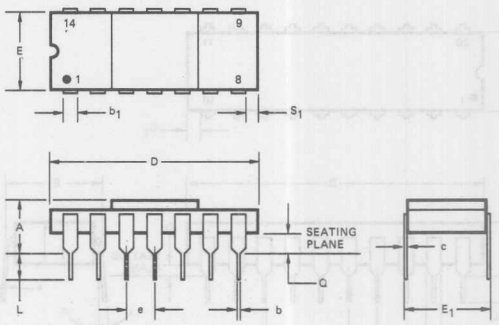

D-8-2



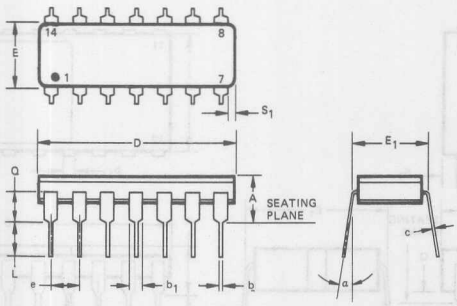

D-14-1



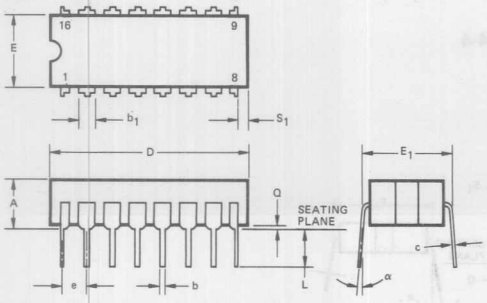

D-14-2



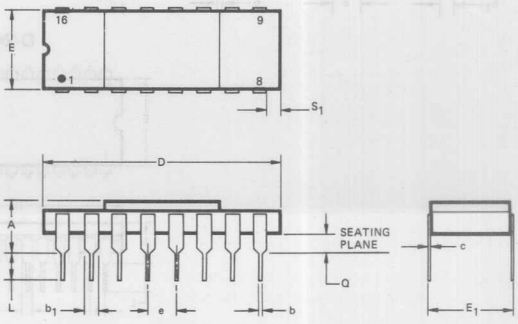

D-14-3




D-16-1




D-16-2

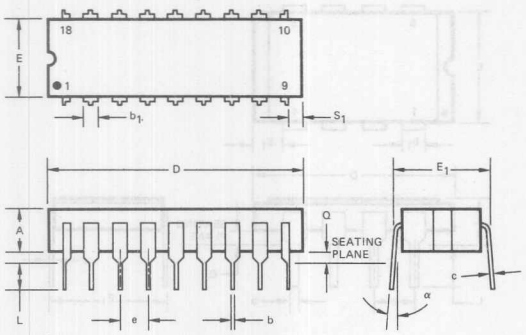



C

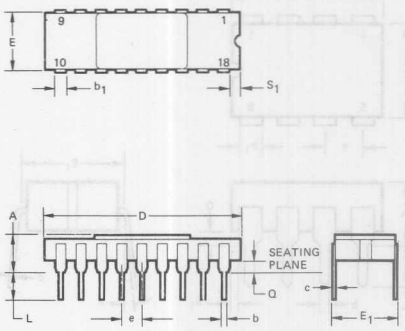
## PACKAGE OUTLINES (Cont.)

### HERMETIC DUAL IN-LINE PACKAGES (Cont.)

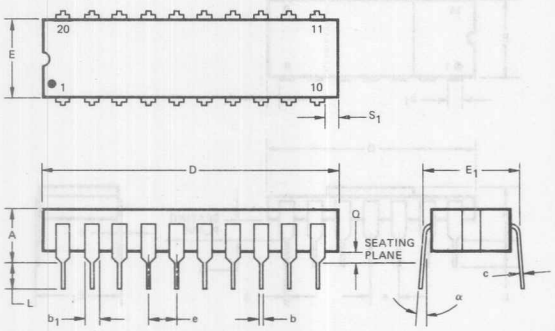
D-18-1



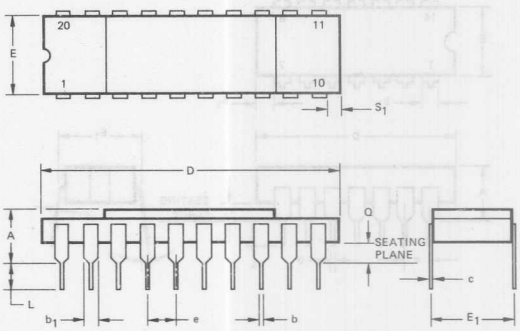

D-18-2



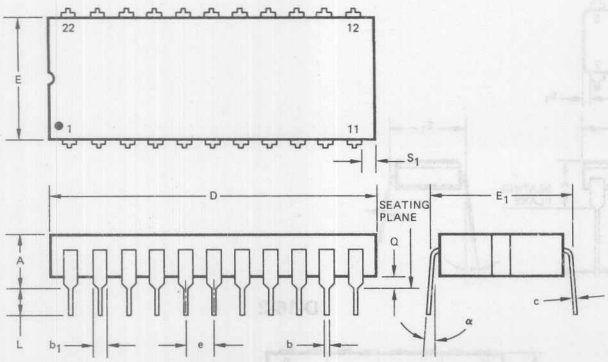

D-20-1



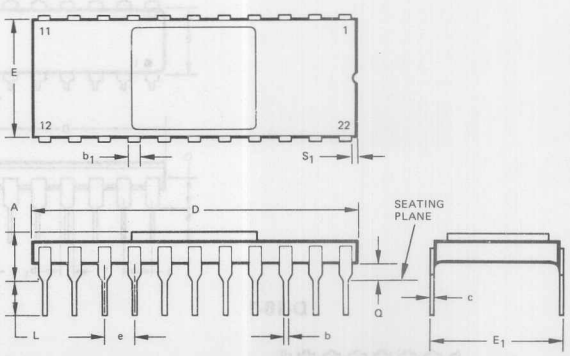

D-20-2



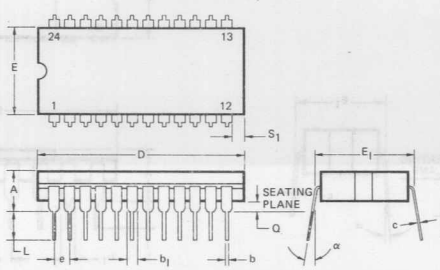

D-22-1




D-22-2



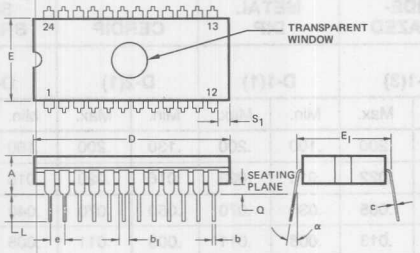

D-24-1 and D-24-4



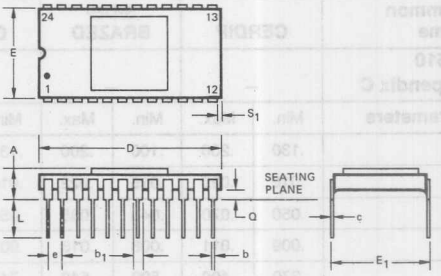
## PACKAGE OUTLINES (Cont.)

### HERMETIC DUAL IN-LINE PACKAGES (Cont.)

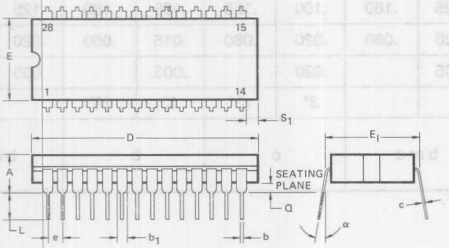
D-24-4*



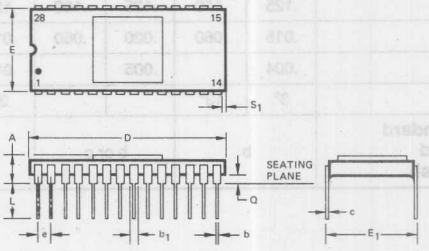

D-24-2



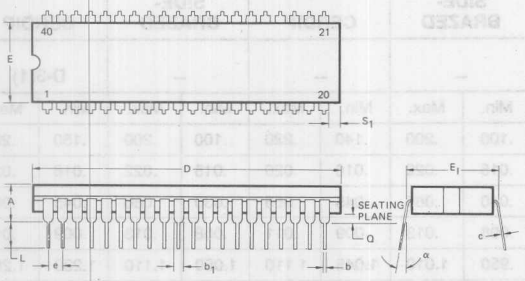

D-28-1



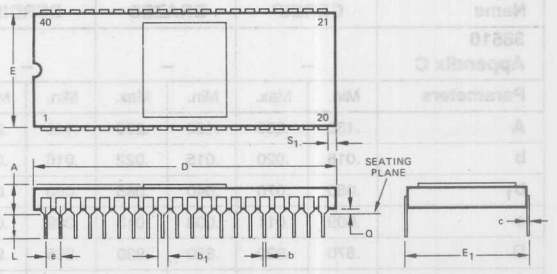

D-28-2



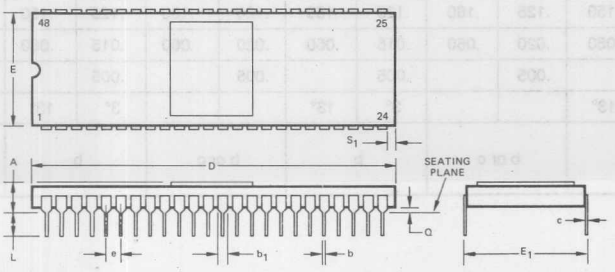

D-40-1




D-40-2




D-48-2




C

## PACKAGE OUTLINES (Cont.)

### HERMETIC DUAL IN-LINE PACKAGES (Cont.)

| AMD Pkg. | D-8-1 | | D-8-2 | | D-14-1 | | D-14-2 | | D-14-3 (Note 2) | | D-16-1 | | D-16-2 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Common Name | CERDIP | | SIDE-BRAZED | | CERDIP | | SIDE-BRAZED | | METAL DIP | | CERDIP | | SIDE-BRAZED | |
| 38510 Appendix C | – | | – | | D-1(1) | | D-1(3) | | D-1(1) | | D-2(1) | | D-2(3) | |
| Parameters | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. |
| A | .130 | .200 | .100 | .200 | .130 | .200 | .100 | .200 | .100 | .200 | .130 | .200 | .100 | .200 |
| b | .016 | .020 | .015 | .022 | .016 | .020 | .015 | .022 | .015 | .023 | .016 | .020 | .015 | .022 |
| $b_1$ | .050 | .070 | .040 | .065 | .050 | .070 | .040 | .065 | .030 | .070 | .050 | .070 | .040 | .065 |
| c | .009 | .011 | .008 | .013 | .009 | .011 | .008 | .013 | .008 | .011 | .009 | .011 | .008 | .013 |
| D | .370 | .400 | .500 | .540 | .745 | .785 | .690 | .730 | .660 | .785 | .745 | .785 | .780 | .820 |
| E | .240 | .285 | .260 | .310 | .240 | .285 | .260 | .310 | .230 | .265 | .240 | .310 | .260 | .310 |
| $E_1$ | .300 | .320 | .290 | .320 | .290 | .320 | .290 | .320 | .290 | .310 | .290 | .320 | .290 | .320 |
| e | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 |
| L | .125 | .150 | .125 | .160 | .125 | .150 | .125 | .160 | .100 | .150 | .125 | .150 | .125 | .160 |
| Q | .015 | .060 | .020 | .060 | .015 | .060 | .020 | .060 | .020 | .080 | .015 | .060 | .020 | .060 |
| $S_1$ | .004 | | .005 | | .010 | | .005 | | .020 | | .005 | | .005 | |
| $\alpha$ | 3° | 13° | | | 3° | 13° | | | 3° | 13° | 3° | 13° | | |
| Standard Lead Finish | b | | b or c | | b | | b or c | | c | | b | | b or c | |

| AMD Pkg. | D-18-1 | | D-18-2 | | D-20-1 | | D-20-2 | | D-22-1 | | D-22-2 | | D-24-1 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Common Name | CERDIP | | SIDE-BRAZED | | CERDIP | | SIDE-BRAZED | | CERDIP | | SIDE-BRAZED | | CERDIP | |
| 38510 Appendix C | – | | – | | – | | – | | – | | – | | D-3(1) | |
| Parameters | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. |
| A | .130 | .200 | .100 | .200 | .140 | .220 | .100 | .200 | .140 | .220 | .100 | .200 | .150 | .225 |
| b | .016 | .020 | .015 | .022 | .016 | .020 | .015 | .022 | .016 | .020 | .015 | .022 | .016 | .020 |
| $b_1$ | .050 | .070 | .040 | .065 | .050 | .070 | .040 | .065 | .045 | .065 | .030 | .060 | .045 | .065 |
| c | .009 | .011 | .008 | .013 | .009 | .011 | .008 | .013 | .009 | .011 | .008 | .013 | .009 | .011 |
| D | .870 | .920 | .850 | .930 | .935 | .970 | .950 | 1.010 | 1.045 | 1.110 | 1.050 | 1.110 | 1.230 | 1.285 |
| E | .280 | .310 | .260 | .310 | .245 | .285 | .260 | .310 | .360 | .405 | .360 | .410 | .510 | .545 |
| $E_1$ | .290 | .320 | .290 | .320 | .290 | .320 | .290 | .320 | .390 | .420 | .390 | .420 | .600 | .620 |
| e | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 |
| L | .125 | .150 | .125 | .160 | .125 | .150 | .125 | .160 | .125 | .150 | .125 | .160 | .120 | .150 |
| Q | .015 | .060 | .020 | .060 | .015 | .060 | .020 | .060 | .015 | .060 | .020 | .060 | .015 | .060 |
| $S_1$ | .005 | | .005 | | .005 | | .005 | | .005 | | .005 | | .010 | |
| $\alpha$ | 3° | 13° | | | 3° | 13° | | | 3° | 13° | | | 3° | 13° |
| Standard Lead Finish | b | | b or c | | b | | b or c | | b | | b or c | | b | |

## PACKAGE OUTLINES (Cont.)

### HERMETIC DUAL IN-LINE PACKAGES (Cont.)

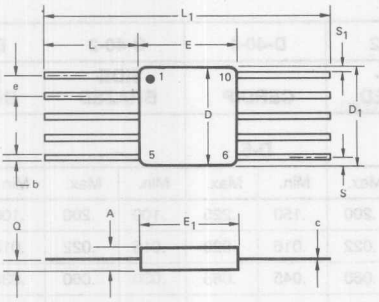
| AMD Pkg. | D-24-2 | | D-24-4/D-24-4* | | D-28-1 | | D-28-2 | | D-40-1 | | D-40-2 | | D-48-2 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Common Name | SIDE-BRAZED | | CERVIEW | | CERDIP | | SIDE-BRAZED | | CERDIP | | SIDE-BRAZED | | SIDE-BRAZED | |
| 38510 Appendix C | D-3(3) | | – | | – | | – | | D-5 | | – | | – | |
| Parameters | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. |
| A | .100 | .200 | .150 | .225 | .150 | .225 | .100 | .200 | .150 | .225 | .100 | .200 | .100 | .200 |
| b | .015 | .022 | .016 | .020 | .016 | .020 | .015 | .022 | .016 | .020 | .015 | .022 | .015 | .022 |
| $b_1$ | .030 | .060 | .045 | .065 | .045 | .065 | .030 | .060 | .045 | .065 | .030 | .060 | .030 | .060 |
| c | .008 | .013 | .009 | .011 | .009 | .011 | .008 | .013 | .009 | .011 | .008 | .013 | .008 | .013 |
| D | 1.170 | 1.200 | 1.235 | 1.280 | 1.440 | 1.500 | 1.380 | 1.420 | 2.020 | 2.100 | 1.960 | 2.040 | 2.370 | 2.430 |
| E | .550 | .610 | .510 | .550 | .510 | .550 | .560 | .600 | .510 | .550 | .550 | .610 | .570 | .610 |
| $E_1$ | .590 | .620 | .600 | .630 | .600 | .630 | .590 | .620 | .600 | .630 | .590 | .620 | .590 | .620 |
| e | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 | .090 | .110 |
| L | .120 | .160 | .120 | .150 | .120 | .150 | .120 | .160 | .120 | .150 | .120 | .160 | .125 | .160 |
| Q | .020 | .060 | .015 | .060 | .015 | .060 | .020 | .060 | .015 | .060 | .020 | .060 | .020 | .060 |
| $S_1$ | .005 | | .010 | | .005 | | .005 | | .005 | | .005 | | .005 | |
| $\alpha$ | | | 3° | 13° | 3° | 13° | | | 3° | 13° | | | | |
| Standard Lead Finish | b or c | | | | b | | b | | b | | b or c | | b or c | |

Notes: 1. Load finish b is tin plate. Finish c is gold plate.
2. Used only for LM108/LM108A.
3. Dimensions E and D allow for off-center lid, meniscus and glass overrun.

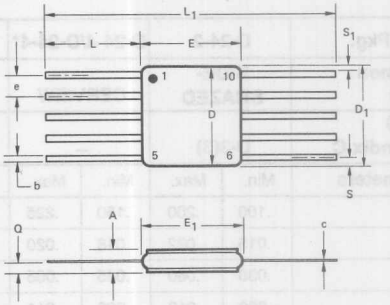
C

## FLAT PACKAGES

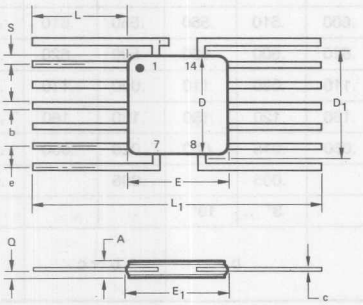
### F-10-1



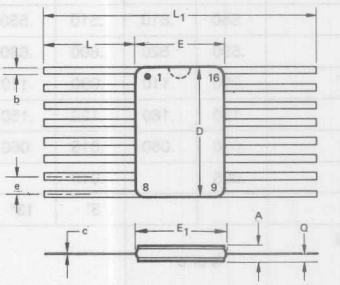

### F-10-2




### F-14-1 and F-14-2

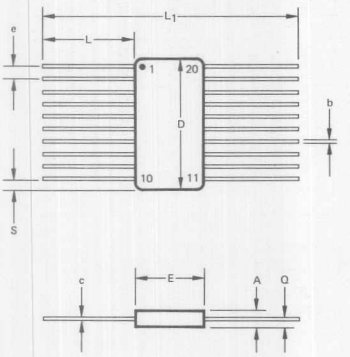



### F-16-1 and F-16-2

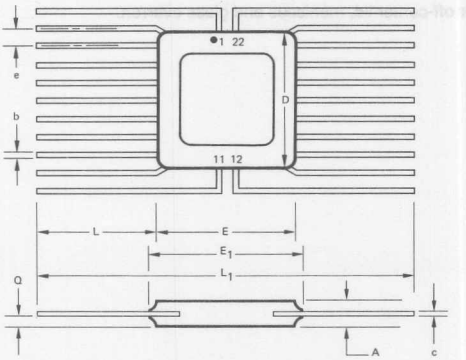



Note: Notch is pin 1 index on cerpack.

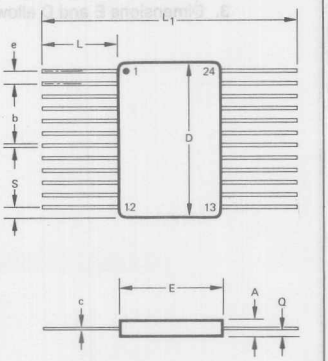
### F-20-1



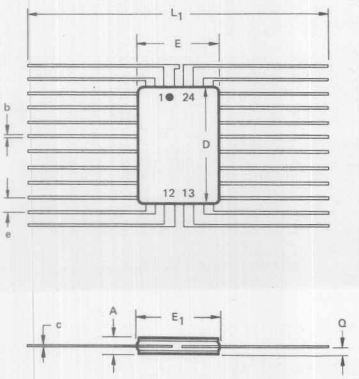

### F-22-1



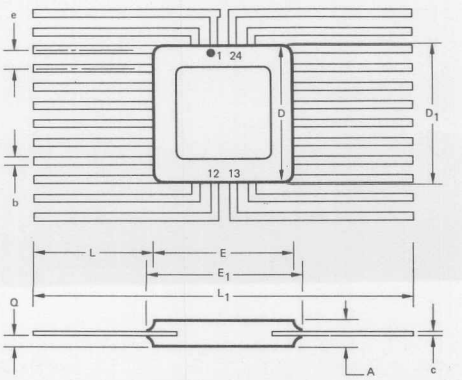

### F-24-1



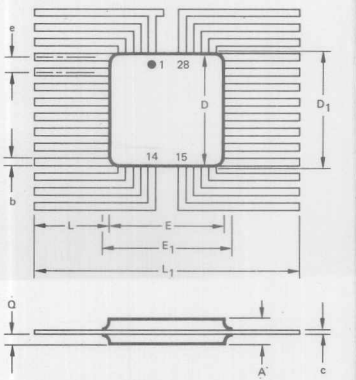

### F-24-2




### F-24-3



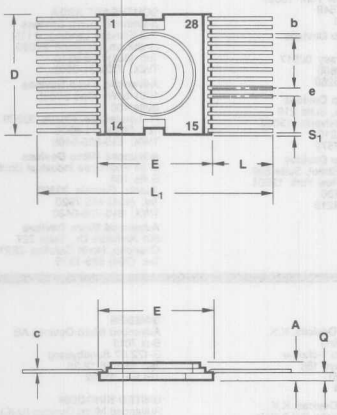

### F-28-1



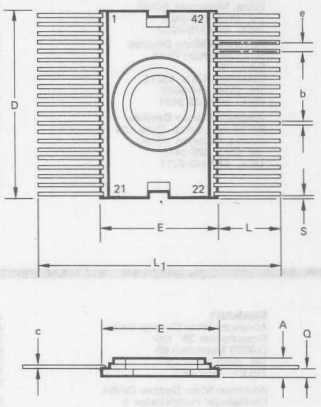
## PACKAGE OUTLINES (Cont.)

### FLAT PACKAGES (Cont.)

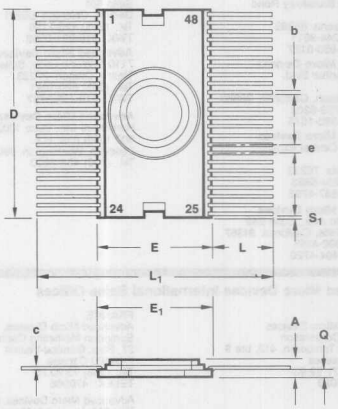
F-28-2




F-42-1




F-48-2




| AMD Pkg. | F-10-1 | | F-10-2 | | F-14-1 | | F-14-2 | | F-16-1 | | F-16-2 | | F-20-1 | | F-22-1 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Common NAME | CERPACK | | METAL FLAT PAK | | CERPACK | | METAL FLAT PAK | | CERPACK | | METAL FLAT PAK | | CERPACK | | METAL FLAT PAK | |
| 38510 Appendix C | F-4 | | F-4 | | .F-1 | | F-1 | | F-5 | | – | | – | | – | |
| Parameters | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. |
| A | .045 | .080 | .045 | .080 | .045 | .080 | .045 | .085 | .045 | .085 | .045 | .085 | .045 | .085 | .045 | .090 |
| b | .015 | .019 | .012 | .019 | .015 | .019 | .012 | .019 | .015 | .019 | .015 | .019 | .015 | .019 | .015 | .019 |
| c | .004 | .006 | .003 | .006 | .004 | .006 | .003 | .006 | .004 | .006 | .003 | .006 | .004 | .006 | .003 | .006 |
| D | .230 | .255 | .235 | .275 | .230 | .255 | .230 | .270 | .370 | .425 | .370 | .400 | .490 | .520 | .380 | .420 |
| $D_1$ | | | | .275 | | | | .280 | | | | .410 | | | | .440 |
| E | .240 | .260 | .240 | .260 | .240 | .260 | .240 | .260 | .245 | .285 | .245 | .285 | .245 | .285 | .380 | .420 |
| $E_1$ | | .275 | | .280 | | .275 | | .280 | | .290 | | .305 | | .290 | | .440 |
| e | .045 | .055 | .045 | .055 | .045 | .055 | .045 | .055 | .045 | .055 | .045 | .055 | .045 | .055 | .045 | .055 |
| L | .300 | .370 | .300 | .370 | .300 | .370 | .300 | .370 | .300 | .370 | .300 | .370 | .300 | .370 | .250 | .320 |
| $L_1$ | .920 | .980 | .920 | .980 | .920 | .980 | .920 | .980 | .920 | .980 | .920 | .980 | .920 | .980 | .920 | .980 |
| Q | .010 | .040 | .010 | .040 | .010 | .040 | .010 | .040 | .020 | .040 | .010 | .040 | .020 | .040 | .010 | .040 |
| $S_1$ | .005 | | .005 | | .005 | | .005 | | .005 | | .005 | | .005 | | | |
| Standard Lead Finish | b | | c | | b | | c | | b | | c | | b | | c | |

| AMD Pkg. | F-24-1 | | F-24-2 | | F-24-3 | | F-28-1 | | F-28-2 | | F-42-1 | | F-48-2 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Common Name | CERPACK | | METAL FLAT PAK | | METAL FLAT PAK | | METAL FLAT PAK | | CERAMIC FLAT PAK | | CERAMIC FLAT PAK | | CERAMIC FLAT PAK | |
| 38510 Appendix C | F-6 | | F-8 | | – | | – | | – | | – | | – | |
| Parameters | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. |
| A | .050 | .090 | .045 | .090 | .045 | .090 | .045 | .080 | .065 | .085 | .070 | .115 | .070 | .110 |
| b | .015 | .019 | .015 | .019 | .015 | .019 | .015 | .019 | .016 | .025 | .017 | .023 | .018 | .022 |
| c | .004 | .006 | .003 | .006 | .003 | .006 | .003 | .006 | .007 | .010 | .006 | .012 | .006 | .010 |
| D | .580 | .620 | .360 | .410 | .380 | .420 | .360 | .410 | .700 | .720 | 1.030 | 1.090 | 1.175 | 1.250 |
| $D_1$ | | | | .420 | | .440 | | .410 | | .720 | | 1.090 | | 1.250 |
| E | .360 | .385 | .245 | .285 | .380 | .420 | .360 | .410 | .625 | .650 | .620 | .660 | .615 | .670 |
| $E_1$ | | .410 | | .305 | | .440 | | .410 | | .650 | | .660 | | .670 |
| e | .045 | .055 | .045 | .055 | .045 | .055 | .045 | .055 | .045 | .055 | .045 | .055 | .045 | .055 |
| L | .265 | .320 | .300 | .370 | .250 | .320 | .270 | .320 | .415 | .435 | .320 | .370 | .320 | .370 |
| $L_1$ | .920 | .980 | .920 | .980 | .920 | .980 | .955 | 1.000 | 1.475 | 1.500 | 1.300 | 1.370 | 1.310 | 1.365 |
| Q | .020 | .040 | .010 | .040 | .010 | .040 | .010 | .040 | .017 | .025 | .020 | .060 | .020 | .055 |
| $S_1$ | .005 | | .005 | | 0 | | 0 | | .005 | | .005 | | .015 | |
| Standard Lead Finish | b | | c | | c | | c | | c | | c | | c | |

Notes: 1. Lead finish b is tin plate. Finish c is gold plate.
2. Dimensions $E_1$ and $D_1$ allow for off-center lid, meniscus, and glass overrun.

C

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